Orthogonal Printing of Uniform Nanocomposite Monolayer and Oriented Organic Semiconductor Crystals for High-Performance Nano-Crystal Floating Gate Memory

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Abstract

Inkjet printing is of great interest in the preparation of optoelectronic and microelectronic devices due to its low cost, low process temperature, versatile material compatibility, and ability to precisely manufacture multi-layer devices on demand. However, interlayer solvent erosion is a typical problem that limits the printing of organic semiconductor devices with multi-layer structures. In this study, we proposed a solution to address this erosion problem by designing polystyrene-*block*-poly(4-vinyl pyridine)-grafted Au nanoparticles (Au@PS-*b*-P4VP NPs). With a colloidal ink containing the Au@PS-*b*-P4VP NPs, we obtained a uniform monolayer of Au nano-crystal floating gates (NCFGs) embedded in the PS-*b*-P4VP tunneling dielectric (TD) layer using direct-ink-writing (DIW). Significantly, PS-*b*-P4VP has high erosion resistance against the semiconductor ink solvent, which enables multi-layer printing. An active layer of semiconductor crystals with high crystallinity and well-orientation was obtained by DIW. Moreover, we developed a strategy to improve the quality of the TD/semiconductor interface by introducing a polystyrene intermediate layer. We show that the NCFG memory devices exhibit a low threshold voltage (< 3 V), large memory window (66 V), stable endurance (> 100 cycles), and long-term retention (> 10 years). This study provides universal guidance for printing functional coatings and multi-layer devices.

KEYWORDS: Nano-crystal floating gate memory; polymer-grafted nanoparticles; organic thin-film devices; direct-ink-writing; self-assembly

1. Introduction

Non-volatile memory devices are ubiquitous in computers, mobile phones, U-disks, and many other electronic products [1, 2]. Among these devices, flash memory devices with floating gates [3], particularly discrete nano-crystal floating gates (NCFGs) embedded in a tunneling dielectric (TD) layer, are attractive due to their high density of capture/trap sites and stable data storage ability[4-8]. There has been great progress in designing NCFG memory devices [9-12], particularly those with an inorganic/organic composite NCFG/TD layer and active layer [13-18]. Previous studies suggest that a uniform NCFG/TD composite layer can prolong the trapped charge retention time and reduce the leakage current [19, 20]. On the other hand, oriented semiconductor crystals in the active layer can significantly improve mobility [21-23]. However, NCFG memory devices with both a uniform NCFG/TD composite layer and an oriented active layer have rarely been reported.

Printing polymer-grafted nanoparticles (NPs) is an effective solution processing and integrated preparation method for uniform inorganic/organic composite NCFG/TD layer. Among various solution processing technologies [19, 20, 24, 25], inkjet printing is of great interest due to its ability to precise digital control, efficient material utilization, versatility of ink materials, and its capability to directly deposit a patterned thin film on large substrates. Combining printing technology with convective self-assembly allows the deposition of a uniform monolayer of NPs [26]. Grafting dielectric polymers on the surface of NCFGs enables uniform dispersion of NCFGs in the polymer TD layer. In our previous study, we obtained a uniform monolayer array of Au NCFGs embedded in a polystyrene (PS) TD layer via direct-ink writing (DIW) of PS-grafted AuNPs [27]. However, the poor solvent resistance of traditional homopolymer ligands (such as PS) limits the printing of the upper active layer on the top of polymer TD layer.

3

Printing has also been widely used for the preparation of active layers in other transistor or diode thin-film devices due to its capability of producing oriented semiconductor crystals [28, 29]. Usually, the orientation of semiconductor crystals shortens the π-π distance and provides optimal charge carrier transport paths, which improves the mobility of organic semiconductor devices [21, 22, 30]. Bao et al. reported that the mobility of their blade-coated devices from 0.8 $cm^2 V^{-1} s^{-1}$ to 4.6 $cm^2 V^{-1} s^{-1}$ while the π-π distance of crystals decreased from 3.33 Å to 3.08 Å [21]. Furthermore, the mobility can be improved to 11 $cm^2 V^{-1} s^{-1}$ through fluid-enhanced crystal growth by blade-coating with micropillars [28]. Owing to directional fluid shearing, DIW printing allows the orientation of semiconductor crystals in the active layer [31-34]. Liu et al. showed that by adjusting printing speed, the mobility of the device with oriented crystals is double than that of non-oriented crystals [33]. Song et al. presented the control of crystal orientations on substrates with a patterned wettability by adjusting the evaporation rate, crystallization rate, and meniscus triple-phase contact line (TPCL) shape. The device's mobility was enhanced more than 5 times with the purely oriented semiconductor crystals [34]. It would be of great interest to print NCFG memory devices with combination of an oriented active layer and a uniform NP/polymer composite thin film. However, interlayer solvent erosion is an obstacle [35]. It is desirable to develop a polymer matrix that is resistant to the solvent of semiconductors.

In this work, we present a printable NCFG memory device with a uniform NCFG/TD composite layer of block-copolymer (BCP) grafted NPs, an active layer with well-oriented semiconductor crystals, and a polymer intermediate layer (**Scheme 1**). The NCFG/TD composite layer is printed by evaporation-induced self-assembly of PS-*block*-poly(4-vinyl pyridine) (PS-*b*-P4VP)-grafted AuNPs using DIW technology. The BCP, PS-*b*-P4VP, can withstand erosion by the solvent of the

semiconductor ink and allows us to print the upper active layer. In addition, we introduce a PS intermediate layer between the TD/semiconductor interface via vertical phase separation. The intermediate layer can reduce interfacial traps and serve as an electret for charge storage. Benefiting from the synergistic effects of the high crystal quality active layer and the intermediate layer, the NCFG memory devices exhibit much more improved performance than those with an active layer prepared by traditional chemical vapor deposition (CVD).
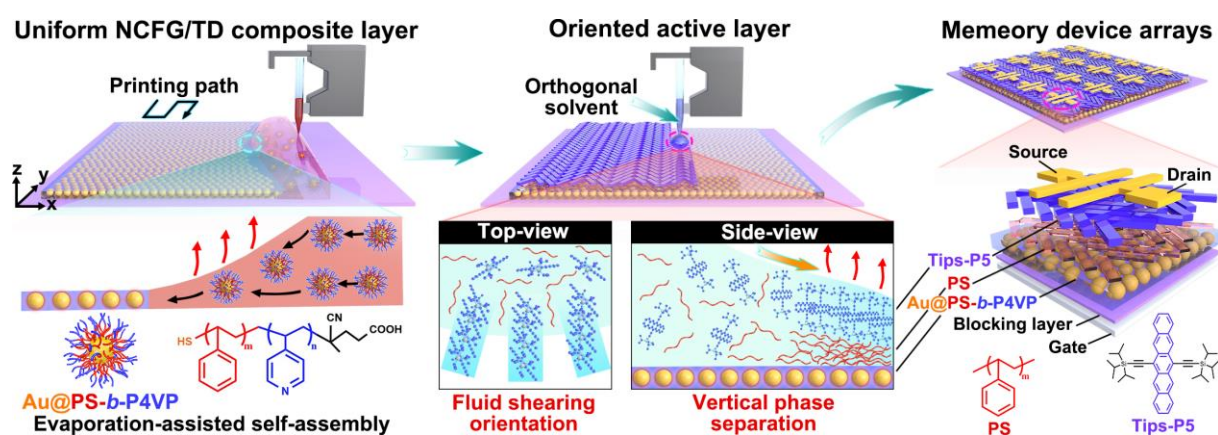
Scheme 1. Schematic illustration for the DIW printing of a uniform NCFG/TD composite layer and an oriented active layer/polymer intermediate layer for NCFG memory devices.

2. Materials and methods

2.1 Materials

Styrene (St, purity > 99.5%) and 4-vinylpyridine (4VP, purity: 96%) were purified by basic alumina columns before use. 2,2′-Azobis(isobutyronitrile) (AIBN, purity: 99%) was recrystallized from ethanol before use. Phenyltriethoxysilane (PTS, purity: 99%), n-butylamine (BTA, purity: 99%), and 4-cyano-4-(dodecyl sulfanyl thiocarbonyl) sulfanyl pentanoic acid (CDTPA, purity: 97%) were obtained from Shanghai Aladdin Biochemical Technology Co., Ltd. HS-PS$_{12K}$ (M_n = 12 kDa, M_w/M_n = 1.09) was obtained from Polymer Source, Inc., Canada. Anhydrous N, N-dimethylformamide (DMF, purity ≥ 99%), ortho-dichlorobenzene (o-DCB, purity ≥ 99%) and dichloromethane (DCM, purity ≥ 99%) were

purchased from J&K Scientific Ltd. Deuterated chloroform ($CDCl_3$) was obtained from Ningbo Cuiying Chemical Co., Ltd. Chloroauric acid ($HAuCl_4 \cdot 4H_2O$, purity > 99%), basic alumina (Al_2O_3, 200-300 mesh), methanol (MeOH, purity: 99%), ethyl acetate (EA, purity: 99%), ethanol (EtOH, purity: 99%), 1-methyl-2-pyrrolidinone (NMP, purity: 99%) and hexane (purity: 99%) were obtained from Sinopharm Chemical Reagent Co., Ltd. Sodium citrate tribasic dihydrate (purity ≥ 99%) and PS_{288K} were obtained from Sigma–Aldrich Inc. 6,13-Bis(triisopropylsilylethynyl)pentacene (Tips-P5) were purchased from TCI (Shanghai) Development Co., Ltd. Decon 90 was obtained from Decon Laboratories Co., Ltd.

2.2 Synthesis of polystyrene (CDTPA-PS) and poly4-vinylpyridine (CDTPA-P4VP) macro-RAFT chain transfer agents

CDTPA-PS and CDTPA-P4VP were synthesized by reversible addition-fragmentation chain transfer (RAFT) polymerization [36, 37]. To obtain CDTPA-P4VP$_{4.9K}$, [4VP]:[CDTPA]:[AIBN] in a 500:5:1 mole ratio was executed. Typically, a mixture of 4VP (1 g, 9.51 mmol), CDTPA (0.0384 g, 0.0951 mmol), AIBN (0.0031 g, 0.0189 mmol) and 3 mL of DMF was added to a 20 mL Schlenk tube. Subsequently, the mixture was treated with three cycles of freeze-evacuate-thaw degassing, and pure argon gas was poured into the tube before it was sealed. Then, the tube was heated at 70 °C for 15 h. Afterward, the tube was put into an ice bath to terminate polymerization, and the obtained mixture was diluted with DMF and slowly added to a 20-fold volume of EA to precipitate CDTPA-P4VP$_{4.9K}$. Finally, CDTPA-P4VP$_{4.9K}$ was collected after two precipitation/centrifugation cycles and dried under vacuum at 40 °C overnight. The synthesis of the macro-RAFT chain transfer agents CDTPA-P4VP$_{10.2K}$ and CDTPA-PS$_{6.2K}$ was similar to the preparation of CDTPA-P4VP$_{4.9K}$, while CDTPA-P4VP$_{10.2K}$ was prepared by adjusting the molar ratio of [4VP]:[CDTPA]:[AIBN] to 1000:5:1. CDTPA-PS$_{6.2K}$ was

obtained from a mixture of [St]:[CDTPA]:[AIBN] in a 600:5:1 mole ratio polymerized at 90 °C for 22 h, then the obtained mixture was precipitated in MeOH by twice precipitation/centrifugation cycles.

2.3 Synthesis of block-copolymers (BCPs) poly4-vinylpyridine-*b*-polystyrene (CDTPA-P4VP-*b*-PS) and thiol-functionalized polymers

CDTPA-PS-*b*-P4VP was also obtained by RAFT polymerization. Briefly, a mixture of CDTPA-P4VP$_{4.9K}$ (0.2055 g, 0.0419 mmol), St (0.9514 g, 9.13 mmol), AIBN (0.0015 g, 0.0091 mmol), and 1.5 mL of DMF was added to a 20 mL Schlenk tube, then the tube was heated at 90 °C for 22 h after three freeze-evacuate-thaw degassing cycles. Then, CDTPA-PS-*b*-P4VP was precipitated in 20-fold hexane for two precipitation/centrifugation cycles and dried under vacuum at 40 °C overnight. Thiol-functionalized HS-PS-*b*-P4VP, HS-P4VP-*b*-PS, and HS-P4VP were obtained by reducing *n*-butylamine [38]. CDTPA-PS-*b*-P4VP (0.2 g, 0.0164 mmol), *n*-butylamine (121.6 μL, 1.23 mmol), and 5 mL DCM were added to a 10 mL flask. Afterward, the mixture was poured into argon gas for 2 h and stirred for 12 h at room temperature. Finally, HS-PS-*b*-P4VP was obtained after the mixture was purified with 20-fold hexane for five precipitation/centrifugation cycles.

2.4 Preparation of polymer-grafted AuNPs

AuNPs (15 nm) were synthesized following Frens' method [39]. Subsequently, the AuNPs were modified by thiol-functionalized polymers, e.g., HS-PS-*b*-P4VP, via a double-ligand exchange method. Briefly, 2 mL of concentrated Au NP aqueous solution (~ 3 mg/mL) was dropped into 30 mL of HS-PS-*b*-P4VP solution in DMF (0.8 mg/mL) via ultrasonication. Then, the mixture was sonicated for 1 h and incubated overnight. After that, the Au@PS-*b*-P4VP was concentrated by centrifugation and then redispersed in 2 mL of DMF. Then, the dispersion was dropped into 15 mL of HS-PS-*b*-P4VP solution in DMF (0.8 mg/mL) under ultrasonication for the second ligand exchange. Finally, Au@PS-

b-P4VP was purified by centrifugation in DMF 6 times to remove free HS-PS-b-P4VP chains completely, and the precipitate was dried by vacuum at 60 °C for 6 h. Afterward, Au@PS-*b*-P4VP was redispersed in NMP at a concentration of 45 mg/mL.

2.5 Fabrication of nano-crystal floating gate (NCFG) memory devices

The preparation of NCFG memory devices is shown in **Scheme 1**. First, the Au@PS-*b*-P4VP ink was printed on a wafer with 300 nm SiO_2 (blocking layer) using direct-ink-writing (Microplotter Proto, Sonoplot) with a nozzle orifice of 50 μm. The optimal printing speed and substrate temperature were 7000 μm/s and 45 °C, respectively [27]. The substrate was prewashed by sonication in water with 2 vol% Decon 90, water, and EtOH for 30 min successively. Second, 40 mg/mL Tips-P5:PS_{288K} (mass ratio: 3:1) in o-DCB was printed on the Au@PS-*b*-P4VP film by using a 250 μm nozzle orifice, and the substrate temperature was 40 °C [34]. During the DIW process, the jetting voltage was set to 1.0 V, the substrate temperature was controlled by the heating stage, and the ambient relative humidity was in the range of 30% - 70%. Finally, gold source and drain electrodes 1500 μm in width and 100 μm in length were vacuum deposited on the Tips-P5 layer using a metal mask. For control memory devices without the Au@PS-*b*-P4VP layer, Tips-P5:PS_{288K} (3:1) was printed onto a phenyltriethoxysilane (PTS)-modified SiO_2 block layer.

2.6 Characterization

The molecular weight distribution of the polymers was measured in DMF at 50 °C by Agilent 1260 GPC, where poly(methyl methacrylate) was used as the reference substance. The UV-vis absorption spectra of the polymers were obtained in DCM using Shimadzu UV 1800 spectrophotometer at 25 °C. The molecular weights (M_n) of the polymers were measured in $CDCl_3$ by Bruker AVANCE AV400 superconducting Fourier transform nuclear magnetic resonance (NMR) spectrometer. The grafting

density of the polymer-grafted AuNPs was measured via thermal gravimetric analysis (TGA, PerkinElmer, TGA 4000) under a dry flow of N_2 (30 mL/min). The measured temperature was varied from 30 °C to 700 °C (10 °C/min). The morphologies of the nanocomposite films and the structures of Tips-P5 were observed via optical microscopy (OM, Nikon, LV150N), scanning electronic microscopy (SEM, Hitachi, SU8010), and atomic force microscopy (AFM, Shimadzu, SPM9700). The crystals of Tips-P5 were characterized by X-ray diffraction (XRD, Rigaku Corporation, SmartLab-SE5KVA). The electrical performance of the NCFG memory devices was measured by a semiconductor parameter analyzer (Tektronix (China) Co., Ltd., Keithley 4200 SCS) under ambient conditions.

2.7 Calculation of the full coverage organic semiconductor thickness

The full coverage equivalent thickness is defined as $t_{eq} = t_{osc} \times \sigma_2/(\sigma_1 + \sigma_2)$ [40], where t_{osc} is the crystal height obtained from the AFM and σ_1 and σ_2 are the surface coverage percentages of the area without and with Tips-P5, respectively.

3. Results and discussion

3.1 Steady-state printing of the NCFG/TD composite layer: Effect of polymer ligands

A DIW printing technology was applied to fabricate uniform and high number-density NCFGs. It is based on a strategy of steady-state evaporation induced self-assembly of NPs. A functional colloidal ink formulation containing (PS-*b*-P4VP)-grafted AuNPs (Au@PS-*b*-P4VP) was developed (**Figure 1**). AuNPs are chosen for NCFGs due to their high work function (-5.1 eV) and chemical stability. The grafting of polymer ligands is based on improving colloidal stability and ensuring uniform dispersion of NCFGs in the TD matrix, as well as integrated printing. PS-*b*-P4VP is designed as the ligand because of the moderate solubility difference of the two blocks (solubility parameters (δ) of PS is 18.6 MPa$^{1/2}$,

and P4VP is 22.5 MPa$^{1/2}$) [41], allowing for flexible selection of both the solvent of the colloidal ink

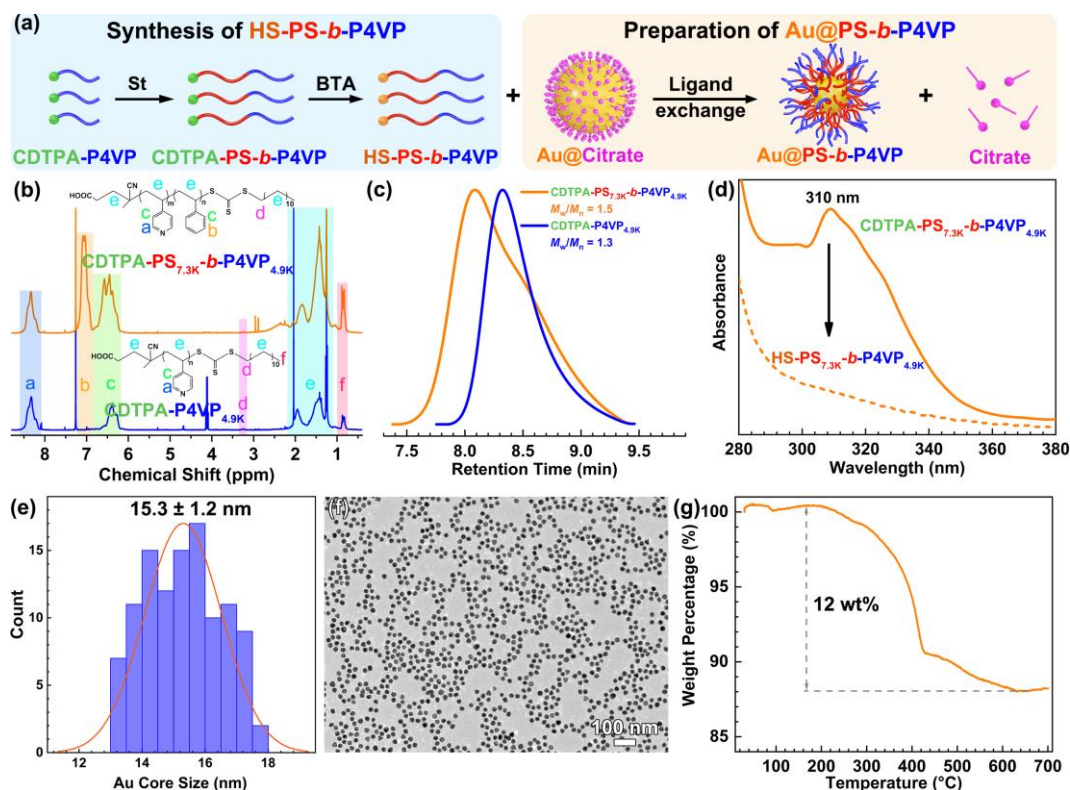and the orthogonal solvent of the semiconductor ink.

Figure 1. Synthesis and characteristics of the PS-*b*-P4VP-grafted AuNPs: (a) schematic illustration of the synthesis of HS-PS-*b*-P4VP and Au@PS-*b*-P4VP; (b) ^{1}H NMR spectra and (c) GPC traces of CDTPA-P4VP$_{4.9K}$ and CDTPA-PS$_{7.3K}$-*b*-P4VP$_{4.9K}$; (d) UV-vis absorption spectra of CDTPA-PS$_{7.3K}$-*b*-P4VP$_{4.9K}$ and HS-PS$_{7.3K}$-*b*-P4VP$_{4.9K}$; (e) statistical histogram of the Au core diameter (over 100 NPs were countered); (f) TEM image and (g) TGA curve of Au@PS$_{7.3K}$-*b*-P4VP$_{4.9K}$ NPs.

The CDTPA-PS-*b*-P4VP was synthesized by reversible addition-fragmentation chain transfer (RAFT) polymerization with 4-cyano-4-(dodecyl sulfanyl thiocarbonyl) sulfanyl pentanoic acid (CDTPA) as the chain-transfer agent (**Figure 1a**) [36, 37]. The number-average molecular weight (M_n) and molecular weight distribution (M_w/M_n) of CDTPA-PS-*b*-P4VP were measured via ^{1}H NMR and GPC (**Figure 1b, c**), respectively. The trithiocarbonate groups of CDTPA-PS-*b*-P4VP were reduced by *n*-butylamine (BTA) to generate thiol (HS-) groups. The disappearance of the absorption peak at 310 nm indicates that aminolysis was complete and HS-PS-*b*-P4VP was obtained (**Figure 1d**) [38].

10

After that, uniform Au@PS-*b*-P4VP NPs with the Au core of 15.3 ± 1.2 nm (**Figure 1e**) were prepared by a double-ligand exchange method with the HS-PS-*b*-P4VP via forming Au-S bond. The TEM image indicates that the Au@PS-*b*-P4VP NPs are uniform and monodispersed (**Figure 1f**). TGA curve shows that the grafting weight percentage of HS-PS-*b*-P4VP on the surface of AuNPs is 12 wt% (**Figure 1g**).
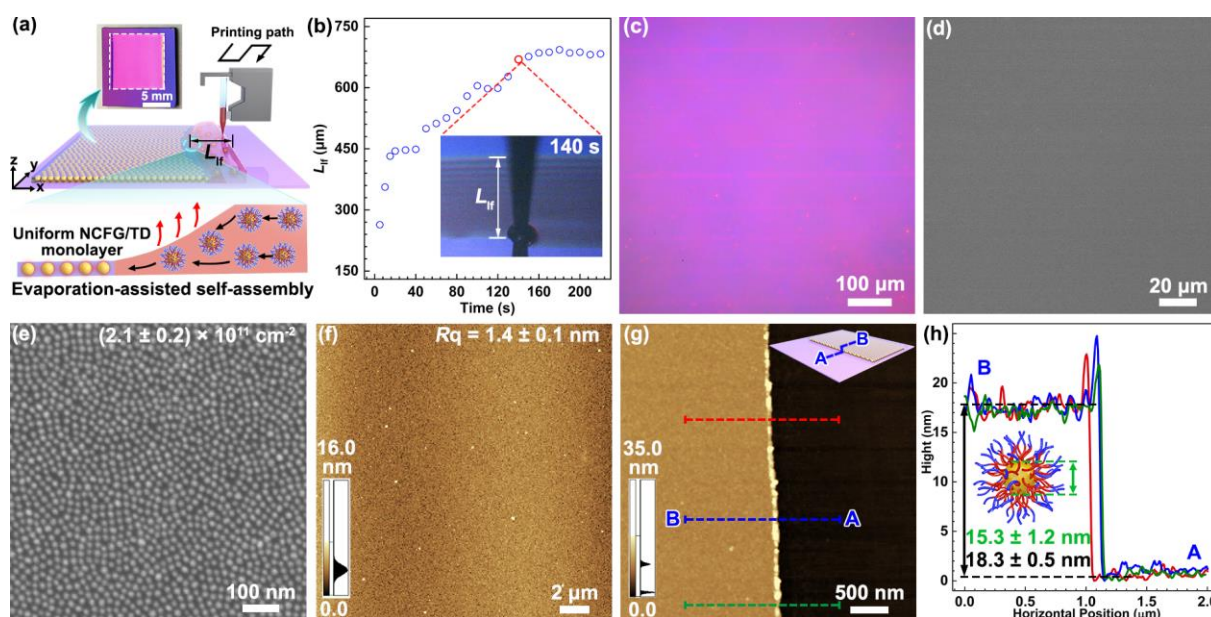

Figure 2. (a) Schematic illustration of the evaporation-assisted self-assembly of Au@PS-*b*-P4VP by steady-state printing with DIW, and the insert is a photograph of a printed film; (b) plot of the length of the liquid film (L_{lf}) as a function of time during printing, and the insert is a snapshot of L_{lf} at 140 s; (c) OM and (d) low-resolution SEM images of the nanocomposite film; (e) high-resolution SEM image of the nanocomposite film, in which the number density of AuNPs was counted from three regions; (f) AFM image of the nanocomposite film, in which the R_q was measured three times; (g) AFM image and (h) corresponding height profile.

A high boiling point and super wettable solvent, 1-methyl-2-pyrrolidinone (NMP, 23.0 MPa$^{1/2}$) [42], is used as the solvent for the colloidal ink containing Au@PS-*b*-P4VP NPs. As shown in **Figure 2** and **Figure S1**, the colloidal ink was printed onto the substrate from the nozzle, and a liquid film was obtained via continuous raster scanning printing mode. The length of the liquid film (L_{lf}) increased with time from 0 to 140 s, then reached a constant value after 140 s, indicating that solvent evaporation

and ink delivery reached a steady-state (**Figure 2b** and **Figure S2b**). Under the solvent evaporation, Au@PS-*b*-P4VP NPs at the triple-phase contact line (TPCL) self-assemble into a nanocomposite film at a suitable particle concentration, solvent evaporation rate and printing speed [26, 27, 43, 44]. OM, SEM, and AFM images (**Figure 2c-h**) show that the nanocomposite film consists of a uniform monolayer of Au@PS-*b*-P4VP and has a low surface roughness (the root mean square roughness (R_q) is 1.4 ± 0.1 nm at an area of 20×20 μm^2; **Figure 2f**). According to the high-resolution SEM image (**Figure 2e**), the average number density of the Au NPs is up to 2.1×10^{11} cm^{-2}.

The composition and grafting density of polymer ligands determine the uniformity of the NCFG/TD composite layer and the number density of NCFGs. In comparison with HS-PS-*b*-P4VP, three other ligands with similar chain lengths were designed, namely, HS-P4VP-*b*-PS, HS-P4VP, and HS-PS (**Figure S2** and **Table S1**). For Au@P4VP-*b*-PS and Au@P4VP, nanocomposite films with a relatively higher number density of Au NCFGs ((2.8 ± 0.1) $\times 10^{11}$ cm^{-2} for the former and (2.7 ± 0.3) $\times 10^{11}$ cm^{-2} for the latter) were obtained(**Figure S3**). The higher number density of Au NCFGs is a result of the low grafting density of the polymer ligands, as confirmed by TGA: the weight percentages (wt%) of HS-P4VP-*b*-PS and HS-P4VP were 5 wt% and 4 wt%, respectively (**Figure S4a**). The low grafting density can be attributed to the multiple linking sites generated via coordination between the Au core and the pyridine group of P4VP (**Figure S4b**) [45, 46]. For HS-PS-*b*-P4VP, the insertion of the PS block enables physical separation between Au and P4VP; therefore, the grafting density of HS-PS-*b*-P4VP increased to 12 wt% (**Figure 1g**). For the Au@PS NPs, a higher grafting density (22 wt%) resulted in a lower number density of Au NCFGs ((1.1 ± 0.5) $\times 10^{11}$ cm^{-2}) in the nanocomposite film (**Figure S4**). Although short-range ordered structures formed, the nanocomposite film of Au@PS contained many blank regions (**Figure S3g-i**) and was not suitable for the NCFG/TD layer. Although

its number density is lower than that of either the Au@P4VP-*b*-PS or Au@P4VP nanocomposite films, the Au@PS-*b*-P4VP nanocomposite film is selected as the NCFG/TD layer for the following reasons: 1) it has the lowest roughness, which facilitates the formation of a high-quality active layer and fast injection of carriers; and 2) it has a relatively large interparticle distance (6.2 ± 1.2 nm, data was measured from more than 100 interparticle distance) and a relatively thick TD layer (~3.1 nm) for better retention.

3.2 Printing of a high-quality active layer on the Au@PS-*b*-P4VP composite layer
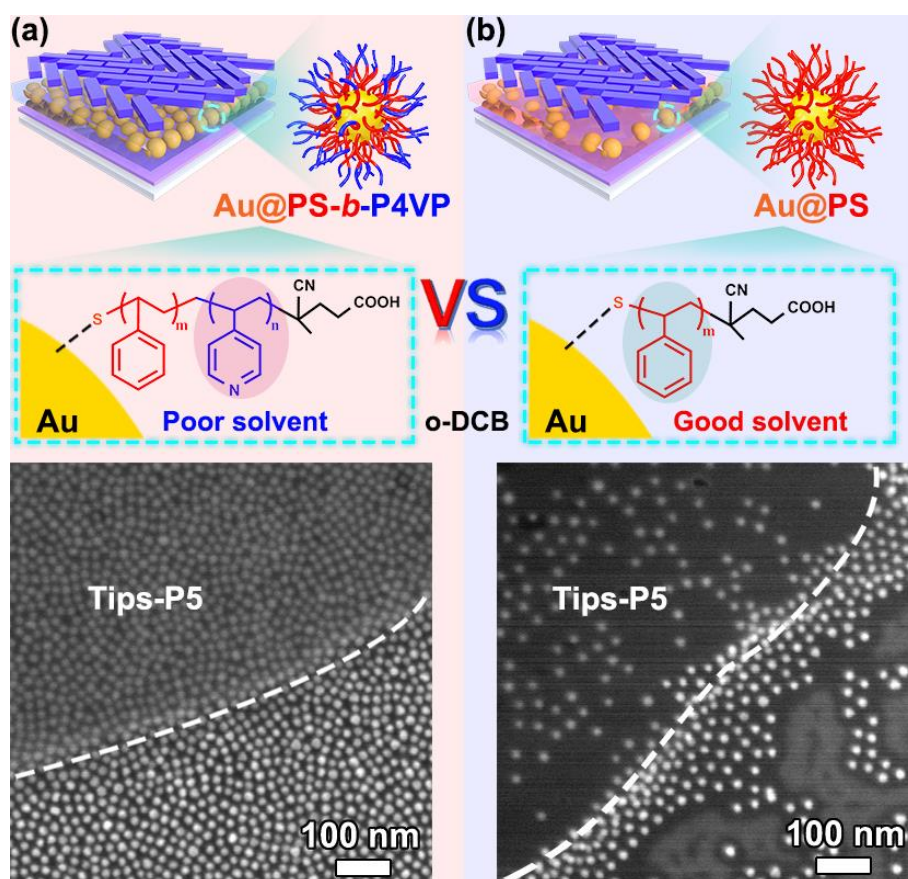
Figure 3. Schematic illustration and SEM images of Tips-P5 printed on (a) Au@PS-*b*-P4VP and (b) Au@PS nanocomposite films.

Another advantage of the PS-*b*-P4VP ligand is that its P4VP block plays a vital role in overcoming the interlayer solvent erosion problem during the printing of the upper active layer of semiconductor (Tips-P5) crystals. The solubility of Tips-P5 is similar to that of PS ($\delta_{\text{Tips-P5}}$ is 18-19 MPa$^{1/2}$); therefore,

a good solvent for Tips-P5 but poor for P4VP can be used as an orthogonal solvent. We found that

ortho-dichlorobenzene (o-DCB) can meet these requirements (**Figure S5**) [41, 47]. From the SEM

image, we can see that the structure of the Au@PS-*b*-P4VP nanocomposite film was well maintained,

which indicates that the interlayer solvent erosion problem was overcome during the printing of the

Tips-P5 active layer (**Figure 3a**). In comparison, the nanocomposite film of Au@PS was destroyed

after printing the active layer (**Figure 3b**). This confirmed that the P4VP chain plays a critical role in

overcoming erosion.
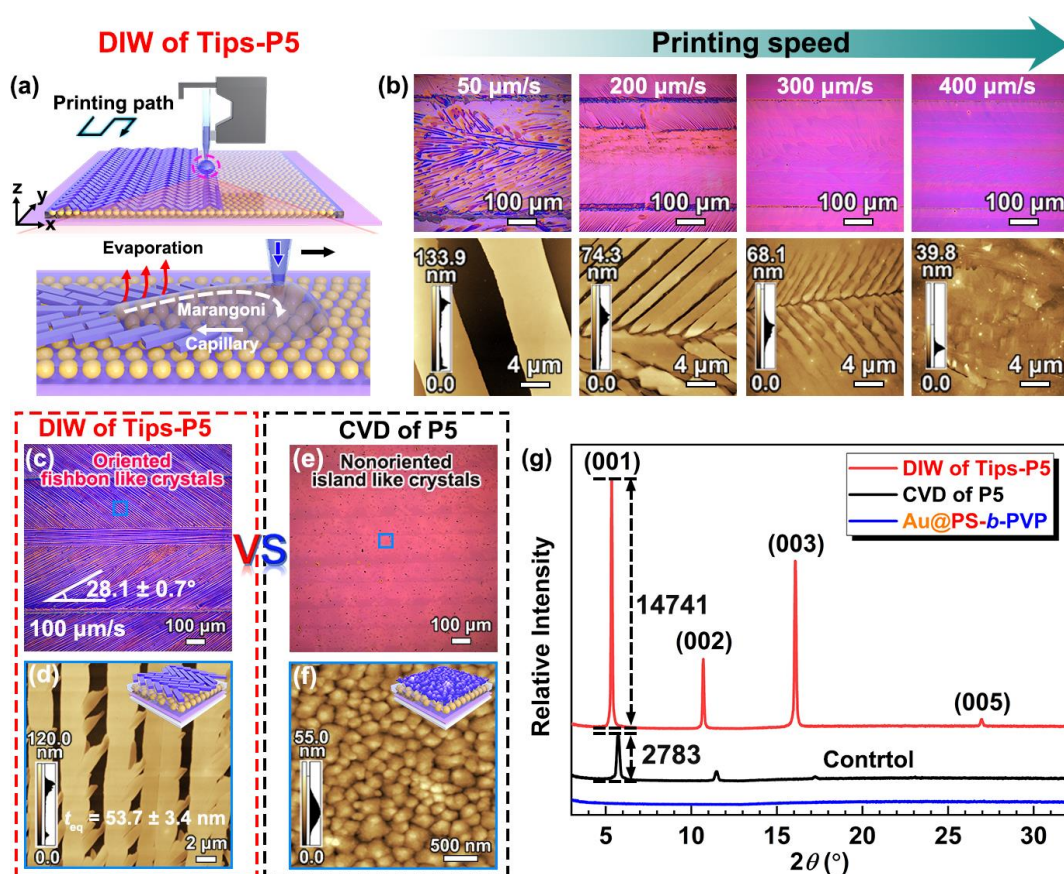
Figure 4. (a) Scheme of the fluid shearing induced orientation of Tips-P5 crystals by DIW; (b) OM
(the upper row) and AFM (the bottom row) images show the morphology change of Tips-P5 crystals
with increased printing speed; (c, d) OM and AFM images of oriented Tips-P5 crystals, the included
angle value in (c) and the full coverage equivalent thickness (t_{eq}) in (d) were measured from nine
crystals; (e, f) OM and AFM images of non-oriented pentacene (P5) crystals prepared by CVD; (g)
XRD curves of semiconductor crystals.

14

Similar to 3D meniscus-guided coating [48, 49], DIW enables the tunable orientation of the semiconductor crystals due to the fluid shearing effect. During printing, the crystals nucleate close to the triple-phase contact line (TPCL) as the solvent evaporates, and the solute concentration gradient creates a Marangoni flow that drives solute migration from TPCL to the solution. Then, the crystals grow along the printing direction when the solvent evaporation rate matches the crystallization rate of the semiconductor (**Figure 4a**). Hence, with DIW printing technology, highly crystalline and oriented semiconductor crystals on a polymer dielectric layer were obtained by adjusting the printing speed when the substrate temperature was fixed [34]. As shown in **Figure 4b**, fast solvent evaporation induces the formation of irregular and ribbon crystals at a low printing speed (50 μm/s), while sheet-like crystals form due to viscous drag at high printing speeds (200 to 400 μm/s). At a medium printing speed (100 μm/s), the solvent evaporation rate matched the crystallization rate of Tips-P5; therefore, well-oriented and fishbone-like crystals of Tips-P5 were obtained (**Figure 4c, d**), in which the included angle of the crystals with the central axis is $28.1 \pm 0.7°$. The AFM image shows parallel and ribbon crystal patterns (**Figure 4d**), and its full coverage equivalent thickness (t_{eq}) is 53.7 ± 3.4 nm. This result is consistent with the printing of Tips-P5 onto silica substrates reported in the literature [31, 33, 50]. The crystal quality of the oriented Tips-P5 is significantly better than that of the pentacene (P5) prepared by chemical vapor deposition (CVD). For the oriented Tips-P5 crystals, strong and sharp interlayer Bragg reflections up to fourth-order diffractions were observed in the XRD curves (**Figure 4g**). The d-spacing calculated at $2\theta \approx 5.35°$ is 1.65 nm, which is close to the (001) d-spacing in the single crystal of Tips-P5 (1.68 nm) [21, 33]. In a control experiment, a non-oriented active layer with a similar thickness (t_{eq}, 50 nm) was obtained by CVD of P5; this layer contains small-sized and island-like P5 crystals (**Figure 4e, f**). Bragg reflections up to third-order diffractions were observed in the

XRD curves of P5 (**Figure 4g**), and the peak intensity was 1/5 that of the printed Tips-P5 due to non-orientation, small grains, and many grain boundaries.

The electrical performance of the oriented semiconductor crystals is better than that of non-oriented island-like semiconductor crystals prepared by CVD. Field-effect transistor-based NCFG memory devices were fabricated after the deposition of source and drain gold electrodes onto the active layer. The electrical performance of the devices with the printed Au@PS-*b*-P4VP NCFG/TD composite layer and oriented Tips-P5 active layer is shown in **Figure S6a, b**. The transfer characteristics were tested at V_{DS} = -30 V, a threshold voltage (V_{th}) of -(4.5 ± 0.9) V, a mobility (μ) of (2.8 ± 2.7) × 10^{-3} cm^2 V^{-1} s^{-1}, and an on/off current ratio ($I_{on/off}$) of (1.7 ± 1.0) × 10^2 (**Figure S6a**). The transfer and output characteristics of the device indicate typical p-type field-effect behavior (**Figure S6a, b**). In contrast, the device with the non-oriented P5 active layer exhibited no field effect (**Figure S6d, e**), even though the NCFG/TD layer was fully covered by P5 crystals (**Figure 4f**). The lack of a field effect for the device with CVD of P5 could be attributed to the pyridine groups of P4VP block on the surface of the NCFG/TD composite layer, which serves as interface traps that hinder carrier transport by deep-trapping or scattering carriers, similar to the hydroxyl (-OH) groups of SiO$_2$ [51, 52]. Compared with P5 crystals formed by CVD, large-sized and oriented Tips-P5 crystals formed by DIW have fewer grain boundaries and high crystallinity, which facilitate carrier transport even though interfacial traps exist (**Figure S6c, f**) [53, 54]. Another control device with high crystallinity yet randomly oriented Tips-P5 crystals (**Figure S7a, b**) exhibited a field effect (**Figure S7c, d**) but with a lower μ (7.7 × 10^{-4} cm^2 V^{-1} s^{-1}) and $I_{on/off}$ (1.0 × 10^2), and a higher V_{th} (-7.1 V). These results indicate that high crystallinity and orientation of the active layer play critical roles in preventing charge leakage and improving the performance of the device.

3.3 Improving the performance of NCFG memory devices by introducing a polymer intermediate layer

The above device exhibits bipolar storage properties and has a large memory window (ΔV_{th} = 47 V) (**Figure S8**). However, due to the interfacial traps induced by the polar P4VP of the NCFG/TD composite layer, the device has a relatively high V_{th} (-(4.5 ± 0.9) V), low μ ((2.8 ± 2.7) × 10^{-3} cm^2 V^{-1} s^{-1}) and $I_{on/off}$ ((1.7 ± 1.0) × 10^2). To address this problem, we propose inserting a nonpolar PS intermediate layer between the TD/Tips-P5 interface. Introducing a polystyrene (PS) intermediate layer not only acts as a tunneling layer to reduce interfacial traps but also serves as an electret for charge trapping. PS was added to the Tips-P5 ink. Because of the incompatibility among the PS additive, Tips-P5, and the P4VP block, integrated printing of the oriented active layer and the PS layer was realized via vertical phase separation between the PS and Tips-P5 (**Figure 5a**) [55]. **Figure 5b** shows the obvious phase separation of Tips-P5 and PS (mass ratio: 3:1) results in a 49.5 ± 2.7 nm Tips-P5 active layer and a 21.3 ± 0.7 nm PS intermediate layer. In addition, we found that the surface coverage of Tips-P5 increased with the relative content of PS (**Figure S9**). Moreover, the XRD curves indicate that the addition of PS has no noticeable impact on the crystal structure of Tips-P5 (**Figure S10**).

The electrical performance of the optimized NCFG memory devices is significantly improved compared to that of the NCFG memory device without the PS intermediate layer (**Control-1**). For example, when the V_{th} significantly decreased by 42% (-(2.6 ± 1.6) V), the μ significantly increased by 15 times (μ, (4.3 ±3.4) × 10^{-2} cm^2 V^{-1} s^{-1}), and the $I_{on/off}$ ratio increased by 10 times ((1.7 ± 0.5) × 10^3) (**Figure 5d, e**). The excellent uniformity of the device performance was proven (**Figure S11**). Moreover, the ΔV_{th} used for hole trapping and electron trapping increased by 10 V and 9 V,

respectively, and the total ΔV_{th} width increased to 66 V with a corresponding charge trapping density (Δn) [19] of 4.4×10^{12} cm^{-2} (**Figure 5f**). In addition, the time for light erasure was reduced to 3 s, which indicates that the device has a quicker erasure speed. For the erasing process by applying -40 V (cyan curve in **Figure 5f**), the slight decrease in $I_{on/off}$ could be attributed to the cumulative defects on the gate oxide [56, 57]. Furthermore, the effect of the Tips-P5:PS ratio on performance was studied. The μ and $I_{on/off}$ increased as the Tips-P5:PS ratio decreased from 5:1 to 3:1 to 1:1 (**Figure S12d, e**) because higher surface coverage of PS led to fewer interfacial traps. However, the ΔV_{th} decreased because charge injection into the NCFG layer was hindered by the increasing thickness of the PS layer (**Figure S12f**). Therefore, an intermediate ratio of 3:1 (Tips-P5:PS) is preferred for accessing NCFG memory devices with a higher mobility and $I_{on/off}$ ratio, and a larger memory window.
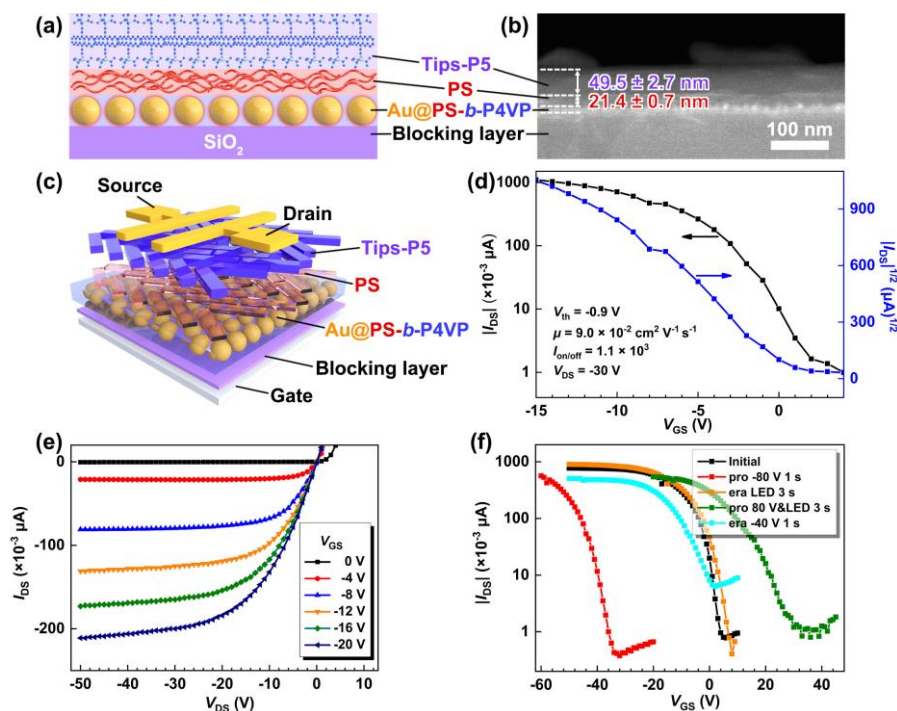
Figure 5. (a) Illustration and (b) SEM image of the cross-sectional of printed Au@PS-*b*-P4VP/PS/Tips-P5 layers, in which the thickness of Tips-P5 and PS layers were measured from three different positions; (c) schematic illustration of an optimized NCFG memory device; (d) transfer and (e) output characteristics of a device, respectively; (f) programming and erasing characteristics of a device.

Table 1. The electrical performance of NCFG memory devices (Control-1), PS electret devices (Control-2), and optimized NCFG memory devices with a PS intermediate layer.

Memory Devices	V_{th} (V)	$I_{on/off}$	Average ΔV_{th} (V)	WRER endurances[a]		Retention[b]	
				Hole-trapping	Electron-trapping	Hole-trapping	Electron-trapping
Control-1	-4.5 ± 0.9	$(1.7 \pm 1.0) \times 10^2$	47	/	/	/	/
Control-2	-5.2 ± 2.0	$(1.9 \pm 1.1) \times 10^3$	42	12.2	2.6	0	0
optimized device	-2.6 ± 1.6	$(1.7 \pm 0.5) \times 10^3$	66	1.3×10^3	3.2×10^2	4.9×10^3	7.0×10^2

[a]Data measured by $I_{on/off}$ after 110 WRER cycles; [b]data measured by $I_{on/off}$ after 10^4 seconds of retention; the V_{th}, $I_{on/off}$ and ΔV_{th} were obtained from three NCFG devices.

We further demonstrated that the Au@PS-*b*-P4VP nanocomposite layer is also critical for the device. Another control device (**Control-2**), which contains the PS intermediate layer but not the Au@PS-*b*-P4VP composite layer (**Figure S13a-c**), has a much lower μ (($6.5 \pm 5.5) \times 10^{-3}$ cm^2 V^{-1} s^{-1}), a comparable $I_{on/off}$ (($1.9 \pm 1.1) \times 10^3$), and a much higher V_{th} (-(5.2 ± 2.0) V). In addition, the **Control-2** device has a smaller ΔV_{th} (42 V) (**Figure S13d**). This result indicated that both the Au@PS-*b*-P4VP-based NCFG/TD composite layer and the PS intermediate layer play significant roles in improving the performance of the memory device (**Table 1**).

The possible memory mechanism of the optimized NCFG memory device is described in **Figure 6**. The lowest unoccupied molecular orbital (LUMO) and highest occupied molecular orbital (HOMO) levels of that are used are obtained from the literature (**Table S2**) [58-61]. When a negative gate bias is applied in the dark, in addition to the migration or diffusion of charge, most holes are injected from Tips-P5 to the Au NCFGs and polymer. Due to the small energy barrier between the HOMO level of Tips-P5 (-5.20 eV) and the work function of Au NCFGs (-5.1 eV) [60], holes are more readily trapped by Au NCFGs than by the polymer. The trapped holes decrease the concentration of holes in the

conductive channel and form an internal electric field (E_{in}), resulting in a negative shift in V_{th}. The PS intermediate layer can be divided into two parts: a superficial TD layer near the active layer and a charge-trapped layer at the bottom [62]. The holes will be transferred into the PS layer by direct tunneling and Fowler-Nordheim (F-N) tunneling. In contrast, the holes will be injected into the Au NCFGs by F-N tunneling through the TD layer because of the high programming voltage used (**Figure 6a**). When the optimized NCFG memory devices are irradiated by white light, many photogenerated carriers will be formed and then divided into photogenerated electrons and holes under E_{in}. Subsequently, the photogenerated holes shift to the conductive channel, reducing the electron-injected energy barrier.
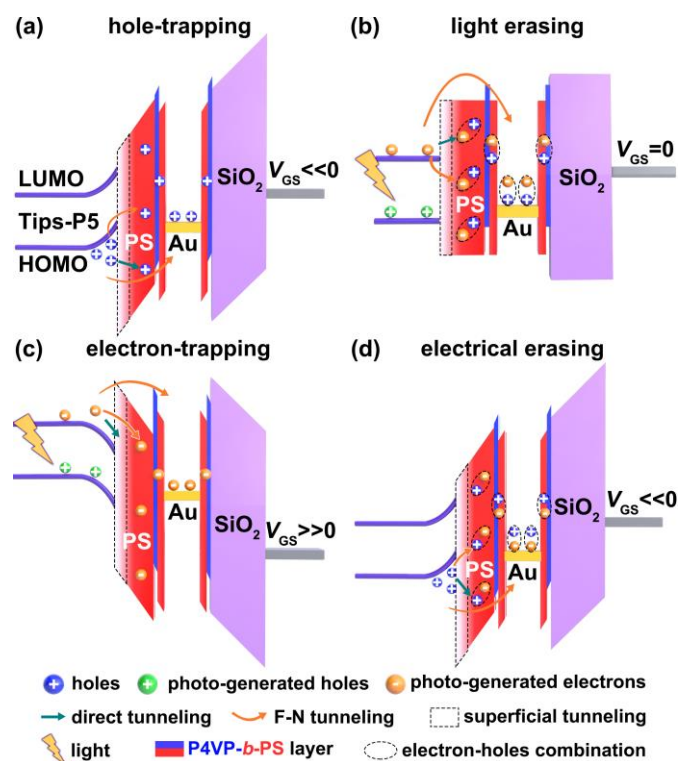
Figure 6. Schematic illustration of the mechanism and energy band diagrams of optimized NCFG memory devices: (a) programming with a negative gate bias in the dark; (b) erasing by white light; (c) programming with a positive gate bias under white light illumination; (d) erasing with a negative gate bias in the dark.

High-energy photogenerated electrons were trapped in the polymer and Au NCFGs and combined

with formerly trapped holes, it induces a positive shift in V_{th} and recovery to the initial state (**Figure 6b**) [63]. The electron trapping process is similar to the light erasing process, and photogenerated electrons and holes are effectively separated under a positive V_{GS}. For Tips-P5, only high-energy photogenerated electrons are injected into the polymer and Au NCFGs; because of the small LUMO energy barrier between Tips-P5 (-3.55 eV) and PS (-2.5 eV) [61], electrons are more easily captured by PS than by Au NCFGs. Then, the residual holes in the Tips-P5 channel led to a positive shift in V_{th} (**Figure 6c**). After a negative gate bias is applied, the trapped electrons will combine with the holes, resulting in the shifting of the transfer curve to the initial state (**Figure 6d**).

In addition to having a large storage window and fast erasing speed, the optimized NCFG memory devices have good reliability and stability. As shown in **Figure 7a, b**, the on-state and off-state are well maintained for both the hole-trapping and electron-trapping modes after 110 write-read-erase-read (WRER) cycles. The $I_{on/off}$ is kept at 1.3×10^3 for the hole-trapping mode and 3.2×10^2 for the electron-trapping mode after 110 WRER cycles. Furthermore, the memory devices exhibit steady characteristics of on-state and off-state after a 10^4 s retention. The $I_{on/off}$ ratio is maintained at 4.9×10^3 for hole-trapping mode and 7.0×10^2 for electron-trapping mode after 10^4 s (**Figure 7c, d**). Additionally, the on-state and off-state of hole-trapping and electron-trapping modes remains stable after 10 years, which is determined by extending the fit curve (**Figure S14**). For comparison, both the endurance and retention of the **Control-2** device dramatically decrease (**Figure S15a-d**). The apparent enhancement in $I_{on/off}$ indicates that the discrete Au NCFGs significantly enhances memory stability.
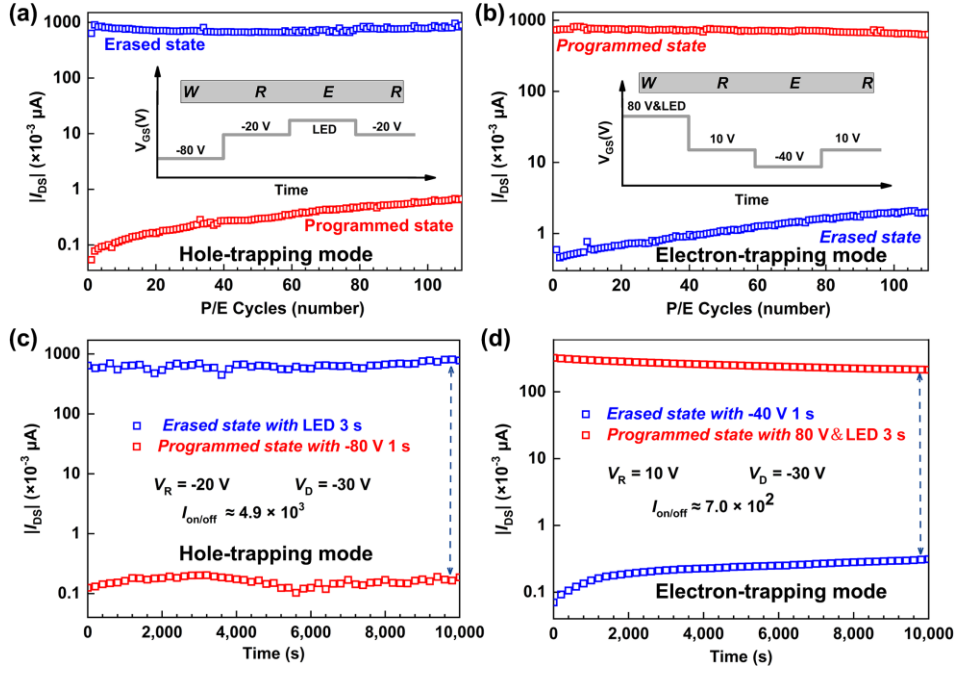
Figure 7. (a, b) Write-read-erase-read (WRER) endurance characteristics of an optimized NCFG memory device; (c, d) retention characteristics of an optimized NCFG memory device.

Compared with previous related reports (**Table S3**) [19, 20, 27, 64], this work provides a method for improving the performance of NCFG memory devices by fully automatic DIW printing of functional layers, especially by decreasing the threshold voltage, enlarging the storage capacity, and improving the write-read-erase-read (WRER) endurance and long-term charge retention for both hole-trapping and electron-trapping modes.

4. Conclusion

In summary, we have achieved a high-performance nano-crystal floating gate (NCFG) memory device with full-printed functional layers. The design of polystyrene-*block*-poly(4-vinyl pyridine) (PS-*b*-P4VP) ligand for Au NCFGs not only ensures the formation of a uniform NCFG/tunneling dielectric (TD) composite layer, but also enables the printing of an high quality active layer on the top of the TD layer without interlayer solvent erosion. The active layer of oriented semiconductor crystals with high crystallinity was obtained via fluid shearing. Furthermore, a PS intermediate layer is inserted between

22

the TD/semiconductor interface to reduce interfacial traps and serve as an electret for charge trapping. As a result, the optimized NCFG memory devices demonstrate high charge storage capability (66 V), stable write-read-erase-read (WRER) endurance (> 100 cycles), long-term data retention (> 10 years), and notably, low threshold voltage (< 3 V, which is better than that of other reported NCFG memory devices). This methodology could be extended for the printing of other functional coatings and multi-layer thin-film devices.

ASSOCIATED CONTENT

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CRediT authorship contribution statement

Xi Mao and **Yonghao Yang** conceived the experiments, analyzed the data, and wrote the paper. **Haowen Qian** and **Wenqi Zhao** characterized the electrical performance of NFGM devices. **Wang Li** performed the the electron-microscopy characterization. **Shuai Deng** and **Shaohong Jin** provided suggestions for study design. **Liangzhu Jiang** and **Changxu Liu** proofread the manuscript. **Wen Li**, **Mingdong Yi,** and **Jintao Zhu** discussed the results and revised the paper. **Lisong Yang** revised the paper. **Renhua Deng** designed the study, discussed the results, and revised the paper.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Appendix A. Supplementary data

The following is the Supplementary material related to this article.

Data availability

Data will be made available on request.

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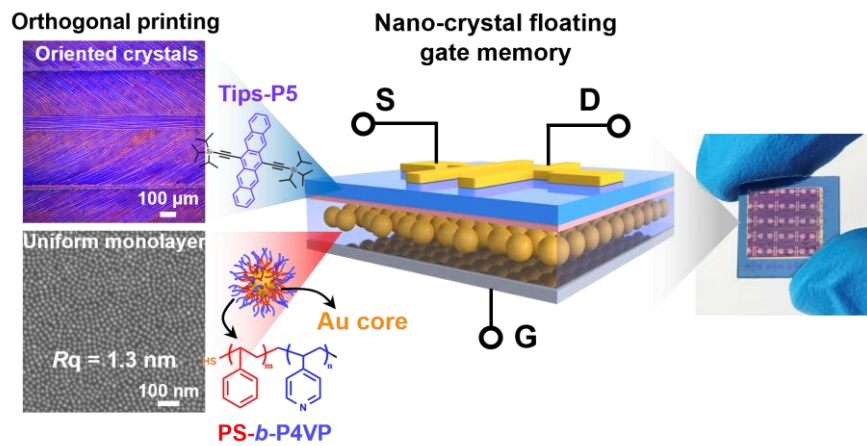
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Graphical abstract:

Orthogonal printing

Oriented crystals

100 μm

Tips-P5

Uniform monolayer

Rq = 1.3 nm

100 nm

Au core

PS-b-P4VP

Nano-crystal floating gate memory

S   D

G

Supporting Information

Orthogonal Printing of Uniform Nanocomposite Monolayer and Oriented Organic Semiconductor Crystals for High-Performance Nano-Crystal Floating Gate Memory

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Figure S1. (a) Scheme of steady-state solvent evaporation-assisted self-assembly; (b) snapshots illustrate the variation in the length of the liquid film (L_{lf}) at different times.
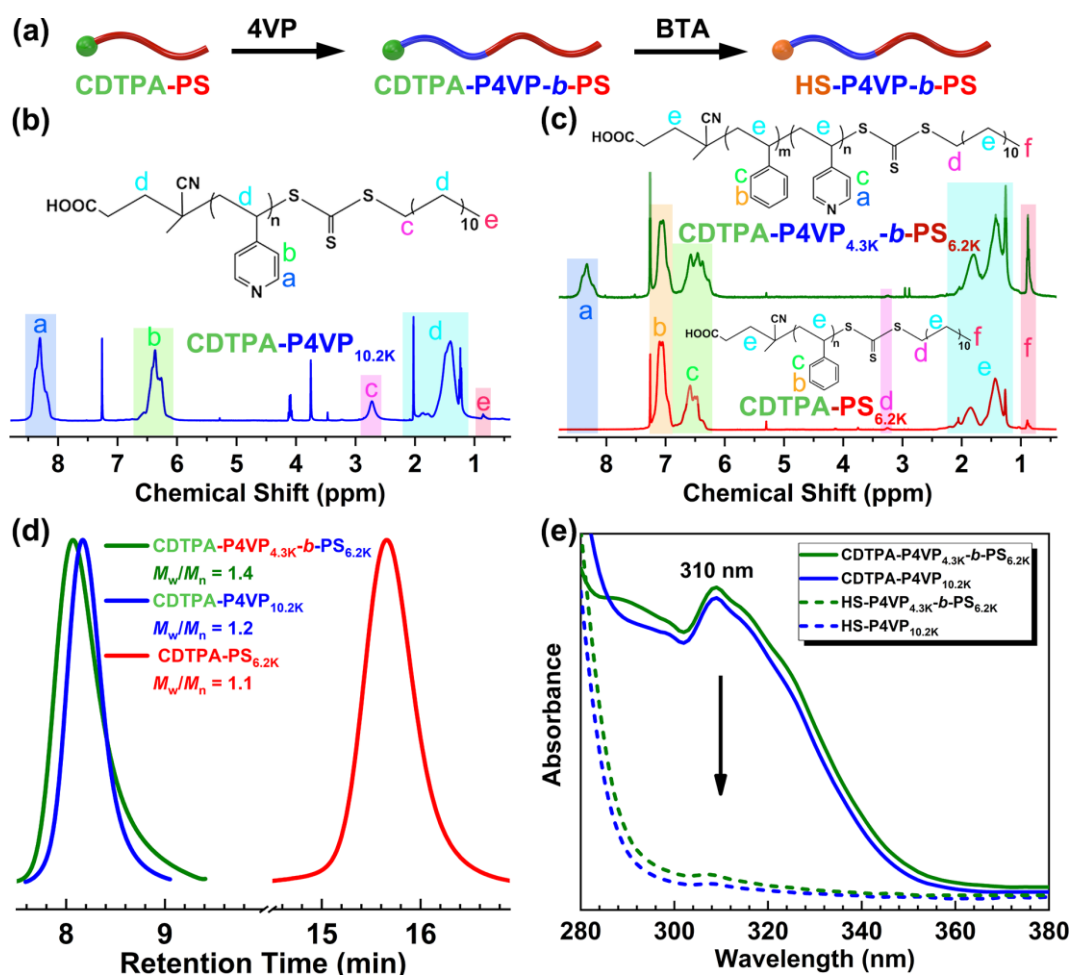
Figure S2. Synthesis of thiol terminated polymers: (a) schematic illustration of the synthesis of HS-P4VP-*b*-PS; (b, c) ^{1}H NMR spectra and (d) GPC traces of CDTPA-P4VP, CDTPA-PS and CDTPA-P4VP-*b*-PS; (e) UV-vis absorption spectra of CDTPA-P4VP and CDTPA-P4VP-*b*-PS before and after thiol functionalization.

Table S1. Molecular weight and molecular weight distribution of HS-terminated polymers used in this study.

Polymers	M_n of PS (kg/mol)[a]	M_n of P4VP (kg/mol)[a]	M_n of PS-b-P4VP (kg/mol)[a]	M_w/M_n[b]
HS-PS$_{7.3K}$-b-P4VP$_{4.9K}$	7.3	4.9	12.2	1.5
HS-P4VP$_{4.3K}$-b-PS$_{6.2K}$	6.2	4.3	10.6	1.4
HS-P4VP$_{10.2K}$	/	10.2	/	1.2
HS-PS$_{12K}$	12.0	/	/	1.1

[a]Data obtained by ^{1}H NMR; [b]data collected by GPC.
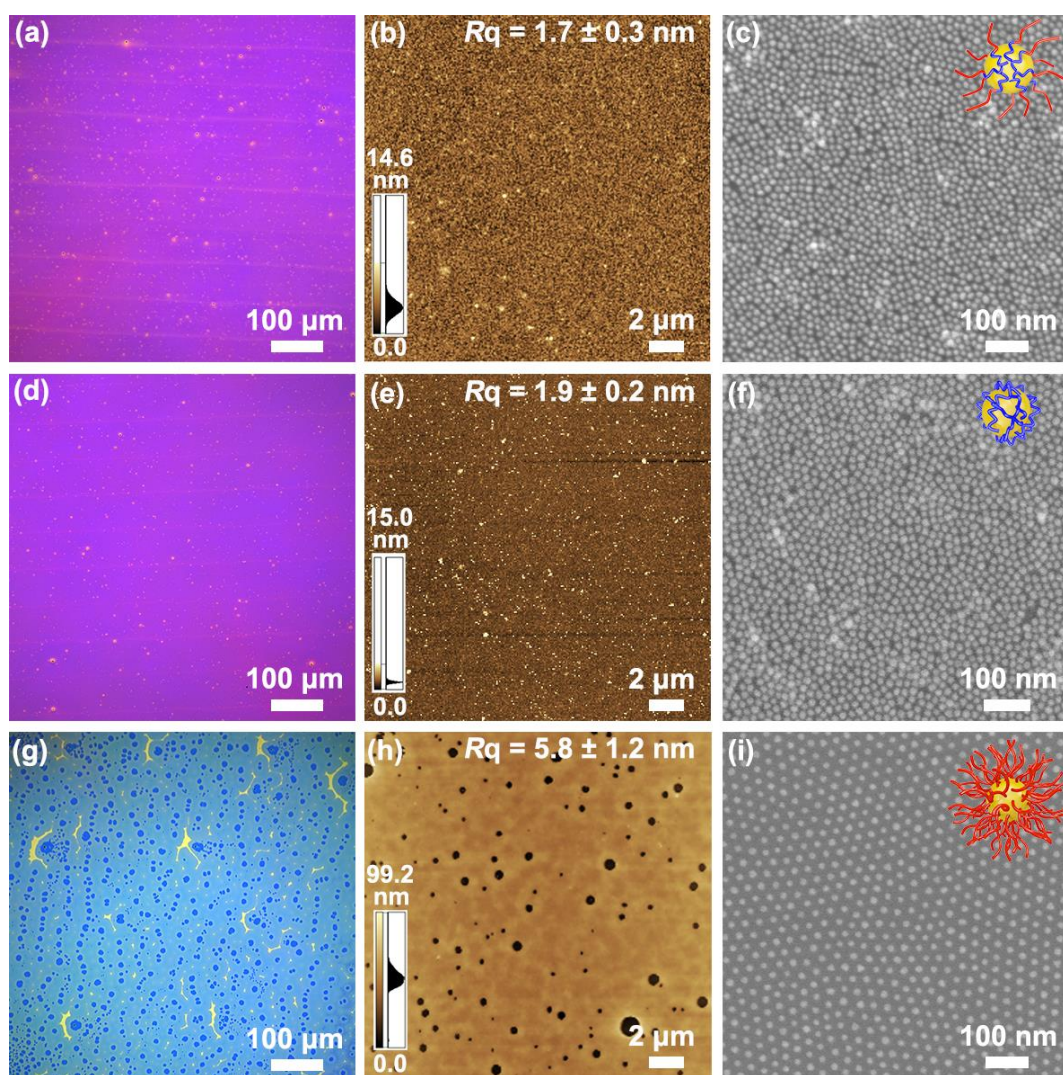
Figure S3. OM (the left column), AFM (the middle column), and SEM (the right column) images of nanocomposite films with different NPs: (a-c) Au@P4VP-*b*-PS; (d-f) Au@P4VP; (g-i) Au@PS. The R_q were measured for three times.
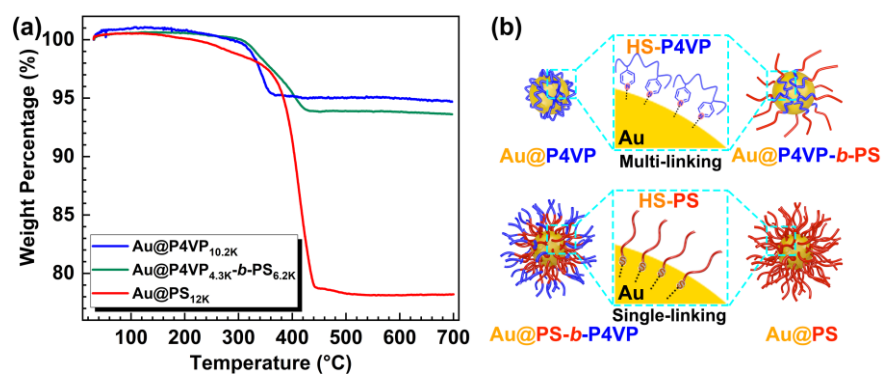
Figure S4. (a) Thermal gravimetric analysis (TGA) curves and (b) schematic illustration of different polymer ligands grafted AuNPs.
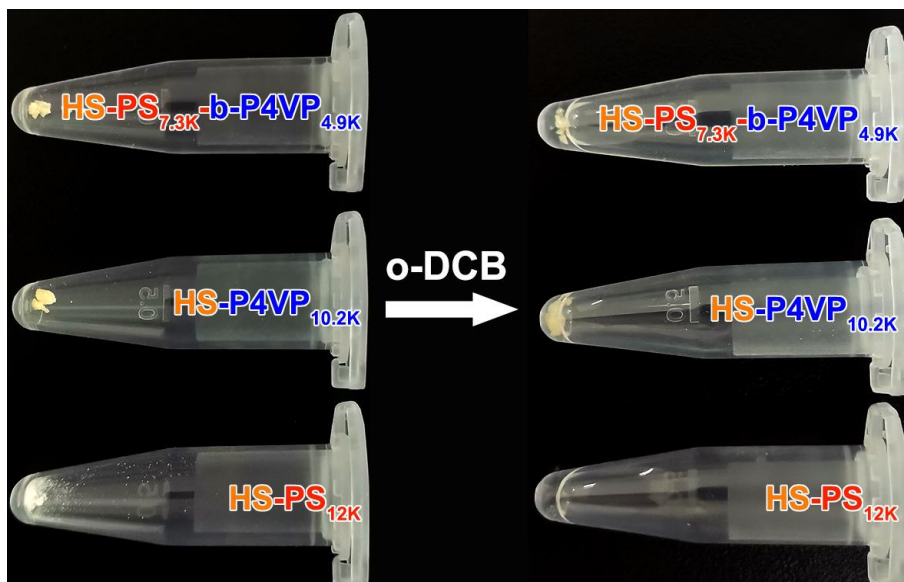
Figure S5. Solubility of polymer ligands in o-DCB: HS-PS$_{12K}$ was rapidly dissolved in o-DCB, while HS-PS$_{7.3K}$-b-P4VP$_{4.9K}$ and HS-P4VP$_{10.2K}$ were hardly dissolved by o-DCB.
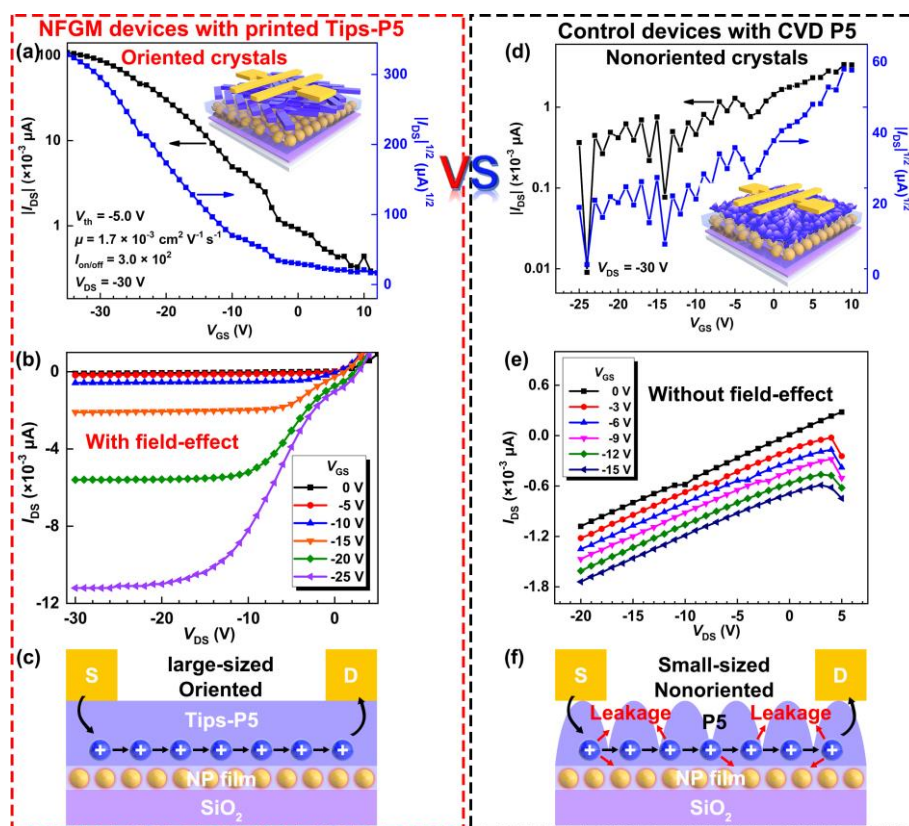
Figure S6. (a) Transfer and (b) output characteristics of a NCFG memory device with a printed Tips-P5 active layer, respectively; (d) transfer and (e) output characteristics of a control memory device, in which their pentancene (P5) active layer was prepared by chemical vapor depostion (CVD); (c, f) schematic illustration of the transport and leakage of charge in the NCFG memory device and the control device, respectively.
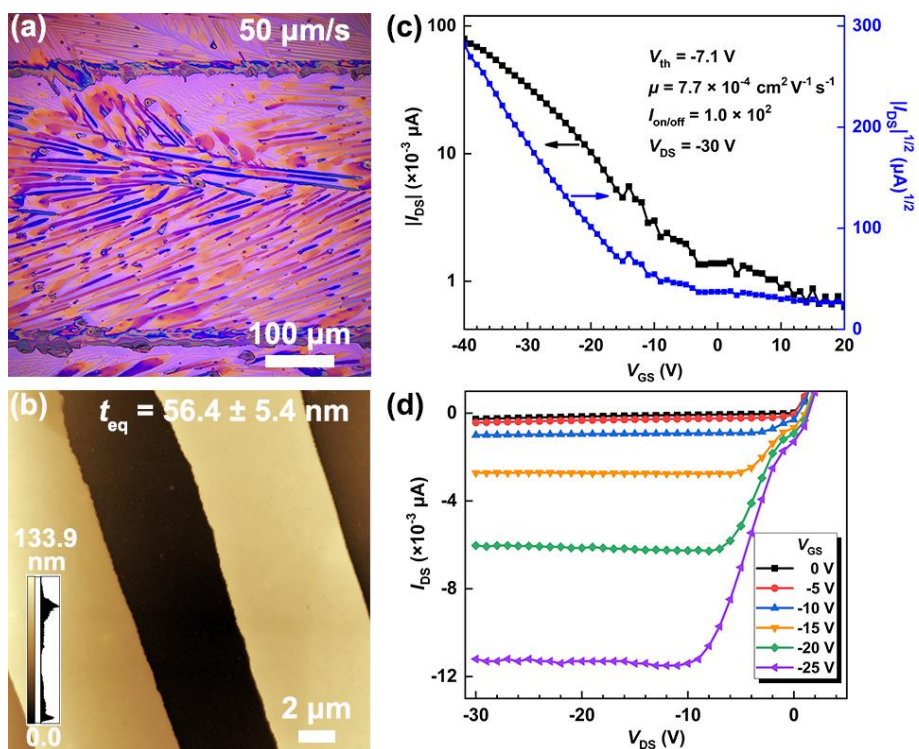
Figure S7. (a) OM and (b) AFM images of printed Tips-P5 with randomly oriented crystals, the crystal thickness (t_{eq}) data was measured from nine crystals; (c) transfer and (d) output characteristics of a NCFG memory device with randomly oriented crystals.
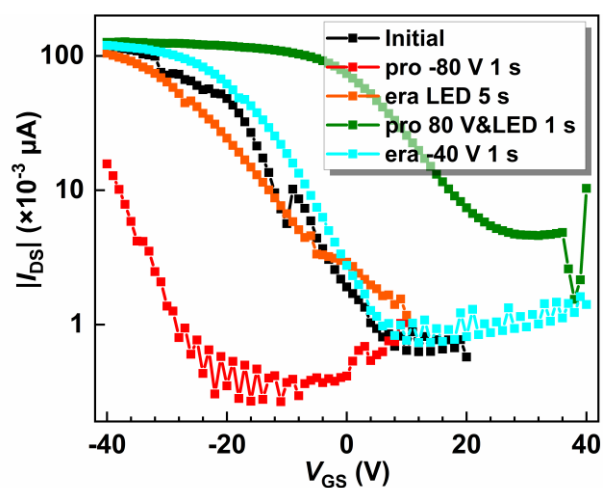
Figure S8. Programming and erasing characteristics of a NCFG memory device with an Au@PS-*b*-P4VP nanocomposite film and an oriented Tips-P5 layer.
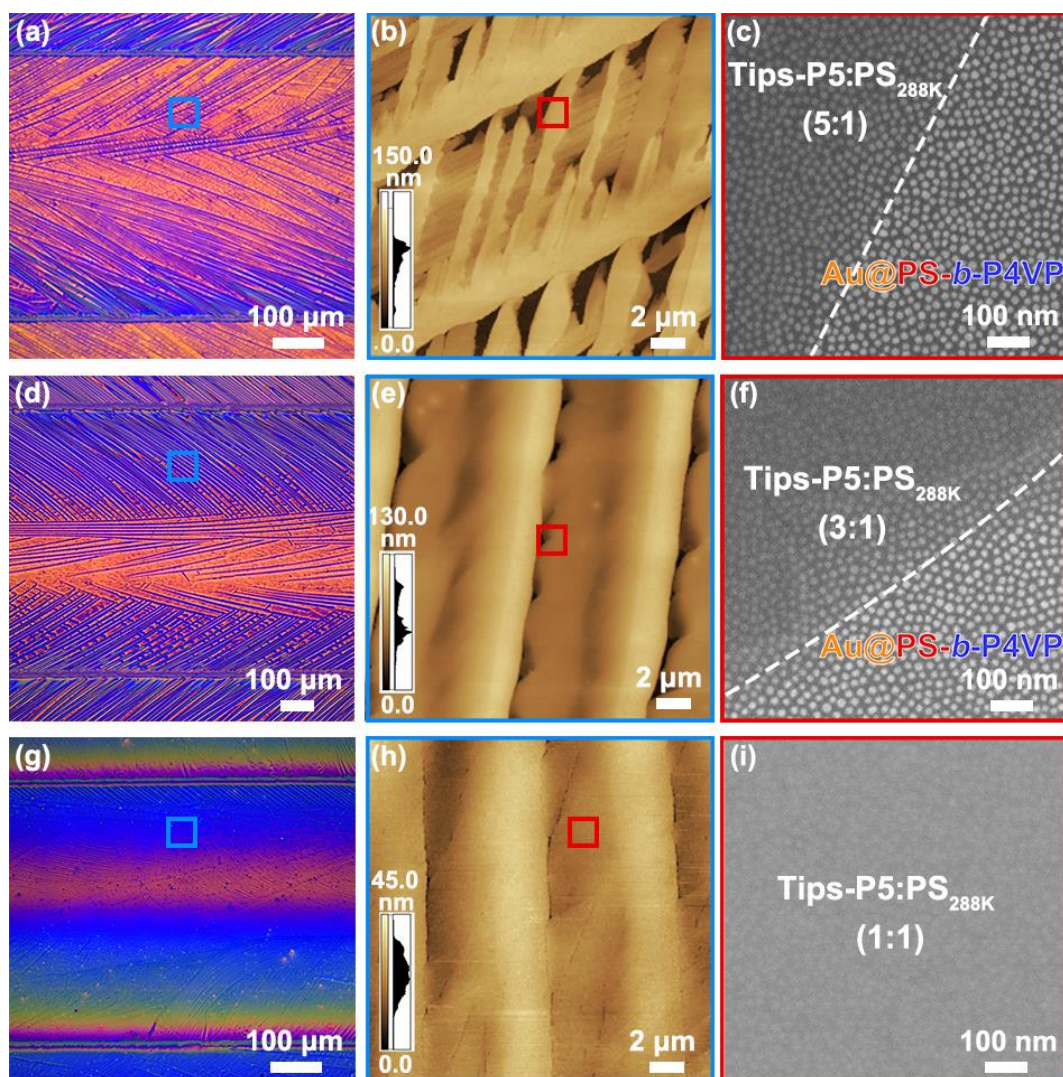
Figure S9. OM (the left column), AFM (the middle column), and SEM (the right column) images of Tips-P5/PS layers with different mass ratios of Tips-P5:PS: (a-c) 5:1; (d-f) 3:1; (g-i) 1:1.
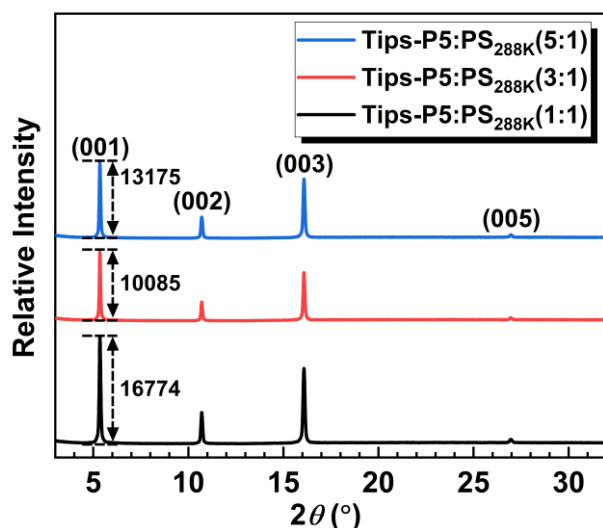
Figure S10. XRD curves of printed Tips-P5/PS layers with different mass ratios of Tips-P5:PS.
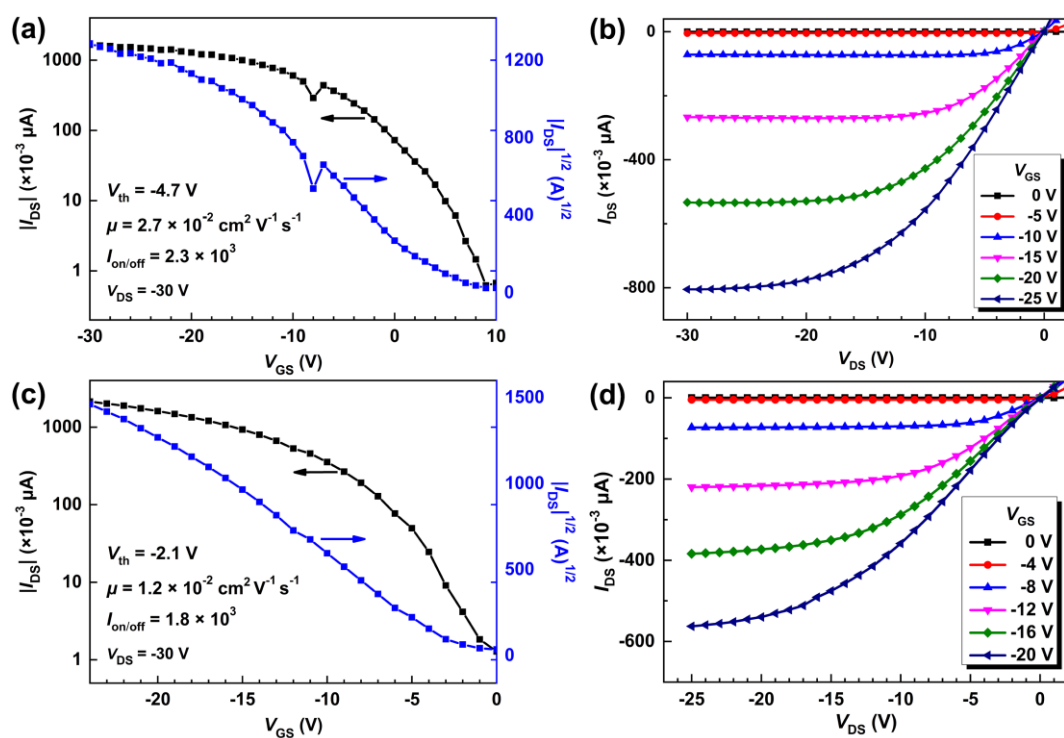
Figure S11. (a, c) Transfer (the left column), (b, d) output curves (the right column) of different optimized NCFG memory devices consisting of the same Au@PS-*b*-P4VP nanocomposite film and oriented Tips-P5 active layer.
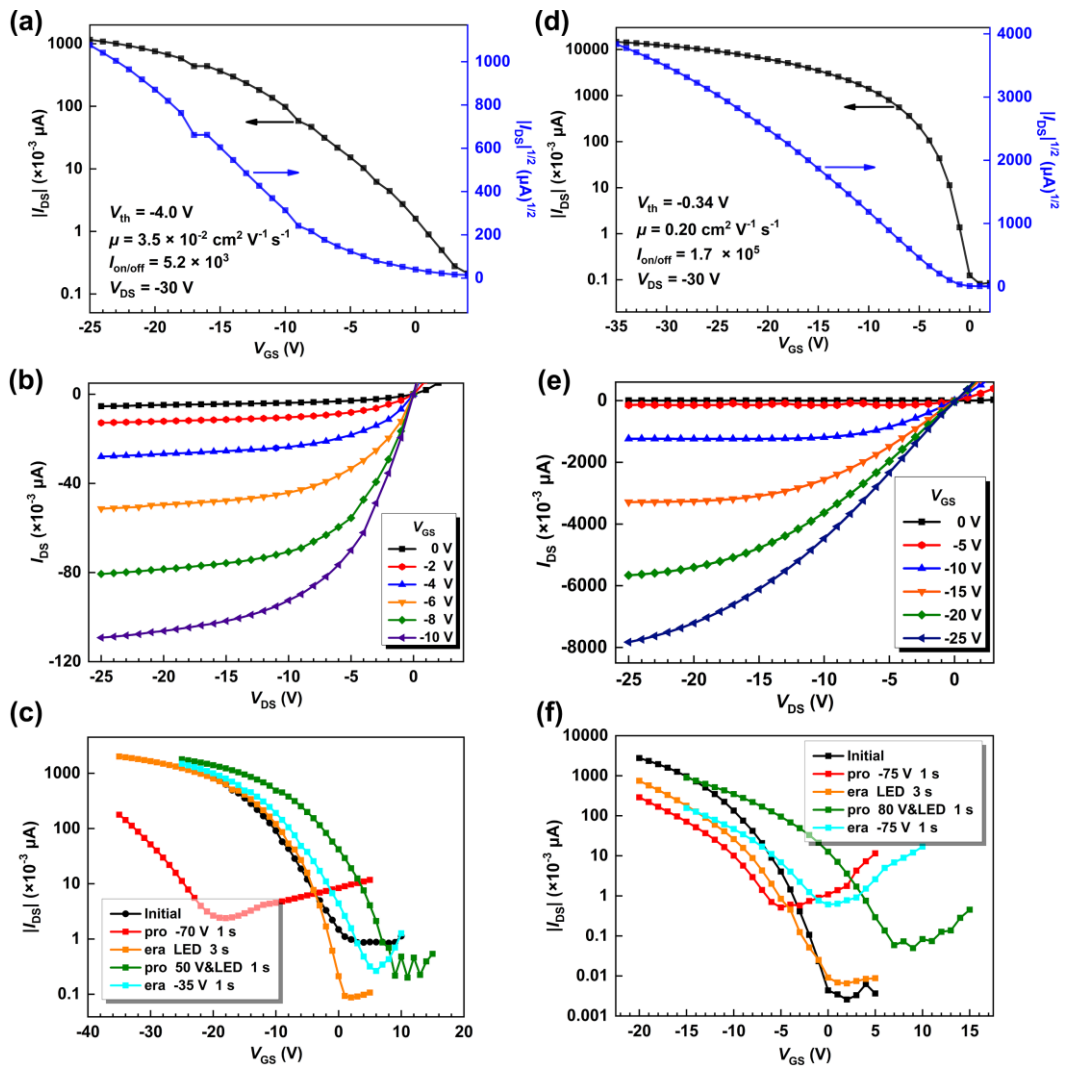
Figure S12. (a, d) Transfer, (b, e) output, (c, f) programming, and erasing curves of optimized NCFG memory devices with different mass ratios of Tips-P5 and PS: (a-c) Tips-P5:PS (5:1); (d-f) Tips-P5:PS (1:1).
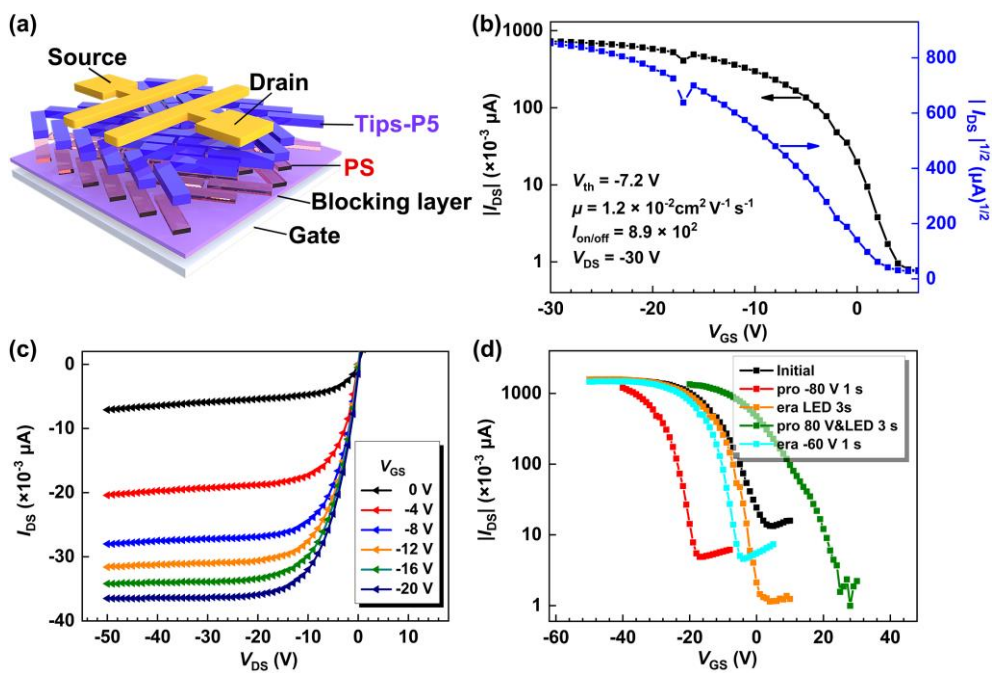
Figure S13. (a) Schematic illustration of the structure of a PS electret memory device; (b) transfer, (c) output, and (d) programming and erasing of an electret memory device.

Table S2. Energy levels of used materials.

	Tips-P5	PS	P4VP	Au	SiO$_2$
LUMO (eV)	-3.6	-2.5	-0.5	/	-1.0
HOMO (eV)	-5.2	-7.5	-6.5	/	-9.9
Work function (eV)	/	/	/	-5.1	/
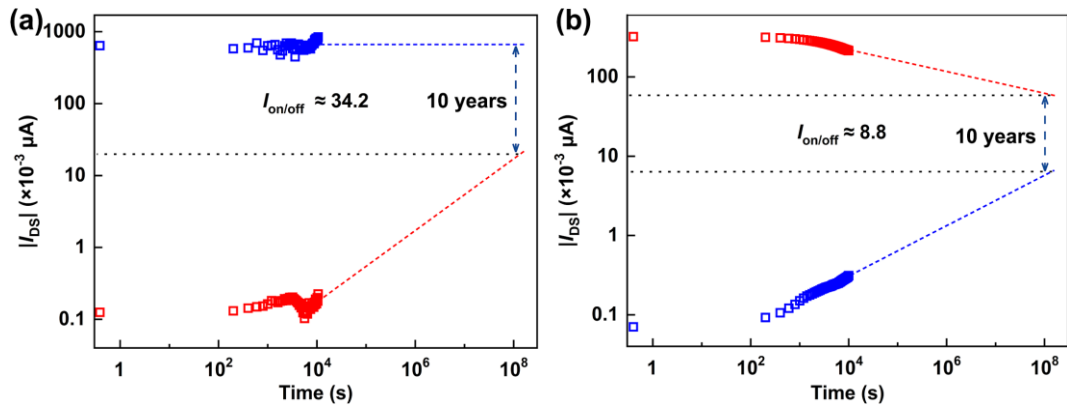
Figure S14. Prolonged retention characteristics of an optimized NCFG memory device: (a) hole-trapping mode; (b) electron-trapping mode.
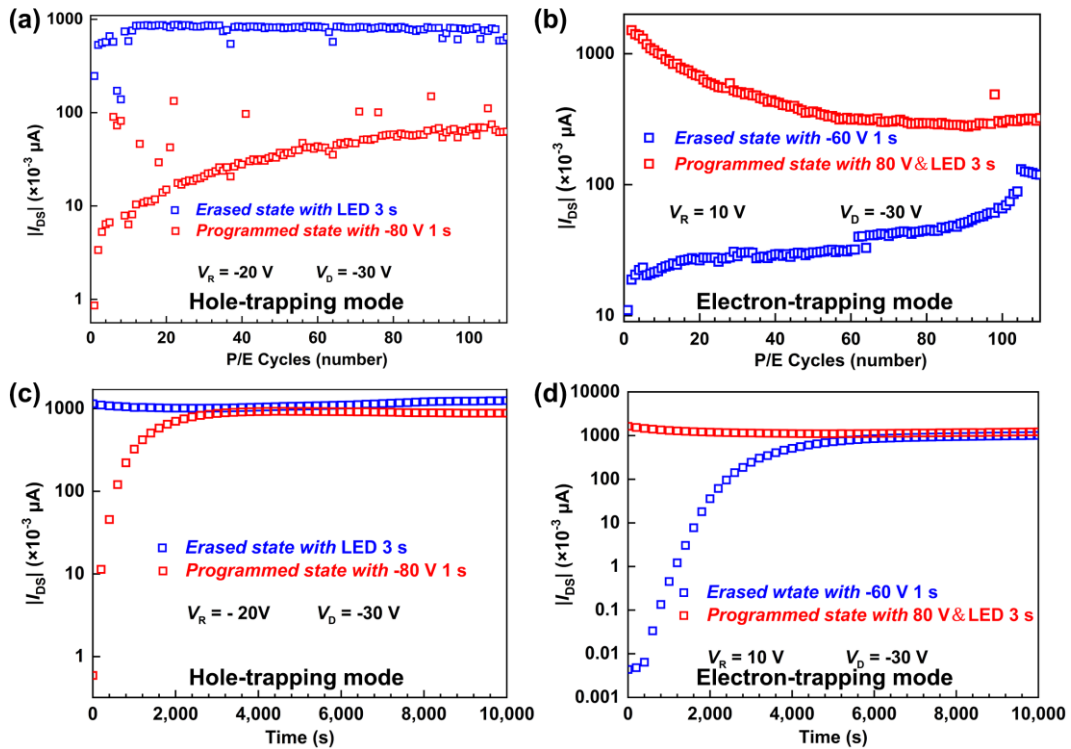

Figure S15. (a, b) Write-read-erase-read (WRER) endurance of a PS electret memory device; (c, d) retention characteristics of an electret memory device.

Table S3. Comparison of the fabrication and electrical performance of optimized NCFG memory devices with the literature.

Devices	Preparation of functional layers		V_{th} (V)	average ΔV_{th} ($V_{P\text{-}H}$/$V_{P\text{-}E}$) (V)[a]	Retention	
	NCFG/TD layer	Active layer			Hole-trapping	Electron-trapping
Ref. 19	Au/PS-*b*-P2VP (spin-coating)	P3HT (spin-coating)	-17.0	43 (-100/+100&L)	> 100 hours	/
Ref. 20	Au@PS$_{12K}$ (interfacial self-assembly)	pentacene (CVD)	-15.4	74 (-100/+60&L[b])	> 10 years	/
Ref. 27	Au@PS$_{22K}$ (DIW)	pentacene (CVD)	/	51 (-80/+80&L)	/	/
Ref. 64	Au/PS-*b*-P4VP (spin-coating)	pentacene (CVD)	-3.8	11 (-25/+20&L)	10^5 seconds	/
This work	**Au@PS-*b*-P4VP (DIW)/PS (DIW)**	**Tips-P5 (DIW)**	**-(2.6 ± 1.6)**	**66 (-80/+80&L)**	**> 10 years**	**> 10 years**

[a]Data includes the programming voltage of hole-trapping ($V_{P\text{-}H}$) and electron-trapping ($V_{P\text{-}E}$) modes and the memory window (ΔV_{th}); [b]L refers to white light illumination.