Concept of a Molecular Charge Storage Dielectric Layer for Organic Thin Film Memory Transistors

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Abstract:

Molecular self-assembly is a key enabler for organic nanoelectronics, because it combines the advantages of low-temperature solution processing, regio-selective monolayer adsorption and Angstrom-scale control of the film thickness. Here we report on a concept by which a mixed self-assembled monolayer containing aliphatic and electron-accepting components is employed as an ultra-thin molecular gate dielectric to facilitate reversible, non-volatile electronic memory functionality in organic transistors at low supply voltages. The aliphatic component of the monolayer provides the necessary electrical isolation while the electron-accepting component acts as a charge storage element. By adjusting the mixing ratio of the two monolayer components, the transistor and memory characteristics can be tuned over a wide range.

Many of the early problems in the field of organic thin-film transistors (OTFTs) have been addressed and have pushed the technology closer to market applications. For example, semiconductors showing large p- and n-type mobilities [1-4], dielectrics and circuit methodologies providing low power consumption [5-8] and smart production methods suitable for flexible substrates [9-12] have been developed. Much attention has focussed on realizing electrically and environmentally stable OTFTs required to successfully implement complex systems such as radio frequency identification (RFID) tags [10, 13-16]. An avenue that has received far less attention, despite carrying tremendous promise, is the "controllable" manipulation of the transistor functionality beyond that of a switch or amplifier. Simple concepts of organic non-volatile memories (NVM) are needed, because of their importance for individualizing RFID tags or to reversibly program organic circuits [17]. Preferably, the memory functionality should be realized with low supply voltage and with the same device structures and the same materials utilized for the transistors, to avoid unnecessary complexity

and to preserve the benefit of low cost and mobile applications. In silicon technology, the most common approach to realize NVM devices for mass storage applications is the reversible manipulation of the threshold voltage of the transistors by charging or discharging a "floating" gate electrode that is sandwiched between two insulating layers inside the gate dielectric. The reversible and reproducible shift of the threshold voltage leads to two or more distinct states that are interrogated as different values of the drain current at a given gate-source voltage. The long-term retention (10 years) of the electronic charge on the floating gate is achieved by employing high-quality insulating oxides of several nanometers thickness but this requires relatively large voltages of app. 8 V for programming and erasing [18].

In this work we report on a novel concept of an electrically programmable self-assembled molecular gate dielectric layer for OTFTs (see figure 1a) that can be reversibly charged and discharged and retains these digital states even when the supply voltage is removed. Due to the small thickness of the dielectric stack (app. 5.7 nm), the memory transistors operate with very small program and erase voltages of ± 2 V. Despite the extremely small dielectric thickness, the retention time is already promising (~6 hours with a read voltage of -750 mV applied continuously). The dielectric is a mixed monolayer of aliphatic and C_{60}-functionalized phosphonic acid molecules (app. 2.1 nm thickness) on a patterned and plasma-oxidized aluminum gate electrode on a glass substrate. The aluminum oxide (AlO_x) contributes with a thickness of 3.6 nm to the dielectric layer stack [6]. As the aliphatic component, n-octadecylphosphonic acid **1** was chosen, which has already shown excellent insulating characteristics as the gate dielectric [6]. As the charge storage component, the C_{60}-derivative **2** was synthesized to take advantage of the strong acceptor properties and reversible redox behavior of C_{60} (Figure 1b and Supplementary Information SI-1) and of the self-assembly properties induced by the C_{18}-aliphatic tail with phosphonic acid anchor group. Mixed self-assembled monolayers of **1** and **2** were created by a simple "one pot" solution

process, providing a thin, robust gate dielectric with integrated charge storage units in a single process step.

We have fabricated four series of transistors (**A, B, C** and **D** - Figure 1a) with different compositions of the monolayer (mixing ratio of **1** : **2**; **A** = 100 : 0, **B** = 99 : 1; **C** = 95 : 5, and **D** = 0 : 100). In the devices **A** and **D** the SAM dielectric consists of pure compound **1** or **2**, respectively. In series **B** and **C,** we have created mixed SAMs of **1** and **2** by simultaneous self-assembly from stoichiometric solutions of the molecules. Top-contact TFTs were completed by depositing 30 nm thick films of the organic semiconductor α,α'-dihexylthiophene and 30 nm thick gold source and drain contacts through a shadow mask (W = 600 μm and L = 40 μm for all transistors). The highest temperature during device fabrication is 60°C, which makes this process fully compatible with flexible polymeric substrates. We have chosen α,α'-dihexylthiophene because of its good hole mobility and because the n-alkyl side chain is expected to provide additional insulation to C_{60}-units and improve the charge retention time by creating an embedded storage unit comparable to floating gate structures in silicon technology [18, 19].

The monolayer gate dielectrics self-assemble by immersing the substrates in a 0.1 mmol solution of the phosphonic acid molecules in 2-propanol for 24 hours. Since **1** and **2** have different head groups, the static contact angle of water is a monotonic function of the composition of the monolayer. Prior to self-assembly, the plasma-oxidized Al has an average contact angle of 10°. After self-assembly of the monolayer, contact angles of 109 ± 2° were obtained for device **A**, 107 ± 2° for device **B**, 99 ± 1° for device **C**, and 66 ± 1° for device **D** (see SI-2). The observation that the surface energy of the mixed monolayers is a monotonic function of the mixing ratio in the solution from which the monolayers were prepared suggests that the mixing ratio in the monolayer is very similar to the mixing ratio in the solution [20]. This could be confirmed by amplitude-modulation atomic force microscopy (AM-

AFM) imaging of the monolayers (Figure 2 and SI3). Due to the fifths times larger dimensions of the head group of **2** (1 nm diameter for C_{60}) compared to **1**, the C_{60} surface coverage in the SAMs occurs expanded compared to their stoichiometry (effectively ~5 times). The phase information(here add the following reference if you can: John Melcher, Carolina Carrasco, Xin Xu, José L. Carrascosa, Julio Gómez-Herrero, Pedro José de Pablo, and Arvind Raman **Origins of phase contrast in the atomic force microscope in liquids** *PNAS* 2009 106:13655-13660) in the AM-AFM images allows differentiation of the regions covered by **1** and **2** down to the molecular level (Fig. 2 and SI 3). Single isolated C_{60} molecules are visible at low concentration (1% , Figure 2b) while larger domains occur at higher concentration up to full coverage at 100% **2**.

The transfer characteristics of the transistors (Figure 3 and SI-6) show that the average threshold voltage (V_{TH}) is -880 mV for devices **A**, -285 mV for devices **B**, +170 mV for devices **C**, and +765 mV for devices **D**. These values are averages from at least three TFTs per substrate and were measured in the dark to prevent light-induced charge transfer [21]. The observation that the threshold voltage is more positive for SAMs with greater acceptor strength is in good agreement with the literature [22, 23], but in contrast to these previous reports we demonstrate here that the effect is observed not only for pure SAMs, but also for mixed monolayers.

The reference devices **A**, with the aliphatic monolayer **1** exhibit transfer curves (Figure 3a) that are essentially free of hysteresis (maximum hysteresis less than 5 mV). The hole mobility of devices **A** is 0.04 cm^2 V^{-1} s^{-1}, the on/off current ratio is larger than 10^5, and the gate current (I_G) is 1.7 x 10^{-11} A. Devices of series **B**, **C**, and **D** show a different behavior (Figure 3b, c and d). Besides the more positive threshold voltage, an anti-clockwise hysteresis that increases with the concentration of **2** in the SAMs was observed. The maximum hysteresis is 45 mV for **B**, 230 mV for **C**, and 350 mV for **D**. We believe the hysteresis in the

transfer curves of the devices with C_{60} content is the result of an efficient and reversible charge transfer between the HOMO of the thiophene molecules in the semiconductor layer and the LUMO of the fullerene acceptor units in the dielectric during device operation. The mobilities are not significantly affected by the composition of the SAM dielectric, ranging from 0.025 cm^2 V^{-1} s^{-1} to 0.06 cm^2 V^{-1} s^{-1}. The on/off current ratio systematically decreases from 10^5 to 10^2 with increasing concentration of **2** in the SAM. However, for negative gate-source voltages the drain current always exceeds the gate current by more than four orders of magnitude, indicating excellent insulator properties for all SAM dielectrics regardless of the composition.

The capacitance of the AlO$_x$/SAM dielectric stack, measured on Al/AlO$_x$/SAM/Au capacitors with an area of 50 μm $\times$ 50 μm, is between 0.68 and 0.85 μF cm^{-2}, depending on the composition of the SAM (see SI-4). The capacitance-voltage characteristics show a pronounced hysteresis that increases monotonically with increasing C_{60} content in the SAM, indicating again a charging of the C_{60} units.

To investigate the nature of the hysteresis for a potential memory behavior, the transistors were biased with positive gate-source voltages (program) and negative gate-source voltages (erase) ($V_{GS} = \pm 2$ V and $V_{DS} = 0$ V) for 30 s. Due to the shift in V_{TH}, the drain current I_D at a given gate-source voltage is different, depending on whether the device was last programmed or erased. Therefore, we have interrogated the devices by measuring I_D at a given gate-source voltage ($V_{GS} = -1$V for **A**, $V_{GS} = -750$ mV for **B**, $V_{GS} = -250$ mV for **C** and at $V_{GS} = 0$ V for **D**). The transfer characteristics of a device of series **B** before and after repeated program/read/erase/read operations are shown in Figure 4a. At a gate-source voltage of $V_{GS} = -750$ mV, the reproducible difference in I_D obtained from the transfer curves is about 23 nA. When the transistor is interrogated with a single-point measurement (less bias stress) at $V_{GS} = -750$ mV, the difference in I_D is 35 nA (see Section I in Figure 4b). The ratio

between I_D after programming and after erasing (memory ratio) depends on the composition of the SAM. Devices **A** show no response to programming. The devices of series **B** (1% C_{60} content) have a relatively small memory ratio of 2.5 (see Section I in Figure 3b), the devices of series **C** (5% C_{60} content) have a memory ratio of 26 (Section I in Figure 3c), and the devices of series **D** (100% C_{60} content) have an excellent memory ratio of 43 (Section I in Figure 4d). We note, that our observations are different to bias stress-induced threshold voltage shifts in organic transistors, observed at much stronger bias stress conditions [24, 25].

Given the small thickness of the SAM dielectrics, the ability of the fullerene units to store electronic charge for longer times (i.e. the retention time), is a major concern. For devices **D** and **C** the drain current in the programmed state decays within 1 minute to less than 10% of the initial value (see Section II in Figure 4c and 4d) indicating that in these devices the charge stored on the C_{60} units is rapidly lost due to leakage. In device **B** – with the lowest content of **2** in the SAM – a more promising long-term stability is observed (see Section II in Figure 3b). Within 1 hour, the memory ratio decreased from 2.4 to 2.2, i.e. to approximately 90 % of the initial value. After 6 hours of continuous reading, the drain current in the programmed state is still 50% of its initial value (see SI-5). The general trend of relatively short retention times is not surprising, due to the very small thickness of the gate insulator (AlO_x/C_{18}-alkyl chain) and the fact that the C_{60} units are separated from the transistor channel only by the alkyl side chains (app. 1 nm) of α,α'-dihexylthiophene molecules. Additionally we note that the read operation (V_{DS} = -1 V and V_{GS} = - 750 mV) greatly assists the transfer of stored charge back into the transistor channel, due to the electric field applied during the read operation. We believe that the longer retention time in devices of series **B** is related to the structure of the SAM. Due to the smaller concentration of **2**, the SAM is composed of small islands or even single molecules of the C_{60} derivative **2** surrounded - and thereby electrically isolated from each other - by the insulating phosphonic acids **1** (figure 2), what

could prevent charge drainage of larger domains. The concept of diluted storage units may provide a design tool to further improve the retention by better isolation of the C_{60} storage units within the SAM and with respect to the transistor channel, analogue to the concepts of "segmented" or "pinned" charge trapping as used in silicon devices by introducing isolated nanoparticles as charge storage elements or SiN_x with deep traps instead of large-area metal floating gates [26, 27]. A reversible switching behavior is observed after the retention measurements (see Section III in Figures 4b – d), indicating a promising endurance of the organic memory devices.

In summary we have demonstrated that a single layer of suitable self-assembled molecules can act as a molecular gate dielectric with addressable charge storage properties. With those layers memory properties can be implemented in organic TFTs. By applying an external electric field, electronic charges can be transferred to and accumulated in the C_{60}-acceptor units. The molecular stoichiometry of the SAM determines the device characteristics, such as threshold voltage, hysteresis and ON/OFF ratio. The memory ratio scales with the density of charge storage units in the SAM. The retention time seems to be limited by charge leakage back to the channel but can be significantly improved by diluting the C_{60} charge storage units within the SAM. The molecular approach allows the devices to operate at a low supply voltage of 2 V, permits low-temperature processing with a maximum temperature of 60°C, and the preparation of a functional charge storage molecular dielectric with a single process step.

Supplementary Information is linked to the online Version of the paper at www.nature.com/nature.

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List of Figures:

Figure 1: Schematic cross section of an organic TFT with a molecular floating-gate dielectrics (**a**) [expansion: schematic composition of the molecular gate dielectrics (with different stoichiometry of **1** and **2**]; chemical structure of molecules composing the SAM in device series A – D (**b**).

Figure 2: AM-AFM images of the SAMs with different **1**:**2** stoichiometric rotios. In each case, the main panel shows the phase image used to identify the molecular species. The C_{60} molecules appear as minima in the phase image (exemplified by arrows in **b** and **c**). The two lower panels present respectively the topographic image (left) and the phase image of the main panel after detection of the regions attributed to **2** in red (right). The detection procedure is detailed in SI with an example. The scale bar corresponds to 10° for all the phase images and to 1.1nm (a), 1.7nm (b), 2.6nm (c) and 1.2nm (d) for topography.

Figure 3: Electrical transfer characteristics of organic thin film memory transistors with different molecular gate dielectrics composition (V_{DS} = -1V); pure **1** (**a**), 99 : 1 (**b**), 95 : 5 (**c**) and pure **2** (**d**).

Figure 4: a) Capture of transfer characteristics of repeated program/read/erase/read operations of device of series **B.** Reversible switching behavior (section I and III) and retention of the "on-state" (section II) of the memory TFTs with different molecular gate dielectrics composition; **b**) 99 : 1 , **c**) 95 : 5, and **d**) pure **2** (The retention in **b** is given for 60 minutes).
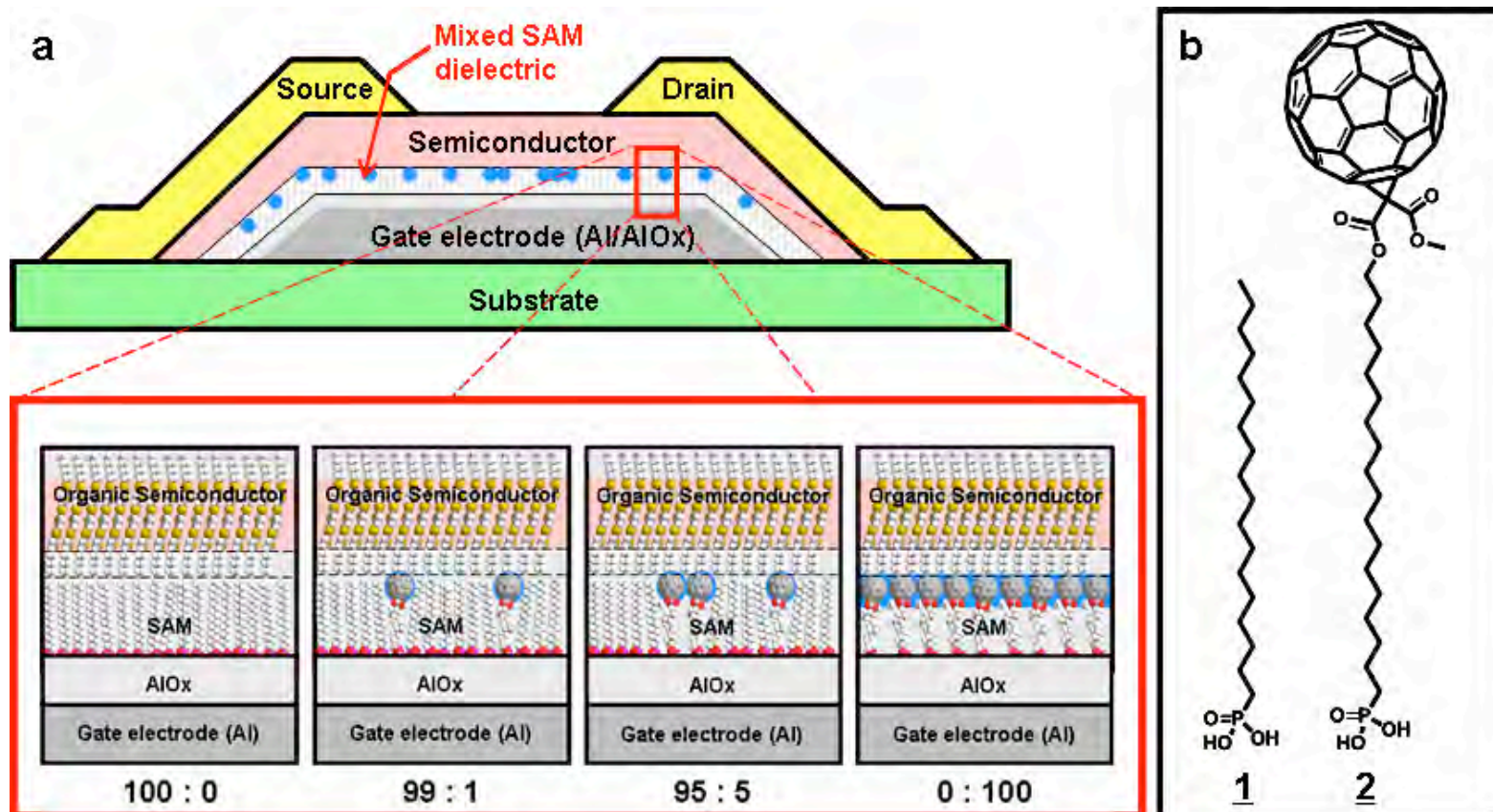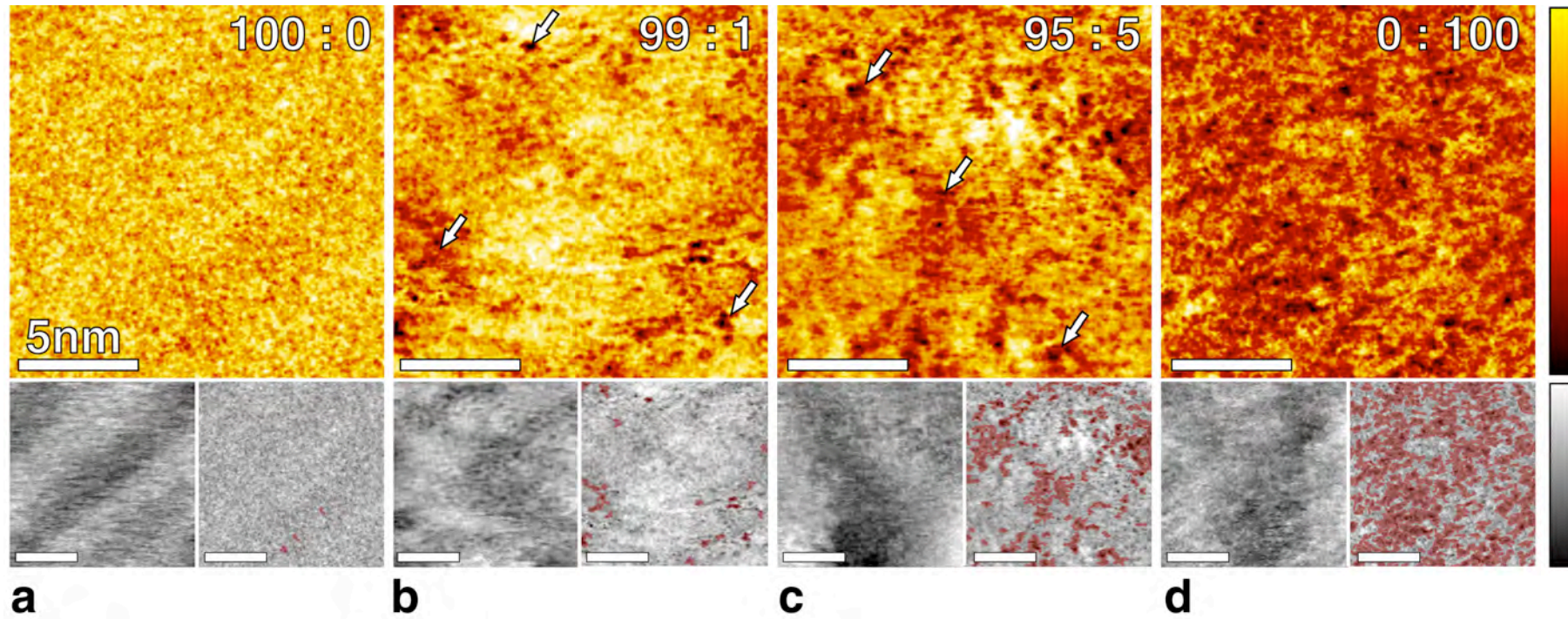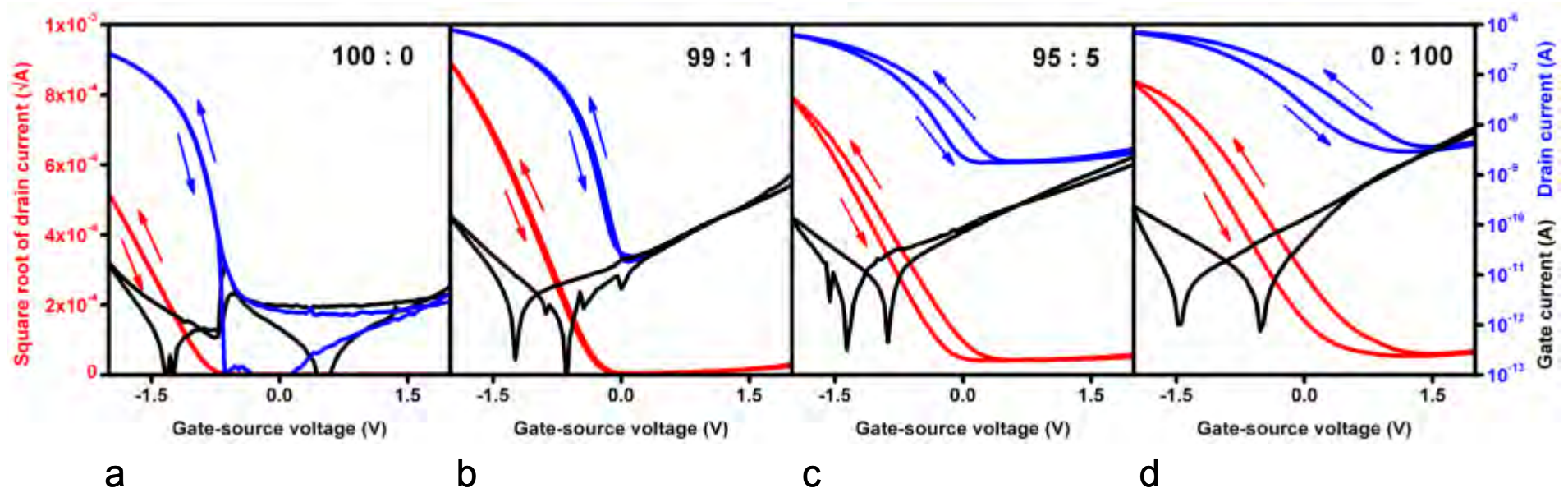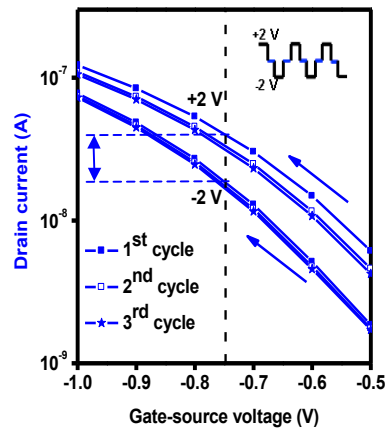
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Figure 3:

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ΔI_D

a

b

c

Figure 4:

d

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