# A New VSC-HVDC Model for Power Flows Using the Newton-Raphson Method

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*Abstract* **— The paper presents a new model of the VSC-HVDC aimed at power flow solutions using the Newton-Raphson method. Each converter station is made up of the series connection of a Voltage Source Converter (VSC) and its connecting transformer which is assumed to be a tap-changing (LTC) transformer. The new model represents a paradigm shift in the way the fundamental frequency, positive sequence modeling of VSC-HVDC links are represented, where the VSCs are not treated as idealized, controllable voltage sources but rather as compound transformer devices to which certain control properties of PWM-based inverters may be linked– just as DC-to-DC converters have been linked, conceptually speaking, to step-up and step-down transformers. The VSC model and by extension that of the VSC-HVDC, takes into account, in aggregated form, the phase-shifting and scaling nature of the PWM control. It also takes into account the VSC inductive and capacitive reactive power design limits, switching losses and ohmic losses.**

*Index Terms* **— VSC-HVDC links, PWM, Newton-Raphson method, power flows**

# I. INTRODUCTION

OWER transmission using VSC-HVDC is a relatively recent progression of the HVDC technology which was originally based on the use of mercury arc valves and replaced in the mid-seventies by solid-state valves of the thyristor type [1]. It is reported that on  $10<sup>th</sup>$  March 1997 power was transmitted on the world's first VSC-HVDC transmission system between Hellsjön and Grängerg in central Sweden - the scheme was an experimental one, rated at only 3 MW and  $\pm 10$  kV [2]. The main two providers of this technology use their commercial brand names when refereeing to the VSC-HVDC technology: ABB uses the name HVDC-Light<sup>®</sup> and Siemens uses the name HVDC PLUS<sup>®</sup>. The semiconductor valves currently employed at VSC-HVDC stations are IGBTs and the valve firing control is PWM; this enables operation at switching frequencies higher than the fundamental frequency resulting in fast and independent control of both active and reactive powers. The HVDC-Light<sup>®</sup> technology has evolved a great deal since its introduction in 1997. It is now in its fourth generation, P

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employs the cascaded-two-level (CTL) topology and low switching frequencies. It is termed HVDC Light G4 and offers two main advantages compared to previous generations: converter losses are in the order of 1% as opposed to 3% found in the early designs, and low harmonic generation which have made the use of AC harmonic filters all but redundant [3]. The HVDC PLUS<sup>®</sup> exhibits similar operational characteristics - it uses multi-level converters of the modular type and low switching frequencies.

The two most basic VSC-HVDC configurations are the back-to-back and point-to-point in either mono-polar or bipolar fashions. The two mono-polar VSC-HVDC links are shown schematically in Fig. 1 [5].



Figure 1: VSC-HVDC schematic representation: (a) back-to-back; (b) point-to-point

As illustrated in Fig. 1, each converter station comprises a VSC and an interfacing LTC transformer. The transformer's primary and secondary windings are connected to the high-voltage power grid and to the AC side of the VSC, respectively – this makes each VSC to be shunt-connected with the AC system, just as if they were two STATCOMs. However, the two VSCs are series-connected on their DC sides; sharing a capacitor in the case of the back-to-back configuration and through a DC cable in the case of the point-to-point configuration.

The fundamental frequency operation of the VSC-HVDC schemes shown in Fig. 1 may be modeled by employing two VSC models which are normally represented each by a variable voltage source behind a coupling impedance, and linked together by a mismatch active power constraining equation [4]-[6] and solved in a unified manner using

Newton-type methods. These contributions address key VSC-HVDC modeling issues such as back-to-back and point-to-point schemes [4], multi-terminal schemes [5], and extensions to optimal power flows [6]. In these contributions the emphasis is on the AC side of the VSC-HVDC links and no DC representation is available. One possible alternative to provide the VSC-HVDC with a certain amount of DC representation is to use two of the equivalent voltage source models reported in [7], where the STATCOM's AC voltage is expressed as a function of the DC voltage and the amplitude modulation ratio. Nevertheless, incorporation of the switching losses in the DC bus or a DC load would be difficult to represent in this model owing to its equivalent voltage source nature. An alternative solution approach to solve the multi-terminal VSC-HVDC power flow problem is put forward in [8,9], where a sequential numerical approach is used. In this paper, the VSC-HVDC converters are represented as variable voltages sources to solve the AC part of the network whose calculated values are then injected into a DC conductance matrix representing the multi-node DC network. This is a full VSC-HVDC power flow solution but the strong convergence characteristics of the Newton-Raphson method are sacrificed owing to the sequential iterative solution adopted. Reference [10] takes a rather simplified approach to the solution of multi-terminal VSC-HVDC links, the VSC are taken to be lossless and the numerical solution is based on power injections in both the AC and the DC nodes of the hybrid power network. A unified method for power flow calculation in AC grids with embedded multi-terminal VSC-HVDC systems is proposed in [11]. In this method all DC and AC equations are solved simultaneously in the same iteration but the converter model itself is represented in a simplified manner - each station is modelled as a PV or PQ bus at the point of common coupling and switching losses are not included. In contrast to all these recent publications on VSC-HVDC, the VSC model reported in this paper and by extension that of the VSC-HVDC, takes into account, in aggregated form, the phase-shifting and scaling nature of the PWM control. It also takes into account the VSC inductive and capacitive reactive power design limits, switching losses and ohmic losses. Furthermore, the numerical power flow solution is a simultaneous one where the AC and DC circuits are solved together using the Newton-Raphson method, keeping its strong convergence characteristics. The power flow algorithm has been programmed in Matlab. It should be noted that although no multi-terminal VSC-HVDC test cases are presented in this paper, the formulation here presented is also suitable for solving such systems.

#### II.NEW VSC-HVDC MODELS

The fundamental frequency operation of the VSC-HVDC schemes shown in Fig. 1, may be modeled by employing two of the VSC models shown in Fig. 2, where the central component of this VSC model is the ideal tap-changing transformer with a complex tap, where the winding connected to node 1 may be interpreted to be a notional AC node, internal to the VSC, and the winding connected to node 0 may be interpreted to be the DC node of the VSC. Such an interpretation is born out of the following basic relationship widely used in power electronic circuits [12]:

$$
\overline{V}_1 = m_{a}^{\dagger} e^{j\phi} E_{\text{DC}} \tag{1}
$$

where the tap magnitude  $m \int_a^b$  of the ideal tap-changing transformer corresponds to the VSC's amplitude modulation coefficient where the following relationship holds for a two-level, three-phase VSC:  $m'_a = \sqrt{3}/2 \cdot m_a$ , where in the linear range of modulation, the index *m<sup>a</sup>* takes values within bounds:  $0 < m_a < 1$  [12]. The phase angle  $\phi$  is the phase angle of the complex voltage  $\bar{v}_1$  relative to the system phase reference, and  $E_{DC}$  is the DC bus voltage which is a real scalar and on a per-unit basis carries a value of  $\sqrt{2}$ .



Figure 2: (a) VSC Schematic Representation; (b) VSC equivalent circuit

Physically the VSC is built as a two-level or a multi-level inverter operating on a constant DC voltage,  $E_{\text{DC}}$ . A relatively small DC capacitor bank of value C<sub>DC</sub>, is used to support and stabilize the controlled DC voltage,  $E_{DC}$ , needed for the converter operation [3]. The VSC provides either reactive power generation or absorption purely by electronic processing of the voltage and current waveforms within the VSC – the PWM control shifts the current waveforms to lead or lag the voltage, according to requirement. It ought to be emphasized that C<sub>DC</sub> is not used *per se* in the VAR generation/absorption process. The switching valve pattern governed by the PWM control gives the converter bridge the overall characteristic of an equivalent susceptance, *Beq*, which could be either capacitive or inductive according to operational requirements. Other elements of the electric circuit shown in Fig. 2(b) are the inductive reactance  $X_1$ representing the VSC's interface magnetics, the series resistor  $R_1$  associated with the ohmic losses, the shunt resistor (conductance *Gsw*) relating to the switching losses in the presence of a DC voltage and paralleled with the small rating capacitor  $C_{DC}$ .

It is noted quite straightforwardly that  $R_1$  is proportional to the AC terminal current squared. However, *Gsw* requires further elaboration. Under the presence of constant DC voltage and constant load current, the switching loss model would be well represented by a constant resistance (conductance)  $G_0$ , which would yield constant power loss for a given switching frequency of the PWM converter. Admittedly, the constant resistance characteristic may be inaccurate because although the DC voltage is kept largely constant, the load current will vary according to the prevailing operating condition. Hence, it is proposed that the resistance characteristic derived at rated voltage and current be corrected by the quadratic ratio of the actual current to the nominal current,

$$
G_{_0} \cdot \left(\frac{I_2^{at}}{I_2^{non}}\right)^2 \Rightarrow G_{_{\text{sw}}} \tag{2}
$$

where  $G<sub>sw</sub>$  would be a resistive term exhibiting a degree of power behavior.

Note that the secondary winding current  $I_2$  splits into  $I'_2$ and *I''*2. The latter current is rather small and it is proportional to the internal power loss of the DC capacitor [1,11]. Indeed, if the capacitor losses are neglected then the average current  $\Gamma$ <sup>2</sup> would be zero in the presence of a constant DC voltage. Alternatively, if the capacitor loss is represented by a small resistor (not shown) in parallel with the capacitor then that resistor may be paralleled instead with the resistor representing the VSC switching losses. In such a case *I''*<sup>2</sup> would be zero in a fundamental frequency, steady state model and the full power relationship between nodes 1 and 0, will be:

$$
V_0 I_2 = \overline{V}_1 (\overline{I}_1 - \overline{I}_1^*) = \overline{V}_1 \overline{I}_1^* + j B_{eq} V_1^2
$$
 (3)

The following nodal admittance matrix, developed in Appendix A in equation form, represents the fundamental frequency operation of the VSC:

$$
\begin{pmatrix}\n\overline{I}_{vR} \\
\overline{I}_{0}=0\n\end{pmatrix} = \begin{pmatrix}\n\overline{Y}_{1} & -m'_{a}(\cos\phi + j\sin\phi)\overline{Y}_{1} \\
-m'_{a}(\cos\phi - j\sin\phi)\overline{Y}_{1} & G_{sw} + m'^{2}_{a}(\overline{Y}_{1} + jB_{eq})\n\end{pmatrix} \begin{pmatrix}\n\overline{V}_{vR} \\
V_{0}\n\end{pmatrix}
$$
(4)

where  $\overline{V}_{\nu R}$  and  $\overline{I}_{\nu R}$  are the complex voltage and current at node  $vR$ ,  $\bar{I}_0$  is a zero injected nodal current at node 0 and  $V_0$ is the voltage at the DC bus which equals the voltage  $E_{DC}$ across the DC capacitor. Also,  $T_v = m'_a(\cos \phi + j \sin \phi)$ ,  $\overline{T}_V = \overline{T}_I^*$  and  $\overline{Y}_1 = 1/(R_1 + jX_1)$ .

# III. POWER FLOW MODEL: BACK-TO-BACK VSC-HVDC

The linearized equation corresponding to the power flow solution of the back-to-back VSC-HVDC, using the Newton-Raphson method is derived in this section.

# *A. Back-to-Back VSC-HVDC Nodal Power Equations*

The complex power model for the rectifier is derived from the nodal admittance matrix:

$$
\begin{aligned}\n\left(\frac{\overline{S}_{vR}}{\overline{S}_{0}}\right) &= \begin{pmatrix}\n\overline{V}_{vR} & 0 \\
0 & V_{0}\n\end{pmatrix}\n\begin{pmatrix}\n\overline{I}_{vR}^{*} \\
\overline{I}_{0}^{*}\n\end{pmatrix} \\
&= \begin{pmatrix}\n\overline{V}_{vR} & 0 \\
0 & V_{0}\n\end{pmatrix}\n\begin{pmatrix}\n\overline{Y}_{1}^{*} & -m'_{a}\left(\cos\phi - j\sin\phi\right)\overline{Y}_{1}^{*} \\
-m'_{a}\left(\cos\phi + j\sin\phi\right)\overline{Y}_{1}^{*} & G_{sv} + m'^{2}_{a}\left(\overline{Y}_{1}^{*} - jB_{eq}\right)\n\end{pmatrix}\n\begin{pmatrix}\n\overline{V}_{vR}^{*} \\
V_{0}\n\end{pmatrix}\n\end{aligned}
$$
\n(5)

Following some arduous algebra, the nodal active and

reactive power expressions for the rectifier are arrived at:  
\n
$$
P_{vR} = G_{1R}V_{vR}^2 - m'_{aR}V_{vR}V_{0R} \left[ G_{1R} \cos(\theta_{vR} - \theta_{0R} - \varphi_R) + B_{1R} \sin(\theta_{vR} - \theta_{0R} - \varphi_R) \right]
$$
\n
$$
Q_{vR} = -B_{1R}V_{vR}^2 - m'_{aR}V_{vR}V_{0R} \left[ G_{1R} \sin(\theta_{vR} - \theta_{0R} - \varphi_R) - B_{1R} \cos(\theta_{vR} - \theta_{0R} - \varphi_R) \right]
$$
\n
$$
P_{0R} = (m'_{aR} G_{1R} + G_{vR})V_{0R}^2 - m'_{aR}V_{vR}V_{0R} \left[ G_{1R} \cos(\theta_{0R} - \theta_{vR} + \varphi_R) + B_{1R} \sin(\theta_{0R} - \theta_{vR} + \varphi_R) \right]
$$
\n
$$
Q_{0R} = -m'_{aR} (B_{1R} + B_{eqR})V_{0R}^2 - m'_{aR}V_{vR}V_{0R} \left[ G_{1R} \sin(\theta_{0R} - \theta_{vR} + \varphi_R) - B_{1R} \cos(\theta_{0R} - \theta_{vR} + \varphi_R) \right]
$$
\n(6)

the inverter,

Likewise, another set of equations may be developed for  
\nthe inverter,  
\n
$$
P_{vl} = G_{1l}V_{vl}^2 - m_{al}^2 V_{vl}V_{0l} \left[ G_{1l} \cos(\theta_{vl} - \theta_{0l} - \varphi_l) + B_{1l} \sin(\theta_{vl} - \theta_{0l} - \varphi_l) \right]
$$
\n
$$
Q_{vl} = -B_{1l}V_{vl}^2 - m_{al}^2 V_{vl}V_{0l} \left[ G_{1l} \sin(\theta_{vl} - \theta_{0l} - \varphi_l) - B_{1l} \cos(\theta_{vl} - \theta_{0l} - \varphi_l) \right]
$$
\n
$$
P_{0l} = (m_{al}^2 G_{1l} + G_{svl})V_{0l}^2 - m_{al}^2 V_{vl}V_{0l} \left[ G_{1l} \cos(\theta_{0l} - \theta_{vl} + \varphi_l) + B_{1l} \sin(\theta_{0l} - \theta_{vl} + \varphi_l) \right]
$$
\n
$$
Q_{0l} = -m_{al}^2 (B_{1l} + B_{eql})V_{0l}^2 - m_{al}^2 V_{vl}V_{0l} \left[ G_{1l} \sin(\theta_{0l} - \theta_{vl} + \varphi_l) - B_{1l} \cos(\theta_{0l} - \theta_{vl} + \varphi_l) \right]
$$
\n(7)

Since both converters are connected their DC side to a common bus 0; it is quite clear that buses 0*R* and 0*I* are the same bus in this back-to-back VSC-HVDC application.

# *B. Back-to-Back VSC-HVDC Linearised Equations*

These nodal power equations are non-linear and their solution, for a pre-defined set of generation and load pattern may be carried out using the Newton-Raphson method. A large number of parameter regulation options are available for the VSC-HVDC link by making use of the voltage and power regulating capabilities of the two VSCs and the voltage regulating capabilities of the two LTCs. A common practice is to use the rectifier to regulate power on its DC side and to use the inverter to regulate voltage magnitude on its AC side. Also, the small DC capacitor banks associated to each VSC are used to support and stabilize the DC voltage,  $E_{\text{DC}}$ , which is needed for converter operation.

A constraining active power equation is required for the action of the phase shifter element of the VSC model to take place - one such equation will be required for the VSC rectifier and another for the VSC inverter. The two state variables associated to the two constraining power equations are the angles of the phase shifter elements. Moreover, constraining equations are required for the reactive powers to force to zero the reactive power at node 0. Hence, two additional state variables become available, namely the equivalent susceptances of the two VSCs.

Linearization of eqns. (6) and (7) around the base operating point:  $(\theta_{\scriptscriptstyle\!{\tiny W}}^{\scriptscriptstyle(0)},V_{\scriptscriptstyle\!{\tiny W}}^{\scriptscriptstyle(0)},\theta_{\scriptscriptstyle\!{\tiny W}}^{\scriptscriptstyle(0)},W_{\scriptscriptstyle\!{\tiny W}}^{\scriptscriptstyle(0)},\theta_{\scriptscriptstyle 0}^{\scriptscriptstyle(0)},m^{\scriptscriptstyle\!{\tiny I}}{\scriptscriptstyle 0},\theta_{\scriptscriptstyle\!{\tiny B}}^{\scriptscriptstyle(0)},\theta_{\scriptscriptstyle\!{\tiny B}}^{\scriptscriptstyle(0)},B_{{\scriptscriptstyle\!{\tiny W}}}^{\scriptscriptstyle(0)},\theta_{\scriptscriptstyle\!{\tiny B}}^{\scriptscriptstyle(0)},$ suitable to regulate power on the DC bus and to regulate voltage magnitude at the inverter's AC side using *m'aI*. Notice that  $V_0$  is kept at a constant value by treating node 0 as a PV-like bus. The relevant system of equations is arranged in the structure shown in equation (8).

$$
\begin{bmatrix}\n\Delta P_x \\
\Delta Q_x \\
\Delta P_y\n\end{bmatrix} = \begin{bmatrix}\n\frac{\partial P_x}{\partial Q_x/\partial \theta_{yx}} & \frac{\partial P_x}{\partial V_{yx}} \frac{\partial V_x}{\partial W_x} & 0 & 0 & \frac{\partial P_x}{\partial Q_x/\partial \theta_0} & 0 & \frac{\partial P_x}{\partial Q_x/\partial \theta_x} & \frac{\partial P_x}{\partial \theta_x} \frac{\partial P_x}{\partial \theta_x} & 0 & 0 \\
\frac{\partial Q_x}{\partial P_y} \\
\Delta Q_y \\
\Delta Q_y \\
\Delta Q_{0x} + \Delta Q_{0y} \\
\Delta Q_{0x-x} \\
\Delta P_{0x-x} \\
\Delta Q_{0y-x}\n\end{bmatrix} = \begin{bmatrix}\n\frac{\partial P_x}{\partial Q_x/\partial \theta_{yx}} & \frac{\partial P_x}{\partial Q_x/\partial \theta_{yx}} & 0 & 0 & \frac{\partial P_x}{\partial Q_x/\partial \theta_0} & 0 & \frac{\partial P_x}{\partial Q_x/\partial \theta_x} & \frac{\partial P_x}{\partial \theta_x/\partial \theta_x} & \frac{\partial P_x}{\partial \theta_x/\partial \theta_x} & 0 & 0 \\
\frac{\partial Q_x}{\partial P_y/\partial \theta_x} & \frac{\partial Q_y}{\partial P_y/\partial \theta_x} & \frac{\partial Q_y}{\partial P_y/\partial \theta_x} & \frac{\partial Q_y}{\partial P_y/\partial \theta_y} & \frac{\partial Q_y}{\partial P_y/\partial \theta_x} \\
\frac{\partial Q_y}{\partial \theta_x} + \Delta Q_{0y} \\
\frac{\partial Q_{0x-x}}{\partial \theta_x} & \frac{\partial Q_y}{\partial \theta_x} \\
\frac{\partial Q_{0x-x}}{\partial \theta_x} & \frac{\partial Q_{0x-x}}{\partial \theta_x} & \frac{\partial Q_{0x-x}}{\partial \theta_x} &
$$

# *1) Mismatch power terms and control variables:*

The mismatch power terms used will be the difference between the net power and the calculated power at buses: *vR*, *vI* and 0. The calculated powers are determined using the nodal power eqns. (6) and (7), giving,

$$
\Delta P_{ik} = P_{ik, \text{rad}} - P_{ik, \text{cal}} = (P_{ik, \text{gen}} - P_{ik, \text{bad}}) - P_{ik, \text{cal}} \n\Delta Q_{ik} = Q_{ik, \text{rad}} - Q_{ik, \text{cal}} = (Q_{ik, \text{gen}} - Q_{ik, \text{bad}}) - Q_{ik, \text{cal}} \n\Delta P_{0k} = P_{0k, \text{end}} - P_{0k, \text{cal}} = (P_{0k, \text{gen}} - P_{0k, \text{bad}}) - P_{0k, \text{cal}} \n\Delta Q_{0k} = Q_{0k, \text{end}} - Q_{0k, \text{cal}} = (Q_{0k, \text{gen}} - Q_{0k, \text{bad}}) - Q_{0k, \text{cal}} \n\Delta Q_{0k} = Q_{0k, \text{end}} - Q_{0k, \text{cal}} = (Q_{0k, \text{gen}} - Q_{0k, \text{bad}}) - Q_{0k, \text{cal}} \n\Delta P_{0k \to ik} = P_{0k \to ik, \text{reg}} - P_{0k \to ik, \text{cal}} \n\Delta Q_{0k \to ik} = 0 - Q_{0k \to ik, \text{cal}} \n\Delta P_{ij} = P_{ij, \text{end}} - P_{ij, \text{cal}} = (P_{ij, \text{gen}} - P_{ij, \text{bad}}) - P_{ij, \text{cal}} \n\Delta Q_{ij} = Q_{ij, \text{end}} - Q_{ij, \text{cal}} = (Q_{ij, \text{gen}} - Q_{ij, \text{bad}}) - Q_{ij, \text{cal}} \n\Delta Q_{0j} = Q_{0j, \text{end}} - Q_{0j, \text{cal}} = (Q_{0j, \text{gen}} - Q_{0j, \text{bad}}) - Q_{0j, \text{cal}} \n\Delta Q_{0j} = Q_{0j, \text{end}} - Q_{0j \to il, \text{cal}} \n\Delta Q_{0j \to ij} = -P_{0j \to il, \text{end}} = (Q_{0j \to pi, \text{cal}} - Q_{0j, \text{bad}}) - Q_{0j, \text{cal}} \n\Delta Q_{0j \to ij} = -P_{0j \to il, \text{end}}
$$

The mismatch power flow in branches 0*R*-*vR* and 0*I*-*vI* is the difference between the target power flow at the branch and the calculated power. In this application, the reactive power targets are set to zero and  $P_{0R\rightarrow R,reg} = -P_{0I\rightarrow I,reg}$ .

*2) State variables and increments:*

The state variables are updated at iteration (*r*), as follows:

$$
\theta_{w}^{(r)} = \theta_{w}^{(r-1)} + \Delta \theta_{w}^{(r)}
$$
\n
$$
V_{w}^{(r)} = V_{w}^{(r-1)} + (\Delta V_{w}^{(r)}/V_{w}^{(r)}) \cdot V_{w}^{(r-1)}
$$
\n
$$
\theta_{q}^{(r)} = \theta_{q}^{(r-1)} + \Delta \theta_{q}^{(r)}
$$
\n
$$
\theta_{0}^{(r)} = \theta_{0}^{(r-1)} + \Delta \theta_{q}^{(r)}
$$
\n
$$
m_{q}^{(r)} = m_{q}^{(r-1)} + (\Delta m_{q}^{(r)}/m_{q}^{(r)}) \cdot m_{q}^{(r-1)}
$$
\n
$$
\phi_{k}^{(r)} = \phi_{k}^{(r-1)} + \Delta \phi_{k}^{(r)}
$$
\n
$$
\phi_{l}^{(r)} = \phi_{l}^{(r-1)} + \Delta \phi_{l}^{(r)}
$$
\n
$$
B_{wq}^{(r)} = B_{wq}^{(r-1)} + \Delta B_{wq}^{(r)}
$$
\n
$$
B_{wq}^{(r)} = B_{wq}^{(r-1)} + \Delta B_{wq}^{(r)}
$$
\n
$$
\theta_{q}^{(r)} = \theta_{q}^{(r-1)} + \Delta B_{wq}^{(r)}
$$

# *3) Practical implementations:*

#### *a) Control strategy:*

As illustrated in Fig. 1(a), the VSC acting as rectifier is assumed to be connected between the sending bus, *vR*, and the receiving bus, 0, with the former taken to be the VSC's AC bus and the latter taken to be the VSC's DC bus. The voltage  $V_0$  is kept constant by the action of a small DC capacitor bank, each of value  $C_{\text{DC}}$ .

The voltage magnitude  $V_{vR}$  is regulated within

system-dependent maximum and minimum values afforded by the following basic relationships:

$$
|V_{\nu R}| = m_{aR} E_{DC} - \sqrt{R_1^2 + X_1^2} \cdot |\bar{I}_1| \tag{11}
$$

Note that in the linear range of modulation, the index *maR* takes values within the bounds:  $0 < m_{aR} < 1$ . However, in VSC-HVDC power transmission applications, it is unlikely that values of the actual amplitude modulation ratio lower than 0.5 will be used. Upper design limits for the VSC current are adhered to:  $|\overline{I}_1| < I_{VSCmax}$ ; and the upper and lower ceilings of  $B_{eqR}$  are attained from the design values of  $E_{DC}$ and  $\pm Q_{VSC}$ :  $B_{eqR+} = + Q_{VSC}/E_{DC}^2$  and  $B_{eqR-} = -Q_{VSC}/E_{DC}^2$ . Similar relationships exist for the VSC acting as inverter which is connected between the sending bus, *vI*, and the receiving bus, 0.

#### *b) Simplifying assumptions:*

The two resistors that account for the internal losses of each one of the VSCs and the inductors that represent their interface magnetics are taken to be constant parameters.

A key feature of this model is that the phase angle value at node 0 is independent of circuit parameters or network complexity to the left of bus *vR* and to the right of bus *vI*. The reason is that the ideal phase shifter decouples, angle-wise, the circuits to its left and to its right. Moreover, the phase angle voltage at bus 0 keeps its value given at the point of initialization. Hence, in the application pursued in this paper, it makes sense to stick to zero phase angle voltage initialization for this bus - when looked at it from the vantage of rectangular coordinates, its imaginary part does not exist,

# i.e.  $V_0 = V_0 \angle 0 \rightarrow V_0 = e_0 + j0 \rightarrow V_0 = e_0$ .

# *c) Initial parameters and limits:*

Three sets of VSC parameters require initialization: the amplitude modulation ratios  $(m'_{aR}$  and  $m'_{aI})$ ; the phase angles ( $\phi_R$  and  $\phi_l$ ) and the equivalent shunt susceptances  $(B_{eqR}$  and  $B_{eqI}$ ). The amplitude modulation ratios and their phase angles may be set at 1 and 0. The VSCs are assumed to operate within their linear regions [12] taking positive maximum values of 1 whereas the phase angles are assumed to have no limits. The equivalent shunt susceptances are initialized at values that lie within the range  $B_{eq+}$  and  $B_{eq-}$ .

# *C. LTC Transformer Model*

The nodal admittance matrix of the LTC transformer

connected between buses *k* and *vR*, is:

$$
\begin{pmatrix} \overline{I}_k \\ \overline{I}_{\kappa} \end{pmatrix} = \begin{pmatrix} \overline{Y}_t & -T\overline{Y}_t \\ -T\overline{Y}_t & T^2\overline{Y}_t \end{pmatrix} \begin{pmatrix} \overline{V}_k \\ \overline{V}_{\kappa} \end{pmatrix}
$$
\n(12)

where  $\overline{V}_k$ ,  $\overline{I}_k$ ,  $\overline{V}_{vR}$ ,  $\overline{I}_{vR}$  are the complex voltages and currents at nodes *k* and *vR*. Also, *T* is the LTC transformer tap and  $\overline{Y}_t$  is the transformer leakage admittance.

The LTC nodal active and reactive power expressions at buses *k* and *vR*, are:

$$
P_k = G_r V_k^2 - TV_k V_{sk} [G_r \cos(\theta_k - \theta_{sk}) + B_r \sin(\theta_k - \theta_{sk})]
$$
  
\n
$$
Q_k = -B_r V_k^2 - TV_k V_{sk} [G_r \sin(\theta_k - \theta_{sk}) - B_r \cos(\theta_k - \theta_{sk})]
$$
  
\n
$$
P_{sk} = G_r T^2 V_{sk}^2 - TV_k V_{sk} [G_r \cos(\theta_{sk} - \theta_r) + B_r \sin(\theta_{sk} - \theta_k)]
$$
  
\n
$$
Q_{sk} = -B_r T^2 V_{sk}^2 - TV_k V_{sk} [G_r \sin(\theta_{sk} - \theta_k) - B_r \cos(\theta_{sk} - \theta_k)]
$$
\n(13)

where  $V_k$  and  $\theta_k$  are the magnitude and phase angle of the nodal complex voltage  $\bar{V}_k$ . Likewise,  $V_{vR}$  and  $\theta_{vR}$  are the magnitude and phase angle of the nodal complex voltage  $\bar{V}_{vR}$ . Also,  $G_t$  and  $B_t$  are the real and imaginary parts of  $Y_t$ .

The LTC tap may be used to regulate voltage magnitude at either bus *k* or bus *vR*. For instance, linearization of eqn. (13) around the base operating point:  $(\theta_k^{(0)}, T^{(0)}, \theta_{vR}^{(0)}, V_{vR}^{(0)})$ , is suitable to regulate voltage magnitude at bus *k*:

$$
\begin{bmatrix}\n\Delta P_k \\
\Delta Q_k \\
\Delta P_m \\
\Delta P_m\n\end{bmatrix}^{\prime\prime} = \n\begin{bmatrix}\n\frac{\partial P_k}{\partial \theta_k} / \frac{\partial \theta_k}{\partial \theta_k} & (\partial P_k/\partial V_m) & \frac{\partial P_k}{\partial \theta_m} & (\partial P_k/\partial V_m) & \frac{\partial P_k}{\partial \theta_m} \\
\frac{\partial Q_k}{\partial P_m} / \frac{\partial \theta_k}{\partial \theta_k} & (\partial Q_k/\partial T) & \frac{\partial Q_k}{\partial \theta_m} & (\partial Q_k/\partial V_m) & \frac{\partial Q_k}{\partial \theta_m} \\
\frac{\partial Q_m}{\partial \theta_m} / \frac{\partial \theta_k}{\partial \theta_k} & (\partial Q_m/\partial T) & \frac{\partial P_m}{\partial \theta_m} / \frac{\partial Q_m}{\partial \theta_m} & (\partial Q_m/\partial V_m) & \frac{\partial Q_m}{\partial \theta_m}\n\end{bmatrix}^{\prime\prime} \begin{bmatrix}\n\Delta \theta_k \\
\Delta T/T \\
\Delta \theta_m\n\end{bmatrix}^{\prime\prime} \tag{14}
$$

With equation (14) describing the LTC connected between buses  $k$  and  $vR$  in Fig. 1 (a) then a similar equation would exist to describe the LTC transformer connected between buses *vI* and *m* in that figure – in fact the only

change would be in the subscripts, where *k* and *vR* would be replaced by *m* and *vI*, respectively.

The interfacing of the two back-to-back VSCs and the two LTCs to represent the full back-to-back VSC-HVDC link shown in Fig. 1(a), is quite straightforward; it requires an expansion of equation (8) to encompass buses *k* and *m*, where the self-terms of bus  $vR$  in equations (8) and (14) are added together. Furthermore, the self-terms of bus *vI* in equation (8) and an equation similar to (14) but for an LTC connected between buses *m* and *vI*, are also added together.

As seen from the linearized equation (14), the additional mismatch power terms introduced by the two LTC transformers are:  $\Delta P_k$ ,  $\Delta Q_k$ ,  $\Delta P_{vRt}$ ,  $\Delta Q_{vRt}$  and  $\Delta P_m$ ,  $\Delta Q_m$ ,  $\Delta P_{vIt}$ ,  $\Delta Q_{vIt}$ . Moreover, the power mismatches of the two LTCs coinciding with the AC nodes of the two VSCs, namely, *vR* and *vI*, are added together:  $\Delta P_{vR}$  and  $\Delta P_{vR}$ ;  $\Delta Q_{vR}$ and  $\Delta Q_{\nu R t}$ ;  $\Delta P_{\nu I}$  and  $\Delta P_{\nu I t}$ ;  $\Delta Q_{\nu I}$  and  $\Delta Q_{\nu I t}$ .

The additional state variables calculated at iteration (*r*) are:  $\theta_k^{(r)}, V_k^{(r)}, \theta_m^{(r)}, V_m^{(r)}$ . Moreover, if either bus *k* or bus *vR* is voltage controlled by the tap of the LTC connected between buses *k* and *vR* then the associated state variable is  $T^{(k)}$ , which replaces either  $V_k^{(r)}$  or  $V_{\nu R}^{(r)}$  depending on which bus the LTC tap is acting upon. A similar argument is developed for the LTC transformer connected between buses *m* and *vI*.

#### *D. Back-to-Back VSC-HVDC Test Cases*

The test case presented in this section relates to a system where the VSC-HVDC link is used to interconnect two otherwise independent AC systems represented in a rather simplified form, as shown in Fig. 3.



Figure 3: Back-to-back VSC-HVDC linking two equivalent AC sub-systems. The following parameters are used: (i) Transmission Line 1 and 2:  $R_{Tl}$ =0.05 p.u. and  $X_{TL}$ =0.10 p.u.,  $B_{TL}$ =0.06 p.u.; (ii) VSC 1 and VSC 2 series resistance and reactance: 0.001 p.u., 0.01 p.u.; (iii) VSC 1 and VSC 2 initial shunt conductance for switching loss calculation  $G_{\text{sw}}=0.01$  p.u.; (iv) LTC 1 and 2 series reactance: 0.06 p.u.; (v) active and reactive power load at bus 2: 1 p.u. and 0.5 p.u.; (vi) active and reactive power load at bus 5: 1.5 p.u. and 0.5 p.u.

In this numerical example the two VSCs are assumed to be connected to their respective AC systems by LTC transformers operating off their nominal tap positions. As shown in Fig. 3, the back-to-back VSC-HVDC is connected between buses 3 and 4, with bus 0 being the DC bus where the voltage is regulated at 1.4142 p.u. and the power leaving the rectifier is set at 1 p.u. using VSC 1. Notice that since the back-to-back VSC-HVDC provides for an asynchronous interconnection of the two AC sub-systems then each AC subsystem requires its own slack bus.

The active and reactive power flows are given on Fig. 3 where it is shown that the equivalent generators connected to buses 1 and 6 contribute 2.2822 p.u. and 0.5172 p.u. of active power, respectively. The voltage magnitudes at all seven buses are treated as voltage controlled nodes by appealing to the voltage regulating capabilities of the two generators, the two LTC transformers and the two VSCs. The phase angles are initialized at 0 in all seven buses. Buses 1 and 6 are designated to be the two Slack buses of this asynchronous interconnection and Bus 0 is a DC-like bus. The phase angle voltage at bus 1 provides a reference for the phase angle voltages at buses 2 and 3 whereas the phase angle voltage at bus 6 is the reference for the phase angle voltages at buses 4 and 5. The voltage solution is given in Table 1.

The active power loss incurred in the VSC connected to bus 3 stands at 1.43% with 0.99% due to switching losses and the rest due to conduction losses – the switching loss is represented by an initial equivalent conductance,  $G_0$ , of 1%. It delivers 1.8780 p.u. of reactive power to supply the reactive power load of 0.5 p.u. connected at bus 2; with 0.6355 p.u. being absorbed by the Slack generator at node 1 and the remaining going to satisfy the reactive power loss incurred by the transmission line connected between nodes 1 and 2 and LTC 1, which stands at 0.7425 p.u.

The active power loss incurred in the VSC connected to bus 4 stands at 0.44%. Switching losses are 0.30% and conduction losses of 0.14%. These power losses are smaller than those of VSC 1 since there is less energy in this part of the network. It delivers 0.6131 p.u. of reactive power to supply the reactive power load of 0.5 p.u. at bus 5 and the reactive power loss of transformer 2. The Slack generator at node 6 absorbs 0.0717 p.u. of reactive power – this being contributed almost in an equal measure by the rectifier VSC and the transmission line connected between nodes 5 and 6.





The complex and real taps corresponding to the two VSCs and the two LTCs, respectively, are given in Table 2. VSC 1 and VSC 2 are used to regulate voltage magnitudes at buses 3 and 4 at 1.01 p.u. with actual amplitude modulation indexes  $m_{aR}$  and  $m_{aI}$  of 0.838 and 0.831, respectively. Likewise, LTCs 1 and 2 are used to regulate voltage magnitudes at buses 2 and 5 at 1 p.u. with resulting taps  $T_1 = 1.1105$  and  $T_2 = 0.9768$ , respectively.



The equivalent susceptances of VSC 1 and 2 produce 1.9226 p.u. and 0.6383 p.u. of reactive power. The solution converges in 7 iterations to a mismatch tolerance of  $10^{-12}$ .

# *E. Comparison of the new back-to-back VSC-HVDC model with conventional models*

For the sake of completeness, the test case in Section *D* is now solved using two alternative modeling solutions and contrasted with the new model put forward in this paper. The first option relates to a situation where the rectifier bus 3 and the inverter bus 4 are both assumed to be *PV-*type buses, i.e., the actual back-to-back VSC-HVDC model is removed from the diagram. The voltage magnitude at both buses is set at 1.01 p.u. Since this is a case where the VSC-HVDC is assumed to incur no power loss then 1 p.u. active power leaves the rectifier bus and 1 p.u. active power is injected into the inverter bus. Notice that with the VSC-HVDC link removed, we end up with two unconnected AC subsystems. Table 3 presents a summary of the power losses incurred by using this modeling option.

A fuller alternative than the *PV*-type models but still more constrained than the new VSC-HVDC model put forward in this paper, is to represent both converter stations by controllable voltage sources behind the corresponding converters' impedances [4]. Such a model yields a closer modeling flexibility to that afforded by the new VSC-HVDC model but for its lack of proper DC circuit representation. More specifically, the DC voltage, the amplitude modulation ratio and the switching power loss are missing in the equivalent voltage sources model. Nonetheless, its numerical accuracy and modeling flexibility is much closer than that afforded by the *PV*-type model. Table 3 presents a summary of the power losses incurred by the three modeling options, where the difference in the calculated active power losses is clear.

TABLE 3 A SUMMARY OF POWER LOSSES INCURRED BY THE VARIOUS MODELS

Model	Active power losses (MW)			Reactive power losses (MVAR)		
	АC	AC,	<i>VSC-HVDC</i>	АC	AC,	<i>VSC-HVDC</i>
PV buses	26.36	27	N/A	72.83	4.13	N/A
<b>Sources</b>	26.49	.28	0.57	73.27	4.13	5.74
New model	26.79	29	1.87	74.25	4 14	5.80

This is a highly regulated test system and, as expected, the power flow solutions differ little from one another, except for the power losses in the converters which the *PV*-type modeling option is unable to take into account. However, if different operational conditions prevail and the requirement is to relax some of the control variables, say, the amount of power flowing through the VSC-HVDC link then application of the model based on *PV*-type buses becomes theoretically infeasible. In such a case, only the model based on the use of equivalent voltage sources or the new VSC-HVDC model may be used but the latter will yield a better estimate of power losses.

# IV. POWER FLOW MODEL: POINT-TO-POINT VSC-HVDC

The nodal power equations developed for the VSC in Appendix A are used here to represent one of the two VSC-HVDC converters, say the rectifier. However, a new model must be derived for the other VSC-HVDC converter, say the inverter. The model derived in this section comprises the VSC model in Appendix A in series with a DC cable where the common point of connection of these two

elements is mathematically eliminated. This is so because of the inherent difficulties found in the power flow Newton-Raphson method to carry out the so-called remote control.

# *A. Combined VSC-DC Cable Representation*

The fundamental frequency operation of a combined VSC and a cable impedance (resistance), shown schematically in Fig. 4 (a), may be represented by combining the simple cable susceptance model shown in Fig. 4 (b) and the VSC model, derived in Appendix A and shown in Fig. 4 (c).



Figure 4. (a) VSC-DC cable schematic representation; (b) cable equivalent circuit; (c) VSC equivalent circuit

The VSC admittance matrix equation (4), with changed subscripts to represent the inverter, and that of a DC cable:

$$
\begin{pmatrix}\n\overline{I}_{0l} \\
\overline{I}_{0R}\n\end{pmatrix} = \begin{pmatrix}\n\overline{Y}_{DC} & -\overline{Y}_{DC} \\
-\overline{Y}_{DC} & \overline{Y}_{DC}\n\end{pmatrix} \begin{pmatrix}\n\overline{V}_{0l} \\
\overline{V}_{0R}\n\end{pmatrix}
$$
\n(15)

are combined to yield the compound representation below,

$$
\begin{pmatrix}\n\overline{I}_{vl} \\
\overline{I}_{0l} \\
\overline{I}_{0R}\n\end{pmatrix} = \begin{pmatrix}\n\overline{Y}_{1} & -m_{al}^{2} \angle \phi_{I} \overline{Y}_{1} & 0 \\
-m_{al}^{2} \angle -\phi_{I} \overline{Y}_{1} & m_{al}^{2} (\overline{Y}_{1} + jB_{eq}) + G_{sw} + \overline{Y}_{DC} & -\overline{Y}_{DC} \\
0 & -\overline{Y}_{DC} & \overline{Y}_{DC}\n\end{pmatrix}\n\begin{pmatrix}\n\overline{V}_{vl} \\
\overline{V}_{0l} \\
\overline{V}_{0R}\n\end{pmatrix}
$$
\n(16)

Mathematical elimination of node 0I, yields,

$$
\left(\overline{I}_{st}\right) = \frac{1}{m_{at}^2\left(\overline{Y}_1 + jB_{\alpha}\right) + G_{sw} + \overline{Y}_{bc}} \left(\overline{Y}_1\left((G_{sw} + jm_{a}^2 B_{\alpha}\right) + \overline{Y}_{bc}\right)
$$
\n
$$
- m_{at}^2 \angle - \phi_t \overline{Y}_1 \overline{Y}_{bc}
$$
\n
$$
- m_{at}^2 \angle \phi_t \overline{Y}_1 \overline{Y}_{bc}
$$
\n
$$
\overline{Y}_{bc}(m_{at}^2 \overline{Y}_1 + (G_{sw} + jm_{a}^2 B_{\alpha})) \left(\overline{V}_{as}\right)
$$
\n(17)

It should be noted that tor the sake of generality, the DC cable parameter has been taken to be an admittance.

#### *B.Point-to-Point VSC-HVDC Nodal Power Equations*

The complex power model is derived similarly to eq. (5) but making use of the nodal matrix eq. (17). Following some arduous algebra, the following active and reactive power expressions are arrived at:

$$
P_{u} = G_{\alpha_{1}}V_{u}^{2} - m'_{al}V_{u}V_{0R} \Big[ G_{\alpha_{1}D C} \cos(\theta_{u} - \theta_{0R} - \phi_{I}) + B_{\alpha_{1}D C} \sin(\theta_{u} - \theta_{0R} - \phi_{I}) \Big] \nQ_{u} = -B_{\alpha_{1}}V_{u}^{2} - m'_{al}V_{u}V_{0R} \Big[ G_{\alpha_{1}D C} \sin(\theta_{u} - \theta_{0R} - \phi_{I}) - B_{\alpha_{1}D C} \cos(\theta_{u} - \theta_{0R} - \phi_{I}) \Big] \nP_{0R} = G_{\alpha_{0}}V_{0R}^{2} - m'_{al}V_{u}V_{0R} \Big[ G_{\alpha_{1}D C} \cos(\theta_{0R} - \theta_{u} + \phi_{I}) + B_{\alpha_{1}D C} \sin(\theta_{0R} - \theta_{u} + \phi_{I}) \Big] \nQ_{0R} = -B_{\alpha_{0}}V_{0R}^{2} - m'_{al}V_{u}V_{0R} \Big[ G_{\alpha_{1}D C} \sin(\theta_{0R} - \theta_{u} + \phi_{I}) - B_{\alpha_{1}D C} \cos(\theta_{0R} - \theta_{u} + \phi_{I}) \Big]
$$
\n(18)

where

$$
G_{\varphi_{1}} = \frac{1}{\Delta} \Big[ (m_{a}^{2}G_{1} + G_{\infty} + G_{bc}) \Big\{ G_{1}(G_{\infty} + G_{bc}) - B_{1}(m_{a}^{2}B_{\varphi_{1}} + B_{bc}) \Big\} + (m_{a}^{2}(B_{1} + B_{\varphi_{1}}) + B_{bc}) \Big\{ B_{1}(G_{\infty} + G_{bc}) + G_{1}(m_{a}^{2}B_{\varphi_{1}} + B_{bc}) \Big\} \Big]
$$
  
\n
$$
B_{\varphi_{1}} = \frac{1}{\Delta} \Big[ (m_{a}^{2}G_{1} + G_{\infty} + G_{bc}) \Big\{ B_{1}(G_{\infty} + G_{bc}) + G_{1}(m_{a}^{2}B_{\varphi_{1}} + B_{bc}) \Big\} - (m_{a}^{2}(B_{1} + B_{\varphi_{1}}) + B_{bc}) \Big\{ G_{1}(G_{\infty} + G_{bc}) - B_{1}(m_{a}^{2}B_{\varphi_{1}} + B_{bc}) \Big\} = \frac{1}{\Delta} \Big[ (m_{a}^{2}G_{1} + G_{\infty} + G_{bc}) (G_{1}G_{bc} - B_{1}B_{bc}) + (m_{a}^{2}(B_{1} + B_{\varphi_{1}}) + B_{bc}) (B_{1}G_{bc} + G_{1}B_{bc}) \Big]
$$
  
\n
$$
B_{\varphi_{1DC}} = \frac{1}{\Delta} \Big[ (m_{a}^{2}G_{1} + G_{\infty} + G_{bc}) (B_{1}G_{bc} + G_{1}B_{bc}) - (m_{a}^{2}(B_{1} + B_{\varphi_{1}}) + B_{bc}) (G_{1}G_{bc} - B_{1}B_{bc}) \Big]
$$
  
\n
$$
G_{\varphi_{0}} = \frac{1}{\Delta} \Big[ (m_{a}^{2}G_{1} + G_{\infty} + G_{bc}) \Big\{ G_{bc}(m_{a}^{2}G_{1} + G_{\infty}) - m_{a}^{2}B_{bc}(B_{1} + B_{\varphi_{1}}) \Big\} + (m_{a}^{2}(B_{1} + B_{\varphi_{1}}) + B_{bc}) \Big\{ B_{bc}(m_{a}^{2}G_{1} + G_{\infty}) + m_{a}^{2}G_{
$$

# *C.Point-to-Point VSC-HVDC Linearised System of Equations*

The numerical solution of the point-to-point VSC-HVDC link involves the combined solution of equations (6) and (18), for a pre-defined set of generation and load pattern. The former set may represent the rectifier and the latter set the inverter. These equations are non-linear and their solution may be carried out very efficiently using the Newton-Raphson method, which implies a linearisation process similar to the one carried out for the back-to-back VSC-HVDC model in Section III.*B*.

# *D. Point-to-Point VSC-HVDC Test Cases*

The test case in this section relates to a simple system where the VSC-HVDC link is used to interconnect two otherwise independent AC systems, as shown in Fig. 5.



Figure 5: Point-to-point VSC-HVDC linking two equivalent AC sub-systems. The following parameters are used: (i) Transmission Line 1 and 2:  $R_{TL}=0.05$  p.u. and  $X_{TL}$ =0.10 p.u.,  $B_{TL}$ =0.06 p.u.; (ii) VSC 1 and VSC 2 series resistance and reactance: 0.001 p.u., 0.01 p.u.; (iii) VSC 1 and VSC 2 initial shunt conductance for switching loss calculation  $G_{\text{sw}}$  = 0.01 p.u.; (iv) LTC 1 and LTC 2 series reactances: 0.06 p.u.; (v) active and reactive power load at bus 2: 1 p.u. and 0.5 p.u.; (vi) active and reactive power load at bus 5: 1.5 p.u. and 0.5 p.u.; (vii) resistance of DC cable: 0.05 p.u.

The rectifier is connected between buses 3 and 0*R*, the inverter is connected between buses 4 and 0*I* and the DC cable is connected between DC buses 0*R* and 0*I*. For the purpose of the iterative voltage solution, bus 0*I* is not represented explicitly. Instead, the nodal voltage and power existing at bus 0*I* is calculated quite straightforwardly once the iterative voltage solution has converged.

Similarly to the back-to-back VSC-HVDC case, bus 0*R* is treated as a PV-type node and regulated at  $\sqrt{2}$  p.u. The power leaving the rectifier is set at 1 p.u. The inverter and rectifier are set to regulate voltage magnitude at 1.01 p.u. at Bus 3 and 4, respectively, whereas the voltage magnitudes at buses 2 and 5 are both regulated at 1 p.u. using LTC 1 and LTC 2, respectively.

Buses 1 and 6 are taken to be the two Slack buses of this asynchronous interconnection and bus 0*R* and 0*I* are DC-like buses. The phase angle at bus 1 provides a reference for the phase angles at buses 2 and 3 whereas the phase angle at bus 6 provides a reference for the phase angles at buses 4 and 5. The full voltage solution is given in Table 4.



The solution converges in 7 iterations to a mismatch tolerance of  $10^{-12}$ , where the nodal voltage at Bus 0*I* is calculated upon convergence of the iterative solution. The active and reactive power flows are given on Fig. 5 where the generators connected to buses 1 and 6 contribute 2.2822 p.u. and 0.5434 p.u. of active power, respectively. Power regulation at the DC output of the rectifier was set at 1 p.u.

As expected, all results relating to nodal voltages, power flows and tap value, comprising buses 1 to 0*R* do not change compared to those obtained for the case of the back-to-back

VSC-HVDC, since the power constraint at Bus 0*R* decouples the power flow solution of the two circuits to the left and to the right of Bus 0*R*. Changes in the solution do occur for the circuit connected to the right of Bus 0*R* since less active power from Slack Generator 1 arrives to the load connected to Bus 5, due to the power loss incurred in the DC resistance. Hence, the Slack Generator at Bus 6 provides additional power to satisfy the demand of 1.5 p.u. active power at Bus 5. The amplitude modulation ratios and taps for the two VSCs and the two LTCs, respectively, are given in Table 5. TABLE 5



The power loss analysis for the power circuit to the left of Bus 0*R* is the same as that existing in the back-to-back VSC-HVDC case, but changes do take place for the circuit to the right of Bus 0*R*. For instance, the active power loss incurred in the VSC connected to bus 4 stands at 0.41% with 0.276% due to switching losses and 0.134% due to conduction losses. The power loss in the DC cable is 2.5%. The VSC 2 delivers 0.6252 p.u. of reactive power to supply the reactive power load of 0.5 p.u. connected at bus 5. It also caters for the reactive power loss of LTC 2 and together with reactive power generated by the transmission line connected between nodes 5 and 6, injects 0.0827 p.u. of reactive power into the slack generator at Bus 6.

# *E.Comparison of the new point-to-point VSC-HVDC model with conventional models*

Similarly to the numerical exercise carried out in Section *III. E*, where the new back-to-back VSC-HVDC model and two conventional models are compared in terms of their power loss representation, the point-to-point VSC-HVDC model is addressed in this section. However, use of the *PV-*type bus concept to represent the rectifier bus and the inverter bus is not an option since the power loss in the DC link cannot be determined a *priori*.

Hence, the new point-to-point VSC-HVDC model is compared only against an equivalent voltage sources model  $[6]$  – one that represents the AC circuit correctly but where the DC circuit does not exist explicitly. Table 6 presents a summary of the power losses incurred by the two modeling options.





The active and reactive power losses in AC systems 1 and 2 calculated by the two models differ little. This is an expected result since both VSC-HVDC models represent well the AC system but the difference lies in the power losses associated with the VSC-HVDC since the equivalent voltage sources model lacks proper DC representation; in particular, switching loss representation, with the associated impact shown in the column corresponding to the MW VSC-HVDC. The new model yields a more realistic result not only because of the incorporation of switching losses but also because of a more accurate representation of the DC voltages than in [6] and with it, a more accurate DC current representation.

# V.CONCLUSIONS

A new model suitable for assessing the fundamental frequency operation of VSC-HVDC links using Newton-Raphson power flows solutions has been introduced. The back-to-back and the point-to-point configurations have received attention. This model represents a paradigm shift in the way the fundamental frequency, positive sequence modeling of VSC-HVDC links is carried out. The new model does not treat the rectifier and inverter stations as idealized controllable voltage sources but rather as compound transformer devices with which key control properties of PWM-based inverters may be linked – just as DC-to-DC converters have been linked, conceptually speaking, to step-up and step-down transformers [12]. The phase angle of the complex tap changer represents the phase shift that would exist in a PWM inverter. More specifically, this would be the phase angle required by the VSC to enable either reactive power generation or absorption purely by electronic processing of the voltage and current waveforms within the VSC. The switching and ohmic losses are all explicitly represented in the new VSC-HVDC model. Comparisons with available models show that the new model yields similar results to a model based on the use of equivalent voltage sources when no switching losses are included in the new model. However, switching power losses do exist in practical VSCs and only the new VSC-HVDC model caters for such losses, hence, the two VSC-HVDC models yield different amount of power loss when realistic conditions are taken into account. Comparisons were also made against a model where the VSC-HVDC link is represented as two *PV*-type nodes at its connecting nodes with the two AC sub-systems. The 9

limitations of this rather contrived VSC-HVDC representation are too many to be of any practical use in light of the two more advanced VSC-HVDC representations already in existence. Concerning reliability towards the convergence, all three VSC-HVDC models converge equally reliable – they exhibit quadratic convergence characteristics. The model has been tested in a simple system for ease of reproduction by interested parties.

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#### APPENDIX A: BASIC VSC MODEL

The nodal admittance equations representing the fundamental frequency operation of the VSC, shown schematically in Fig. 2(b), is developed below using first principles. Key assumptions in the derivation of the VSC model are that the tap magnitude  $m'_a$  is an equivalent amplitude modulation coefficient of the actual VSC and that its phase angle  $\phi$  is the phase angle of the complex voltage  $\overline{V}_1$ . The two resistive components representing the VSC's internal loss are placed one in series and the other one in shunt. The former is associated with the ohmic loss which is proportional to the AC terminal current squared and the latter yields a power loss for the switching action of PWM converter. The first term is placed on the primary side of the equivalent tap-changing transformer, together with the inductor representing the interface magnetics, and the second term is placed in parallel with the DC bus. The rating of the DC capacitor is quite small; it normally stands at about

10% of the total reactive power capacity of the VSC.

In a phase-shifting transformer the relationship between the voltage tap and the current tap is a complex conjugate one,

$$
\overline{T}_V = \overline{T}_I^*
$$
 (A.1)

Hence, in connection with Fig. 2(b), the voltage and current relationships in the ideal tap-changing transformer are:

$$
\frac{\overline{V}_1}{V_0} = \frac{m'_a \angle \phi}{1} \text{ and } \frac{m'_a \angle -\phi}{1} = \frac{I_2}{\overline{I}_1 - \overline{I}'_1} \tag{A.2}
$$

where  $\overline{T}_V = m'_a \angle \phi$  and  $\overline{T}_I^* = m'_a \angle -\phi$ .

The current through the admittance connected between *vR* and 1 is:

$$
\overline{I}_1 = \overline{Y}_1 (\overline{V}_{vR} - \overline{V}_1) = \overline{Y}_1 \overline{V}_{vR} - m'_a \angle \phi \overline{Y}_1 V_0 = \overline{I}_{vR} \quad (A.3)
$$

where  $Y_1 = 1/(R_1 + jX_1)$ . At node 0, the following relationship holds:

$$
\overline{I}_0 = -I_2 + I'_2 = -m'_a \angle -\phi(\overline{I}_1 - \overline{I'}_1) + G_{sw}V_0
$$
  
=  $-m'_a \angle -\phi\overline{Y}_1\overline{V}_{vR} + G_{sw}V_0 + m'_a(\overline{Y}_1 + jB_{eq})V_0$  (A.4)

Combining equations (A.3) and (A.4) yields:

$$
\overline{I}_{vR} = \overline{Y}_1 \overline{V}_{vR} - m'_a \left( \cos \phi + j \sin \phi \right) \overline{Y}_1 V_0
$$
\n
$$
\overline{I}_0 = 0 = -m'_a \left( \cos \phi - j \sin \phi \right) \overline{Y}_1 \overline{V}_{vR} + G_{sw} V_0 + m'_a \left( \overline{Y}_1 + j B_{eq} \right) V_0
$$
\n(A.5)







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