Open and Short-Circuit Switch Fault Diagnosis for Non-Isolated DC-DC Converters Using Field Programmable Gate Array

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Abstract— **Fault detection (FD) in power electronic converters is necessary in embedded and safety critical applications to prevent further damage. Fast FD is a mandatory step in order to make a suitable response to a fault in one of the semiconductor devices. The aim of this study is to present a fast yet robust method for fault diagnosis in non-isolated DC-DC converters. FD is based on time and current criteria which observe the slope of the inductor current over the time. It is realized by using a hybrid structure via coordinated operation of two FD subsystems that work in parallel. No additional sensors, which increase system cost and reduce reliability, are required for this detection method.**

For validation, computer simulations are first carried out. The proposed detection scheme is validated on a boost converter. Effects of input disturbances and the closed-loop control are also considered. In the experimental set-up, a Field Programmable Gate Array (FPGA) digital target is used for the implementation of the proposed method, to perform very fast switch FD. Results show that with the presented method, FD is robust, and can be done in a few microseconds.

Index Terms— **DC-DC power converters, Digital control, Fault detection (FD), Fault diagnosis, Field Programmable Gate Arrays (FPGA), Power semiconductor switches, Switched-mode power supply.**

NOMENCLATURE

D	Duty cycle
e_o	Capacitor stored energy
i_L	Inductor current
IGBT	Insulated Bipolar Transistor
N	Threshold of fault detection (FD) in FD1
q	Switching command

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T_c	Sampling period
T_d	Total inherent delay
t_{det}	Total detection time
T_{OCF}	Open circuit fault occurrence time
T_{SCF}	Short circuit fault occurrence time
T_s	Switching period
V_o	Output voltage

I. INTRODUCTION

DC-DC power converters are widely used in a variety of applications including aerospace, ships, electric vehicles and renewable energy power systems. In such embedded or safety critical applications, a high level of system reliability is mandatory. The two most critical elements in DC-DC converters are aluminum electrolytic capacitors and semiconductors. More than 50% of malfunctions and breakdowns are reported to be due to aluminum electrolytic capacitor failures and 30% due to power semiconductor failures [1]. Several works have been reported in the literature on FD of aluminum electrolytic capacitors in different applications [1]. This paper focuses on power electronics switch failures.

Several papers have studied FD methods in power electronic converters [2]-[10]. FD in a multilevel converter is studied in [2], [3]. A detection method for faults in IGBT switches based on gate signal monitoring is presented in [4]. Open-circuit faults (OCF) in matrix converters are studied in [5], [6]. Nonlinear observers are used in [7] to detect open-circuit switch faults in induction motor drives. Another method for the detection of open-switch faults in voltage source inverters feeding AC drives, based on analyzing the load currents, is presented in [8]. A fast FPGA-based FD based on a simultaneous "time and voltage criteria" for two-level converters is proposed in [9].

Although most of the previously cited research deals with AC-DC or AC-AC converters, an increasing number of recent papers are focused on fault diagnosis in DC-DC converters. Fault diagnosis in the power conversion stage of a grid-connected photovoltaic system is studied in [10]. Open circuit fault detection in an isolated full bridge converter is presented in [11]. A FD method for a three-level DC-DC converter is presented in [12] which is based on the monitoring of the flying capacitor voltage. Application of Kalman filters in model based fault diagnosis of a DC-DC boost converter is

studied in [13]. Another diagnosis method based on harmonic components of the magnetic near field of a DC-DC converter is presented in [14]. In [15], switch faults are detected in a boost converter by comparing the duty cycle and inductor current sloop. In this method three switching periods are needed for FD.

Once the fault has been detected, the stoppage of the converter must be avoided. To ensure continuity of service, a fault-tolerant DC-DC converter topology must be used. Several approaches are presented in the literature for fault-tolerant DC-DC converters, based on redundancy, reconfiguration or modularity. Reconfiguration is proposed in [15] in a fault-tolerant power conversion system for a hybrid electric vehicle. Ambusaidi et al. have proposed a fault-tolerant DC-DC converter topology based on redundancy [16]. A fault tolerant modular DC-DC converter is proposed in [17].

This paper, an effective FPGA-based method is presented for very fast switch fault diagnosis in non-isolated DC-DC converters operating in Continuous Current Mode (CCM). This concerns both open-circuit and short-circuit faults (SCF). The proposed approach is based on the monitoring of the inductor current. Fault is detected using a hybrid structure via coordinated operation of two FD subsystems. No additional sensors are used, as the inductor current has to be normally measured for control purposes. By avoiding additional sensors, cost is not increased and overall system reliability is maintained.

In order to perform very fast FD, the proposed algorithm must be implemented on a very fast digital target. On the other hand, fault diagnosis must be executed in parallel with other control tasks. Thanks to its parallel architecture, FPGA can run these tasks very quickly; as a result, it appears to be the most suitable choice for the implementation of such switch FD schemes. Moreover, high performance of FPGA for many power electronic and drive applications has been proved [18]. Also, by implementing both fault diagnosis and converter control units on a single FPGA chip, the system cost will be decreased and required interfaces will be minimized. An Altera Stratix family FPGA chip is used to perform the proposed FD method in addition to the control of the converter. The FPGA implementation procedure is based on a methodology for rapid prototyping, detailed in [19]. Experimental tests are also carried out to validate the effectiveness of this method.

In the following, the studied DC-DC converter and its control scheme are reviewed briefly in section II. The proposed FD method is presented in section III. Simulation results are presented in section IV. The full experimental results are provided in section V. Both simulation and experimental results confirm the effectiveness of the proposed fault detection method. It is shown that using this method, switch fault diagnosis may be performed in only 20μs, while this value is only restricted by the natural delays in the system. However, in the worst cases two switching periods are needed for fault diagnosis.

II. SINGLE-ENDED NON-INSOLATED DC-DC CONVERTERS: OPERATION AND CONTROL

A. Single-Ended Non-insolated DC-DC converters

Several topologies of DC-DC converters are used in classical power electronic applications. In this paper, a very fast switch fault diagnosis method is proposed, dedicated to one family of DC-DC converters, called "non-isolated single-ended DC-DC converters". Fig. 1 summarizes this family that consists of buck, boost, buck-boost, Ćuk, SEPIC (Single-Ended Primary Inductor Converter), and dual SEPIC converters.

These converters are increasingly being used in industrial applications. Among their vast range of applications one can mention electric traction, electric vehicles, renewable DC sources, machine tools, and power factor correction (PFC) applications. Some other applications are in distributed DC systems in ships, airplanes, computers and in telecommunications [20]-[22].

Most of the previously cited applications are either embedded or safety critical ones for which switch fault diagnosis is of major interest.

As shown in Fig. 1, in non-isolated single-ended DC-DC converters, the shape of the inductor current (i_L) is the same. Because of this similarity, the proposed fault detection method studied in this paper is applied to the particular case of a boost converter and can be generalized to the other mentioned topologies.

B. Converter operation modes

There are two modes in one switching period in the boost converter operating in CCM. Mode 1 starts when the switch S is turned on as illustrated in Fig.2 (a). In this mode, the diode is reverse biased and is off. During DT_s the input voltage is applied across the inductor, where T_s is the switching period and D is the duty ratio. Consequently, the inductor current i_L ramps up linearly (ignoring the effect of r_L,) increasing the energy stored in the inductor. During this mode q=1.

Mode 2 begins when the switch S is turned off. The simple equivalent circuit is shown in Fig. 2 (b). During $(1-D)T_s$, the stored energy in the inductor flows to the load and forces the diode to conduct. As a result the inductor current i_L decreases. During this mode is q=0.

This common inductor current shape in single-ended dc-dc converters is considered in the proposed fault diagnosis.

C. Control of the converter

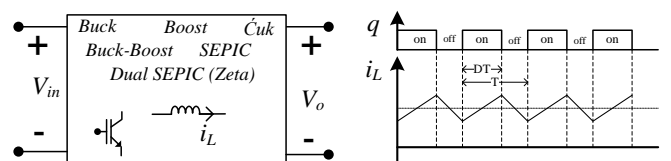The studied system consists of an AC three-phase source, a

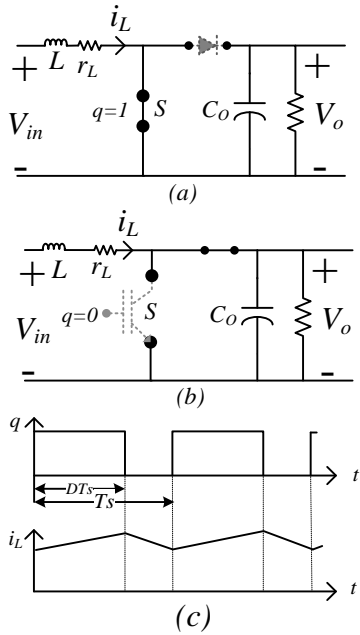Fig.1. Single-ended DC–DC non-isolated converters.

Fig. 2. (a) Boost converter in mode 1; (b) Boost converter in mode 2; (c) Signals for a boost converter in mode 1 and mode 2.

three-phase diode rectifier, a boost converter and a resistive load, as shown in Fig. 3.

Here, for the control, instead of controlling the output voltage v_o directly, the stored energy in the output capacitor (e_o) is controlled. This change of variable simplifies the synthesis of the v_o controller.

A Proportional Integral (PI) controller is employed to regulate e_o (and indirectly the output voltage) according to its reference (e_{oref}) as is illustrated in Fig. 3. The output of this PI controller is the inductor current reference (i_{Lref}). An intern loop is used for the control of this current. A second PI controller is used in this loop. Finally, q is produced by a Pulse Width Modulation (PWM) block, as shown in Fig. 3.

III. SWITCH FAULT DIAGNOSIS

A. Switch faults

The most common failures in semiconductors are short-circuit faults, gating faults and open-circuit faults [23]-[25]. These failures may happen due to external or internal events, for example:

1) Incorrect gate voltage,
2) Lifting of bonding wires due to thermal cycling,
3) Driver failure,
4) Rupture of the switch which can be a consequence of a short-circuit fault,
5) Electrical over stress (voltage or current) which may appear by electromagnetic pulses, electrostatic discharge, system transient and lightning [23]-[25].

In practice, open-circuit faults may be a consequence of a short-circuit or a gating fault. In this paper, we consider both open and short-circuit faults.

The proposed switch fault diagnosis is based on two algorithms that consider the shape of the inductor current to detect an open-circuit fault or short-circuit fault in a switch (Fig. 4). The primary algorithm (so called FD1) is faster than the secondary one (FD2) but it is less robust at detecting an OCF for small values of D and at detecting a SCF for large values of D or in high frequency switching cases. The secondary algorithm is more robust and efficiently detects faults in any conditions, but it is not as fast as the primary algorithm. It can be said that the secondary algorithm acts as a backup fault diagnosis. Both algorithms are described in the following.

B. Primary algorithm (FD1)

As shown in Fig.5, turning on the switch S increases the inductor current i_L. Consequently, the sign of the slope of i_L remains positive during this time interval (DT_s). Fig. 4 presents the general scheme of the proposed fault diagnosis. In subsystem FD1, the inductor current (i_L) passes through a derivation block and then through a sign block which computes sgn di/dt. If i_L increases, sgn di/dt =1 and if i_L decreases sgn di/dt =-1. The calculated error signal is equal to 1 when the estimated and measured current slopes are different. If there is no switch failure, the two signals sgn di/dt and $S_{q'}$ have the same values, then the signal "error" is equal to 0, as described in

$$\begin{cases} \begin{cases} sgn_{\frac{di}{dt}} = 1 \\ S_{q'} = 1 \end{cases} & t \in [0, DT_s] \\ \begin{cases} sgn_{\frac{di}{dt}} = -1 \\ S_{q'} = -1 \end{cases} & t \in [DT_s, T_s] \end{cases} \xrightarrow[normal\ condition]{} error = 0 \quad (1)$$
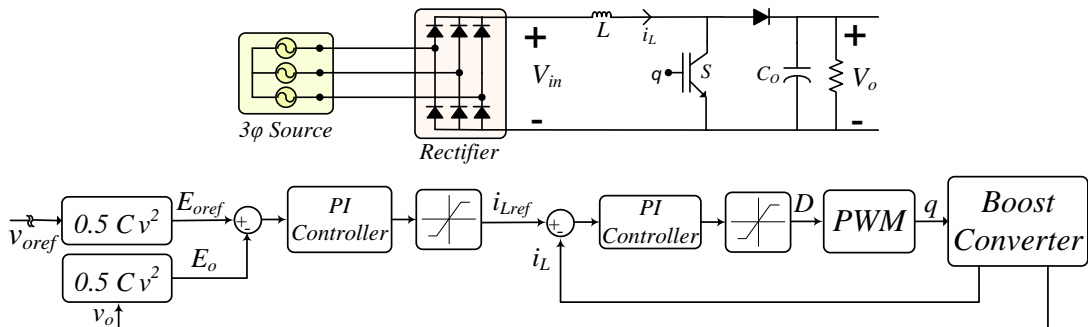

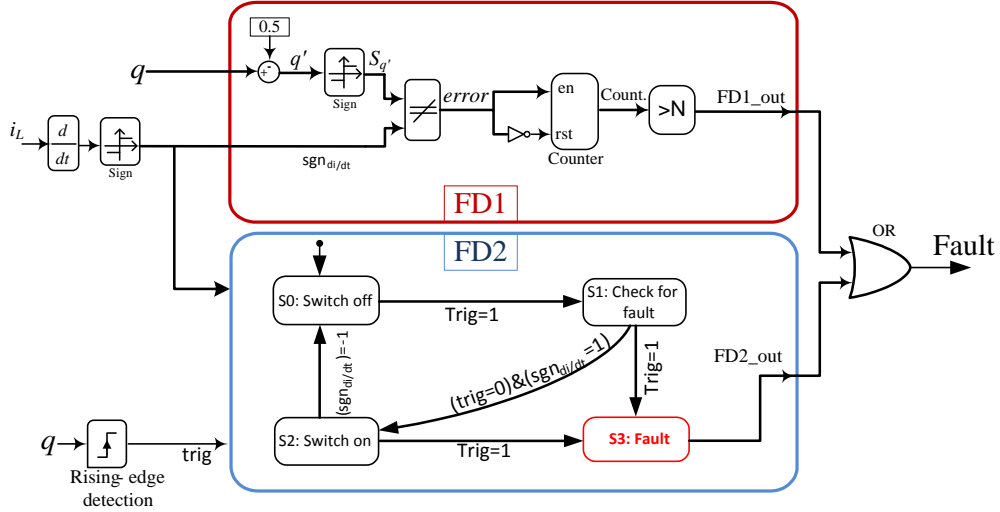Fig. 3. Studied system and its control loops.

Fig. 4. Switch fault diagnosis based on FD1 and FD2 algorithms

$S_{q'}$ is the sign of the signal q', which is in turn equal to:

$$q' = q - 0.5 \qquad (2)$$

It is noticeable that, as a result of non-ideal behavior of power switches, delays and dead times are inevitable. Therefore, as shown in Fig. 5, even in the normal operation of the converter, *sgn di/dt* will be delayed in respect to q and $S_{q'}$, and hence the error signal will be momentarily unequal to zero. That is why a time criterion is employed to take into account for these delays and dead times. Here the signal "error" is observed, and if it always remains in state "1" for a long enough time (N observation periods equal to NT_c, where T_c is the sampling period), then it may be concluded that there
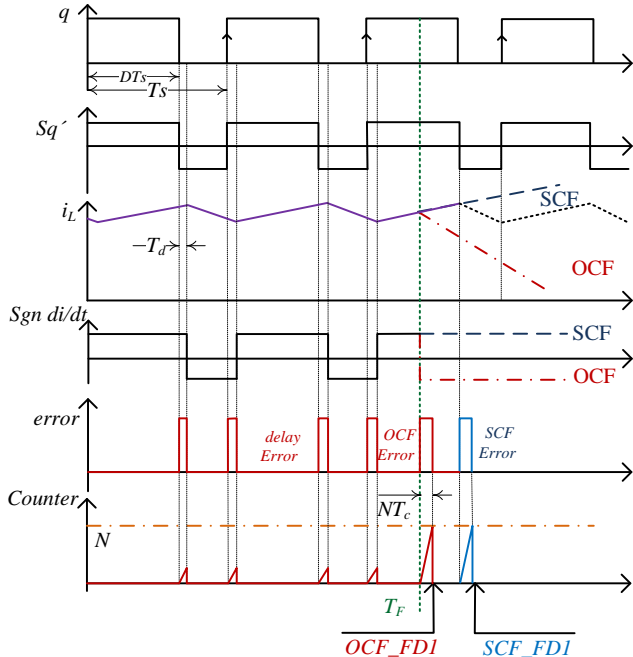

Fig. 5. FD1 algorithm signals.

is a fault. As depicted in Fig. 5, in faulty conditions, the shape of i_L does not correctly follow the switch command. In OCF, i_L decreases and in SCF i_L increases regardless of the switch command. In any case, the error signal will be set to '1' and then the counter starts to count. This mentioned observation time should be longer than the overall delays caused by the sensors, drivers, controllers and switches; otherwise the inherent but normal delay of the system may be interpreted as a fault:

$$N.T_c > T_d \qquad (3)$$

where T_d is the delay between the switching command change and the change of $(sgn \, (di_L/dt))$, known as "total inherent delay". In the studied experimental setup (mentioned in section V), this total inherent delay is about 10 µs. Therefore the observation time (NT_c) is chosen equal to 20 µs.

FD1 algorithm can be very fast and can detect a fault after its occurrence within N sampling period. However, the fault detection time in FD1 depends on several parameters. Let's consider in detail the FD process for an OCF with FD1. Three cases may be considered, based on the fault occurrence moment in a faulty switching period. Fig. 6 shows the first case. The FD signals are shown in two switching periods, where the first one shows the normal operation of the converter, and a fault is occurred in the second period. In this first case, the OCF has occurred in the time interval $[t_1, t_2]$ which is highlighted in the figure. The fault will be detected by FD1 if time criteria is satisfied, i.e., if $DT_s > NT_c$. In this case, thanks to the inherent delays, the counter has already been started to count before OCF has occurred. Then FD1 can detect the OCF in less than the observation time (NT_c), i.e. the detection time is ($NT_c - T_{OCF}$).

The second case is when the fault occurs in the time interval $[t_2, t_3 - NT_c]$. This case is shown in Fig. 7. In this case the fault can be detected by FD1 after N sampling periods (NT_c) if $(DT_s - T_{OCF}) > NT_c$.
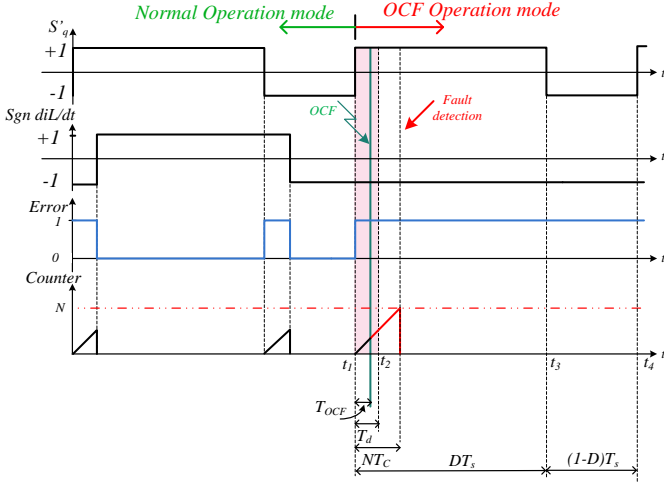
Fig. 6. FD1 algorithm signals - case1: OCF occurs in $[t_1, t_2]$.

Finally, in the third considered case, if the OCF occurs in the time interval $[t_3 - NT_c, t_3]$, the counter output cannot be greater than N before the switching command of the faulty switch changes, thus the fault cannot be detected in the switching period in which the fault is occurred, as shown in Fig. 8. However the fault will be detected in the next switching period, if $DT_S > NT_c$ (this case corresponds to the case 1 with $T_{OCF}=0$).

Therefore, we can summarize FD1 limits for OCF detection as:

$$NT_c > T_d \tag{4}$$
$$T_{OCF} < D \, T_s - N \, T_c \tag{5}$$
$$DT_s > NT_c \tag{6}$$

These three criteria must be entirely satisfied in order to have successful fault detection with FD1. The minimum detection time in this case can be as low as:

$$\text{Min}(t_{\text{det}}) = NT_c - T_d \tag{7}$$

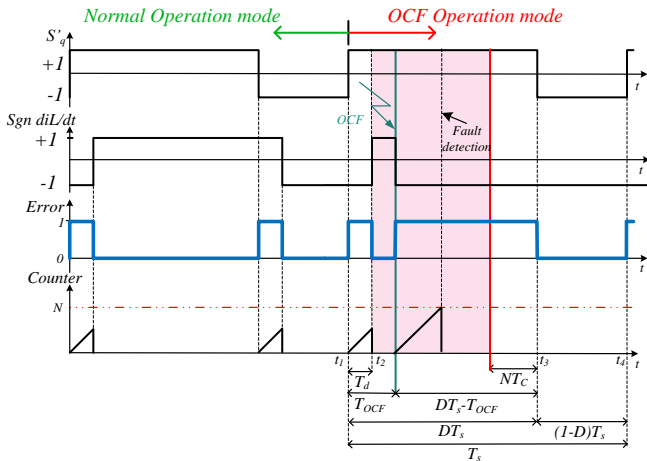when the fault occurs in $[t_1, t_2]$ with $T_{OCF} = T_d$.

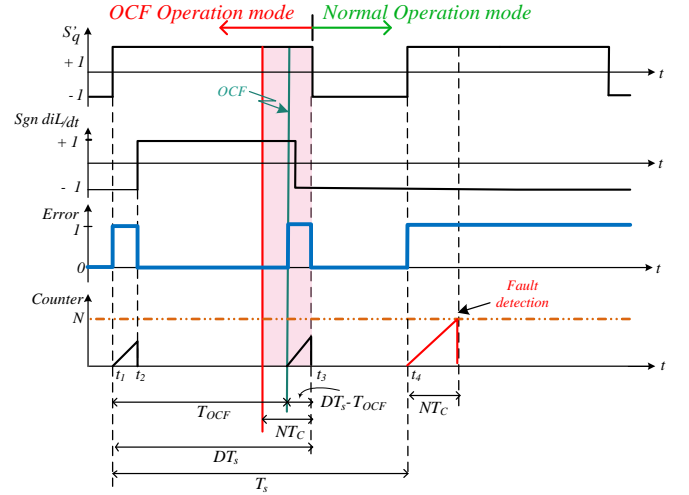Fig. 7. FD1 algorithm signals - case2: OCF occurs in $[t_2, t_3 - NT_c]$.

Fig. 8. FD1 algorithm signals - case3: OCF occurs in $[t_3 - NT_c, t_3]$.

The total detection time is at its maximum value when the fault occurs at $(T_{OCF} = t_3 - (N-1)T_c)$. In this case, FD1 detects the fault in the next switching period, thus the detection time is equal to $(N-1)T_c + (1-D)T_S + NT_c$. This value is at its maximum for $DT_S = NT_C$ and the resulting maximum total detection time is:

$$Max(t_{det}) = T_s + (N-1)T_c \tag{8}$$

This same analysis can be done in case of SCF. Using the same approach, one can conclude that, in case of SCF, FD1 can detect the fault successfully if the three following conditions are simultaneously satisfied:

$$NT_C > T_d \tag{9}$$
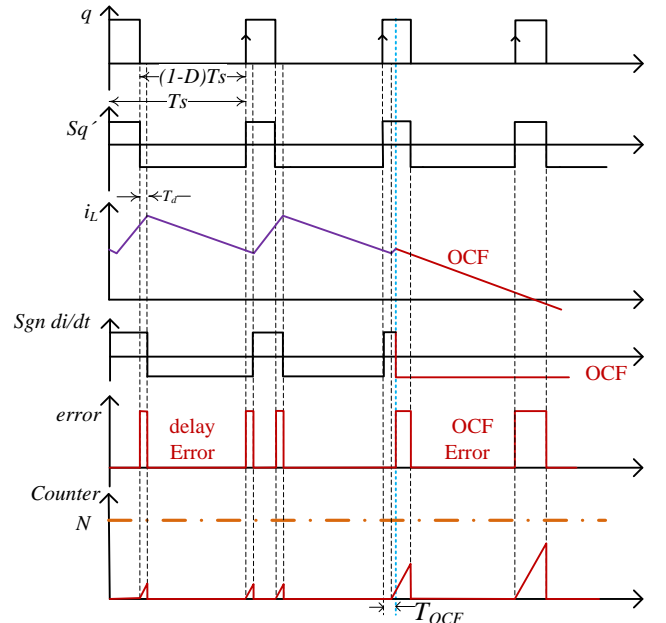$$T_{SCF} < (1-D)T_s - NT_C \tag{10}$$
$$(1-D)T_s > NT_C \tag{11}$$

Fig. 9. Unsuccessful OCF detection by FD1 algorithm when D is small.

Moreover, the minimum and maximum total detection times are the same for OCFs and SCFs.

These analyses describe the functionality of FD1 and show the necessary criteria for successful fault detection with FD1. If these criteria are not entirely satisfied, fault detection will not be possible. For example, for an OCF, considering (5) and (6), it may be seen that for small values of *D* or in high frequency switching, fault detection with FD1 may not be possible. This is shown in Fig. 9. In this case, for a small value of D, the counter could not reach the predefined value of *N* because the value of *Sq'* will change after *DTs* and the error will come back to '0'. For an SCF, it may be concluded from equations (10) and (11) that for a large value of D or a small T_s, the fault cannot be detected with FD1. This is shown in Fig. 10 for a large duty cycle. For this reason, the secondary algorithm FD2 is proposed

C. Secondary Algorithm (FD2)

As described before, there are two operation modes (in CCM) for the conventional boost converter. In the first mode the inductor current increases while in the second it decreases. According to Fig. 10 by each pulse of "Trig" the inductor current i_L increases and then decreases. If i_L is always increasing or decreasing between two Trig signals it can be concluded that a failure has occurred.

As shown in Fig. 4 for fault diagnosis by FD2, a state machine with four states is used. In initial transition (state S0) converter is in mode 2 of operation i.e. q=0, and stays in this state until q=1 and Trig=1; then the transition to state S1 occurs.

In state S1:
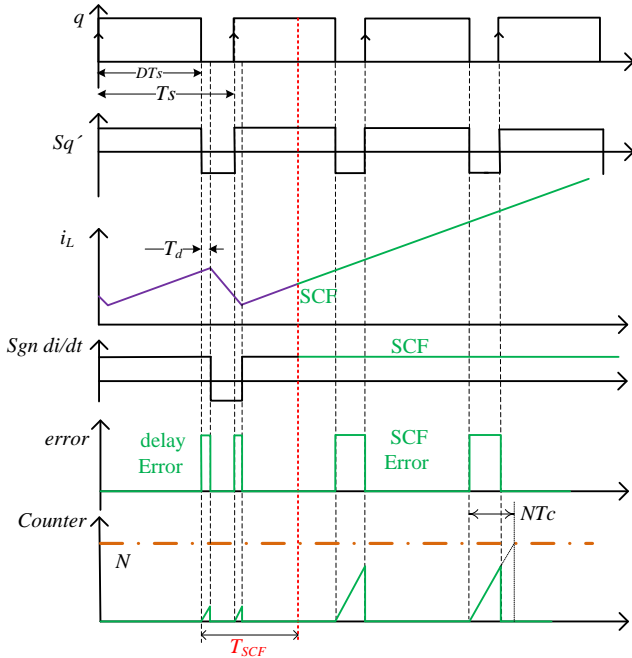1) If no failure has occurred, the switch S is turned on, i_L

V_{in}		50 V
L		3 mH
r_L		0.1 Ω
C		2200 μF
R_L		50 Ω
Switching Frequency		15 kHz
Controller Parameters	K_{peo}	22.5
	K_{ieo}	112.50
	K_{piL}	0.0895
	K_{iiL}	0.8953

increases and *sgn di/dt* =1 thus a transition to state S2 occurs.
2) If an OCF has occurred, i_L decreases and s*gn di/dt* =-1. The conditions for the transition from S1 to state S2 are not satisfied. The system stays in S1 until the next Trig, then a transition to S3 occurs.
3) If an SCF has occurred the switch S is closed, so as in normal conditions, i_L increases and *sgn di/dt* =1, and a transition occurs from S1 to S2.

State S2 corresponds to mode 1 of operation i.e., q=1. In normal conditions, the system stays in S2, and when q=0, a transition occurs to S0. However, in SCF condition when q=0, the switch cannot be turned off, so no transition occurs to S0 until the next Trig, and then, a transition to S3 occurs.

When a failure has occurred, the system goes to state S3 and stays in this state. In this state FD2_out becomes "1", and the fault is detected.

This algorithm is slower than the primary algorithm but it can detect the faults in any conditions, for any D and any switching frequency (Fig. 11).
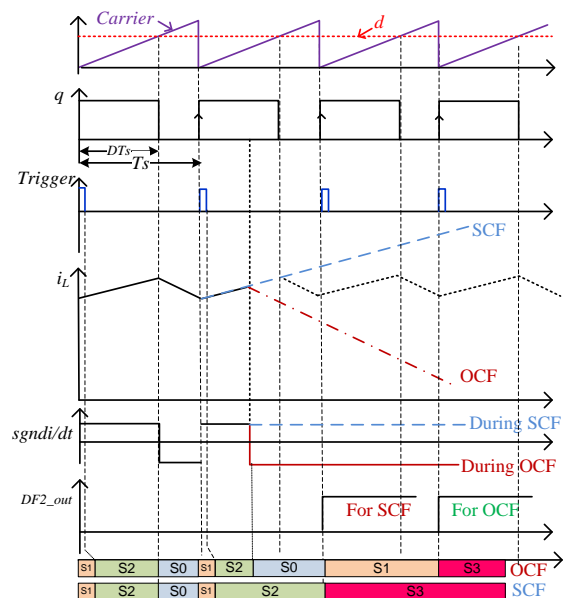

Fig. 10. Unsuccessful SCF detection by FD1 algorithm when D is large.

Fig. 11. FD2 algorithm signals and states.

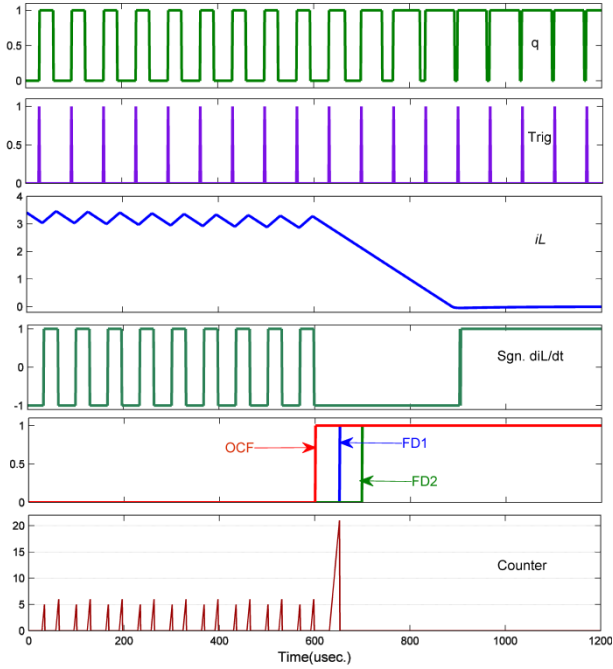Fig.12. Open circuit fault when D is close to 50%.

Fig. 13. Short circuit fault when D is close to 50%.

Finally, the general FD signal is set to '1' when one of the algorithms detects a fault (Fig. 4).

As described in this section, the proposed FD method can detect OCFs as well as SCFs very quickly, without adding any extra current or voltage sensors in the system. It is interesting because additional sensors affect the reliability, cost and weight of the system.

IV. SIMULATION RESULTS

Based on SimPowerSystems toolbox and Matlab/Simulink, a model was developed for verifying the validity of the proposed FD method. As mentioned before, because of similarity in the operation of single-ended nonisolated dc-dc converters family, the FD method is applied to a boost converter. The parameters used in simulation and experimentation are summarized in TABLE I. To consider the system delay, a large enough fault observation time is used. Here NT_c is chosen to equal 20 μs. The sample time (T_c) is chosen to equal 1 μs, corresponding to the FPGA operation frequency which is used in the experimental setup, as explained in section VI. Consequently, N is chosen to equal 20.

It is noticeable that in order to study the effects of input voltage variations on the proposed fault detection method, we did not use any capacitor after rectifier stage. Therefore V_{in} and consequently D are not constant.

Simulations are performed in different operating conditions, for OCF and SCF with D close to 50%, OCF with small D value, and SCF with D close to 80%. The results are presented and discussed in the following.

As shown in Fig. 12, D is close to 50% and an OCF occurs at t=600 μs. The primary algorithm (FD1) detects the fault after 20 μs. The secondary algorithm (FD2) detects the OCF

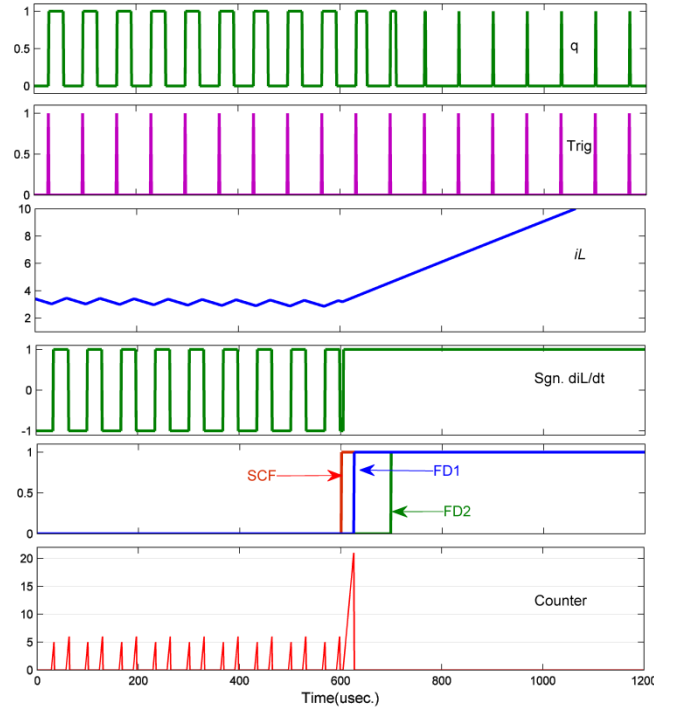by second Trig after fault occurrence. Since the two algorithms work in parallel, the fastest response will be considered as the response of the FD. Overall, the fault is detected very quickly (in 20 μs) by FD1. Both methods detect SCF in this condition as well, as presented in Fig.13.

For OCF with small D value, the simulation results are presented in Fig. 14. It can be clearly seen that because of the small duty ratio, the counter cannot reach N=20 before the change of the command order q, so the FD1 algorithm cannot
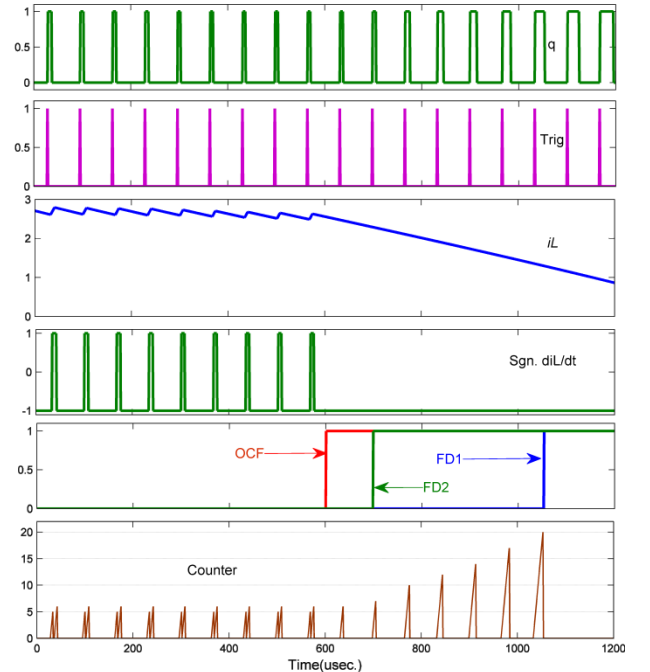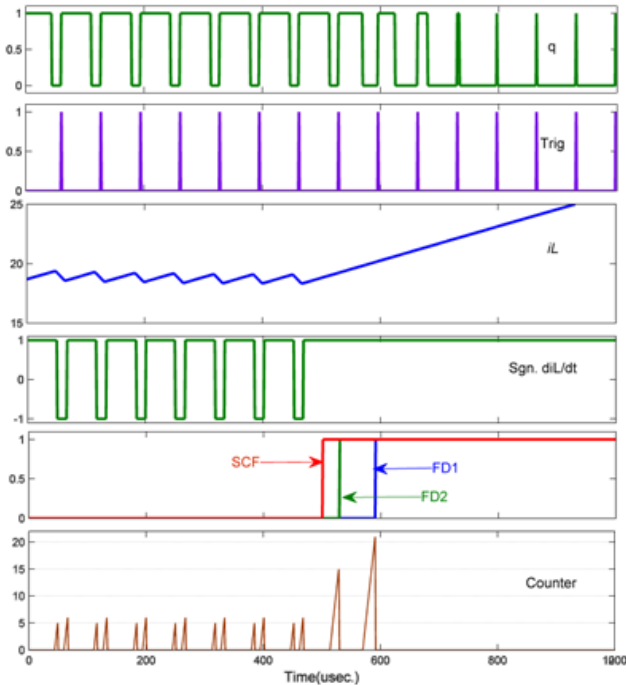

Fig.14. Open circuit fault when D is small.

Fig.15. Short circuit fault when D is around 80%.

detect the OCF in the period when the fault is occurred. After the OCF occurrence the control tries to increase i_L by increasing D. As can be seen in Fig.14, FD1 has detected the fault when D value is sufficient for the counter to reach $N=20$ which, in this case, occurs after seven switching periods. However, FD2 detects the fault once the second Trig is applied. The maximum time that is needed to detect the fault is two switching periods after fault occurrence. It confirms the robustness and the rapidity of the proposed method.

Fig. 15 presents the simulation results for an SCF when D is around 80%. As in OCF with small D, here the counter cannot reach to N=20, so the fault cannot be detected immediately by FD1, and it can be detected only when the controller reduces D, as shown in Fig. 15. But FD2 detects the fault in the

following Trig. These simulation results confirm that the proposed method can detect a fault within a maximum of two switching periods after its occurrence.

V. EXPERIMENTAL RESULTS

The experimental setup is shown in Fig.16. It consists of a boost converter, an FPGA with an interface board, a resistive load, a three-phase AC source and a three-phase diode rectifier. Parameters are the same as reported in the previous section.

The FD and the control schemes are implemented on a single FPGA chip. The FPGA implementation is briefly explained in this section; a more detailed flow implementation can be found in [19]. After discrete simulations with Simulink in Matlab environment, simulation with Altera DSP Builder blocks is carried out. Simulink blocks are replaced with DSP Builder ones. For data exchange between DSP Builder and Simulink blocks, proper input/output blocks are used. Using DSP Builder allows us to have visual programming and to translate it to Hardware Description Language (HDL) form very easily. An intermediate Hardware In the Loop (HIL) step is used for more realistic evaluation of the control and detection implementation. In this step, the power system is simulated in the Matlab/Simulink environment, while the control and diagnosis parts are both implemented on the FPGA. The VHDL (Very high speed integrated circuits Hardware Description Language) design is later compiled using Quartus software and uploaded on the Altera FPGA board via a Joint Test Action Group (JTAG) interface. Here, a Stratix DSP S80 development board is used, which includes the Stratix EP1S80B956C6 FPGA chip. This chip contains 79,040 programmable logic elements. For IGBT, SEMIKRON SKM50GB123D devices are used. It is controlled by a SKHI22A driver. A PR30 current sensor is used for current measurement. Voltage measurement is done by MTX 1032-B. AMP02E op-amps (operational amplifiers) are used in order to amplify the outputs of voltage and current sensors, for
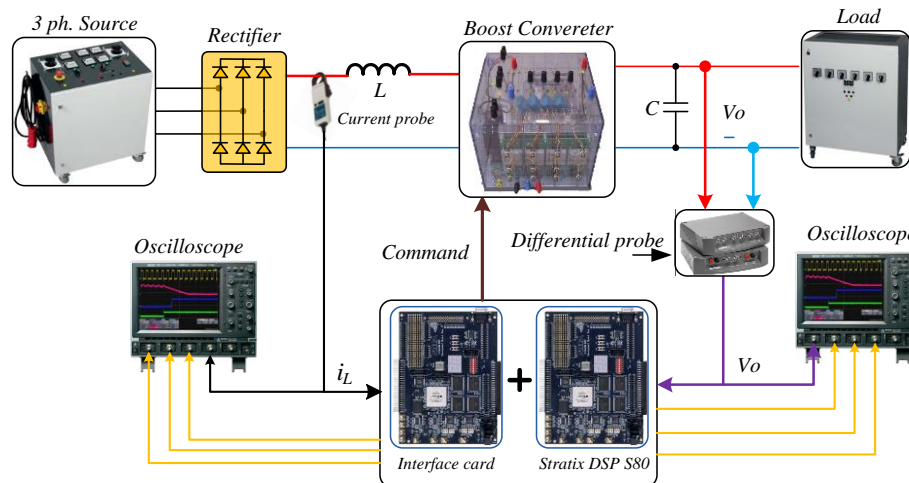

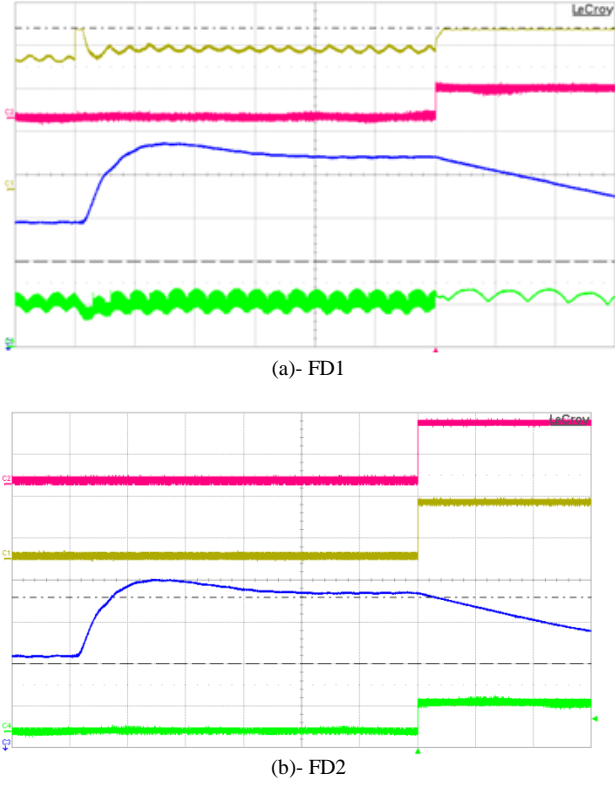Fig. 16. Experimental setup realized for this study.

(a)- FD1

(b)- FD2

Fig. 17. Experimental results for an open circuit fault - (a) From top to bottom: duty cycle (D), fault, V_o (20V/div), V_{in} (50 V/div)
(b) From top to bottom: FD1_out, FD2_out, V_o (20V/div), Fault - Time scale: 10 ms/div

(a)- FD1

(b)- FD2

Fig. 18. Open circuit fault detection with d≈40%. - (a) From top to bottom: FD1_out, counter, sgn(di/dt), q - (b) From top to bottom: q, i_L (1 A/div), FD2_out, fault - Time scale: 100 µs/div.

analogue to digital (A/D) conversion. The measured variables are then digitalized using ADS7810 A/D Converters (ADCs). The logic states at the output of the ADCs are memorized during the conversion process using SN74HC174N D-type flip flops. In this experimental setup, maximum total system delay (delay of IGBT and driver, A/D converter, sensors, interface circuit, etc.) is less than 10 µs, therefore to avoid false FD, observation time (NT_c) is chosen to equal 20 µs. The FPGA operation frequency is chosen to equal 1MHz, corresponding to a sample time (T_c) equal to 1 µs. Consequently, N is chosen to equal 20. It should be noted that a higher operation frequency for the FPGA will only result in higher sampling rate and a larger N, and the fault cannot be detected any faster. In fact, the detection time is only restricted by the unavoidable natural delays of the system. The switching frequency of the converter is equal to 15 kHz.

In these experiments, we have estimated the sign of the slope of the inductor current by a simple yet effective method:

$$(sgn(i_L)) \cong sgn(i_L(1 - z^{-5})) \qquad (12)$$

The effectiveness of this method is later approved through the experimental waveforms.

First, an open switch fault is studied. The switch is held open by removing its switching command. Fig. 17 presents the behavior of the system and the FD method in response to such a fault. In order to evaluate the closed loop control, a step in the output voltage reference is applied to the controller, before the fault occurrence. The output voltage V_o is presented in both
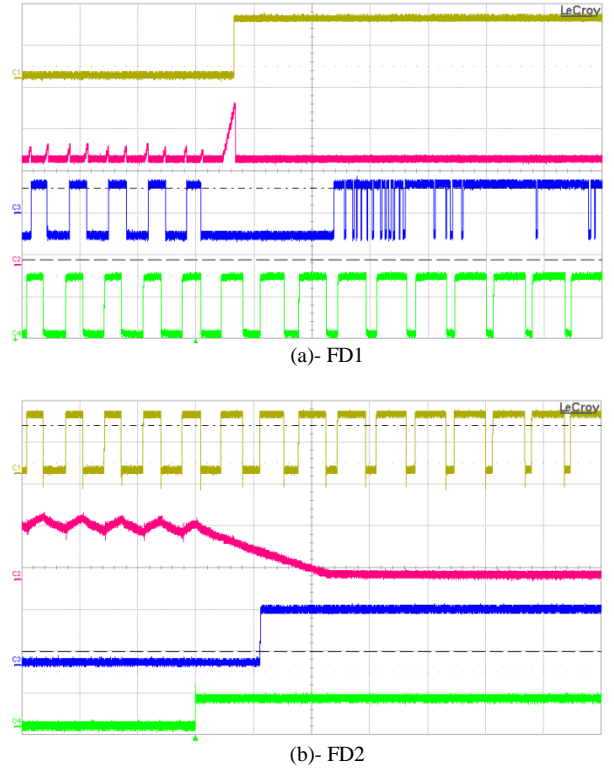
oscilloscopes, as visible in the Fig. 17(a) and Fig. 17(b). In 60ms after this step in the output voltage reference, the fault is applied. Fig. 17(a) shows that the output voltage is decreased after fault occurrence. Since the inductor current decreases constantly after the fault occurrence, the control loop tries to compensate this effect by increasing the duty cycle. This phenomenon and its effect on the FD are later explained. Fig. 17(b) shows that both detection subsystems have detected the fault very quickly. In order to be able to study the performance of the presented FD method, following experimental results will provide zoomed views of the FD signals.

Fig. 18 shows the results for a duty cycle around 40%. Fig. 18(a) shows the detection signals in FD1. It can be seen that after fault occurrence, the counter output passes the defined threshold (N), hence the fault is detected in 20µs. Fig 18(b) shows the detection signals of FD2. The fault is detected when during a whole switching period, the current slope is negative. In this case, the fault is detected in less than two switching periods (110 µs). Both methods have successfully detected the fault, but FD1 is faster. One can observe that very similar to the simulation results, after the open switch fault, the inductor current has constantly reduced, although its reference has not. Therefore, the current controller has increased the duty cycle over the time.

Fig. 19 shows the open-circuit fault with duty cycle around 20%. Clearly, in this case FD1 is unable to detect the fault immediately after the fault occurrence. On the other hand, the controller will gradually increase the duty cycle, since the inductor current is constantly decreasing. Therefore FD1 can
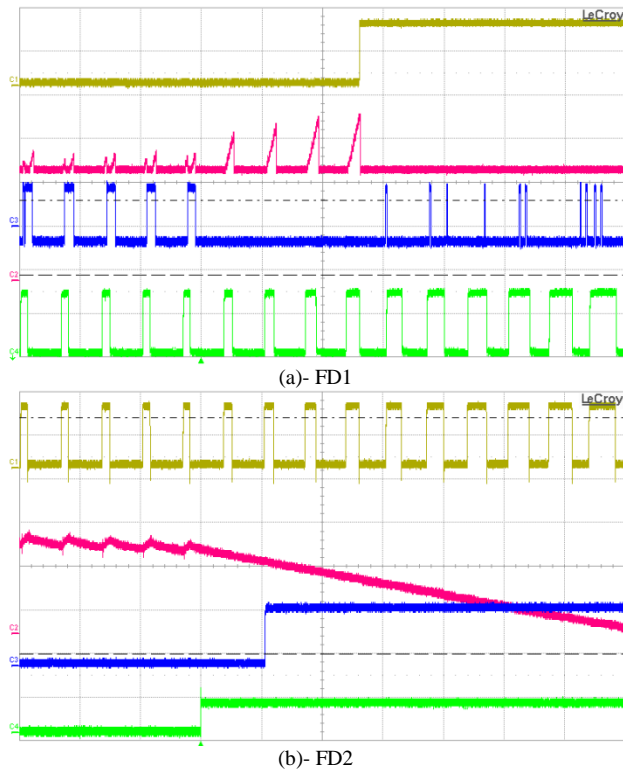
(a)- FD1

(b)- FD2

Fig. 19. Open circuit fault detection with d≈20% - (a) From top to bottom: FD1_out, counter, sgn(di/dt), q - (b) from top to bottom: q, i_L (2 A/div), FD2_out, fault - Time scale: 100 µs/div.

(a)- FD1

(b)- FD2

Fig. 20. Short-circuit fault detection with d≈60%. (a) from top to bottom: FD1_out, counter, sgn(di/dt), q (b) from top to bottom: q, i_L (2 A/div), FD2_out, fault. Time scale: 50 µs/div.

ultimately detect the fault, but the detection time will depend on the speed of the controller. In this case the fault has been detected in 260 µs. However, FD2 will again detect the fault successfully in less than two switching periods ($t_{det} = 105$ µs). In other words, fast and robust FD is always possible using FD2. If possible, the FD will be still more rapid using FD1.

To realize the SCF, the switch command is forced to be equal to '1'. Fig. 20 shows the results for a switch short-circuit fault. Both methods have detected the fault, and FD1 has been able to do it more quickly. Results are provided in Fig. 21 for a large duty cycle (D≈80%). FD1 is unable to detect the fault immediately after the fault occurrence, but as the inductor current increases, the controller reduces the duty cycle. This will lead ultimately to the possibility of FD by FD1 (in 160µs); however the detection time in this case depends on the controller behavior, and would have been higher with a slower controller. FD2, however, has successfully detected the fault again (in 90µs).

These results show that the proposed method can always detect both open and short-circuit faults very quickly. The maximum detection time is around two switching periods (133 µs in these experiments), but in most cases, it can be reduced to 20µs by using FD1 subsystem. Therefore robust real-time FD with this method is possible.
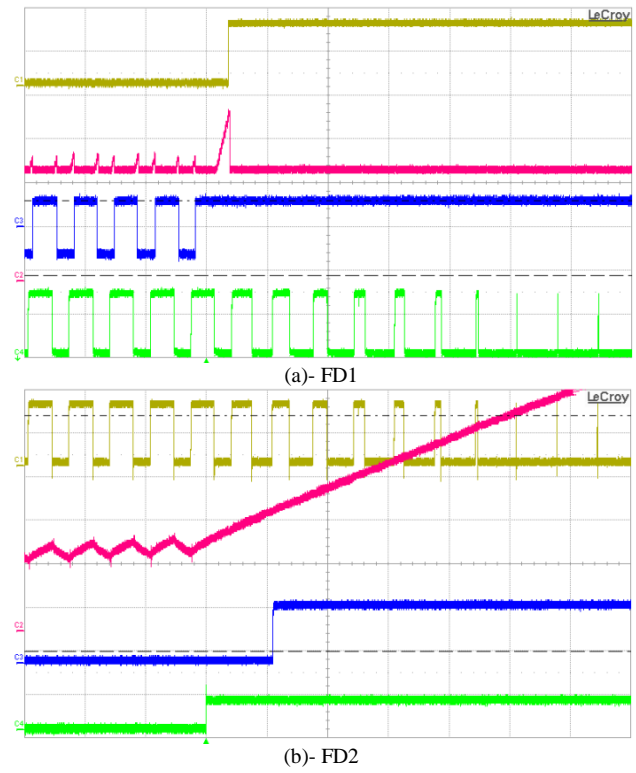

(a)- FD1

(b)- FD2

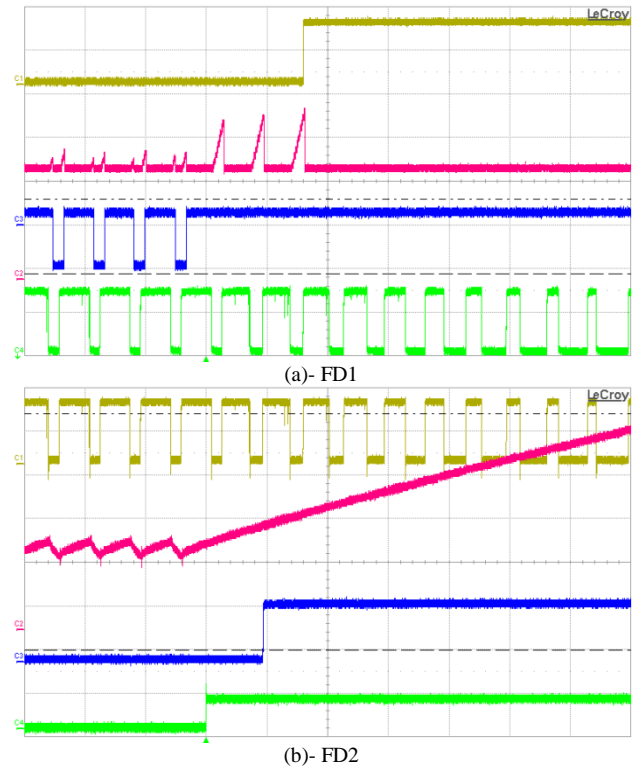Fig. 21 Short-circuit fault detection with d≈80%. (a) from top to bottom: FD1_out, counter, sgn(di/dt), q (b) from top to bottom: q, i_L (2 A/div), FD2_out, fault. Time scale: 50 µs/div.

VI. CONCLUSION

DC-DC converters are increasingly being used in industrial applications. In many cases, they are used in either embedded or safety critical applications, such as applications in distributed DC systems in ships, airplanes, computers and in telecommunication. On the other hand, switch faults are the second most common faults in these converters, after aluminum electrolytic capacitor. In order to have a suitable response to a switch fault in a DC-DC fault tolerant system, fast FD is the first step. Very fast FD of non-isolated DC-DC converters is studied in this paper. A hybrid method is proposed that is based on two subsystems, one for robust FD (FD2) and the other one for fast FD, (FD1). FD in FD2 is based on the fact that in normal operation of the converter, during a switching period with restricted duty cycle, the inductor current cannot always increase or decrease. FD1 directly compares the estimated and measured values of the sign of inductor current over the time for FD. Simulation and experimental results are carried out on a boost converter in order to evaluate the proposed method. An FPGA is used for experimental implementation of this method to perform very fast FD. A closed loop controller is used, and its effect on the FD is considered. Results show excellent performance of this method for both open and short-circuit switch faults. It is shown that the performance of the FD1 algorithm may depend on the controller speed in some cases, whereas the maximum detection time of FD2 is constant and equal to two switching periods.

The proposed method is simple enough to be implemented in a small FPGA target and it is fast, robust and efficient, without requiring any additional sensors.

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