Recent Advance in High Manufacturing Readiness Level and High Temperature CMOS Mixed-Signal Integrated Circuits on Silicon Carbide

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Abstract

A high manufacturing readiness level silicon carbide (SiC) CMOS technology is presented. The unique process flow enables the monolithic integration of pMOS and nMOS transistors with passive circuit elements capable of operation at temperatures of 300°C and beyond. Critical to this functionality is the behaviour of the gate dielectric and data for high temperature capacitance-voltage measurements are reported for SiO_2/4H-SiC (n and p type) MOS structures. In addition, a summary of the long term reliability for a range of structures including contact chains to both n-type and p-type SiC, as well as simple logic circuits is presented, showing function after 2,000 hours at 300°C. Circuit data is also presented for the performance of digital logic devices, a 4 to 1 analogue multiplexer and a configurable timer operating over a wide temperature range. A high temperature micro-oven system has been utilised to enable the high temperature testing and stressing of units assembled in ceramic

dual in line packages, including a high temperature small form-factor SiC based bridge leg power module prototype, operated for over 1,000 hours at 300°C. The data presented show that SiC CMOS is a key enabling technology in high temperature integrated circuit design. In particular it provides the ability to realize sensor interface circuits capable of operating above 300°C, accommodate shifts in key parameters enabling deployment in applications including automotive, aerospace and deep well drilling.

Keywords: silicon carbide, SiC, CMOS, mixed-signal, integrated circuit, wide bandgap, High temperature, HiTSiC®

Introduction

Emerging technologies in wide band-gap silicon carbide (SiC) positions it as a leading candidate for the manufacture of integrated circuits (ICs) operating at temperatures beyond 450°C [1]. The development of SiC based power switches [2] and rectifying devices [3] are enabling technologies for the realisation of power systems [4] capable of operation at temperatures beyond those possible with conventional silicon based devices. Silicon on Insulator SOI-based integrated circuits are in general limited to operation at temperatures below 200°C [5]. The high temperature operation of SiC in both power systems and integrated circuits enables potential advantages realised through system level efficiencies. However, the maximum operating temperature achieved by these SiC based components depends on the selected transistor technology, as well as the interconnect metallisation and device packaging [6]. In order to exploit the potential of high temperature power electronic systems realised through the use of SiC components, a supporting integrated circuit technology, which can be located in close proximity to the local heat sources, is required to provide sensing control and gate drive functions.

Reports in the literature of BJT circuits operating up to 500°C have shown promising differential amplifier characteristics [7, 8]. Other high temperature power SiC MOSFET evaluation at up to 200°C has also been realised by University of Tennessee [9]. An innovative high temperature 3D half-bridge

by ABB [10] and data from both characterisation and simulation work using gate drivers have been reported on a hotplate up to 300°C by Ohio State University [11]. Nevertheless, recent advances in high temperature SiC integrated circuits are still based on nMOS technology [11]. CMOS based circuits incorporating both nMOS and pMOS have demonstrated package devices operating at temperatures in excess of 300°C [12, 13] and more recently 540°C [13] using the HiTSiC® CMOS. The most significant advantage of CMOS is the ability to provide circuit designers with a more comprehensive option to implement control and drive functions. In conventional power electronic applications, silicon based high temperature electronics have been limited to ratings set within the boundaries based on the material properties and the dissipation from the heatsink of the package. SiC offers superlative material properties, which enable the resulting circuits to operate in extreme environments, resulting in a capability to integrate both digital logic and analogue sensing functions close to the heat generating power switches.

A manufacturing process using 4H-SiC has been realised, which is capable of enabling the integration of mixed signal circuit elements to form integrated circuits. The components used in the design of the transistors are optimised for the resulting circuit to operate on a single supply of 15V. The CMOS process results in highly integrated p-channel and n-channel MOS transistors along with high temperature passive components. The CMOS integrated circuit process utilises a poly-silicon gate process, combined with a single layer refractory metal interconnect, enhanced with gold enforcement layers on the bond pad sites. Functional circuits have been demonstrated at a range of temperatures up to 400°C. Whilst nMOS based SiC IC technologies have been demonstrated previously, they rely on the use of passive pull-up loads. The lack of active pull up elements in a logic circuit significantly reduces the switching speed of the elements that form the basis of the logic functions. The use of a passive load topology also increases the power consumption of the circuit significantly. Through the use of a full CMOS topology, the current and speed performance of logic circuits can be improved [14].

CMOS process overview

The High Temperature Silicon Carbide CMOS (HiTSiC®) manufacturing process results in the formation of monolithically integrated CMOS circuits within a thin epitaxial layer on a 100 mm, Si

face, 4° off axis 4H-SiC substrate [15]. The transistors are manufactured in spatially localized, lightly doped implanted wells formed in the epilayer, with further heavily doped n+ and p+ implants to produce the source and drain regions. The doping profiles, dielectrics and deposited films are designed to allow operation on a single 15V supply at temperatures from room temperature to beyond 300°C. The threshold voltage of both the nMOS and pMOS devices are controlled through the use of threshold adjust implants in the channel region. All implants are annealed simultaneously using a carbon cap process to protect the surface of the SiC [16], prior to field oxide and gate dielectric growth. The gate conductor is fabricated from a deposited polysilicon layer, with a subsequent layer used to produce a customizable resistor layer and/or the second plate of an integrated capacitor. The interconnect metallisation is a refractory metal with the bond pads constructed with suitable barrier layers allowing a gold layer to passivate the surface. Figure 1 shows a schematic cross section of the structures used in the HiTSiC® process.

Passive circuit elements

At high temperatures, the leakage current of the transistor junctions and capacitors can compromise the performance of the logic elements used in the circuits. The formation of a monolithically integrated capacitor can be achieved by using the polysilicon gate material and a second layer of polysilicon deposited over a thin dielectric layer, resulting in a capacitance density of approximately 0.7fF/μm^2. The variation in the capacitance density of this integrated capacitor structure with temperature is shown by the data in Fig. 2. As can be seen from the data, a linear increase in the capacitance density with increasing temperature is evident, however, the change between room temperature and 400°C is less than 2%, reducing the demands on the circuit design. The DC leakage current as a function of voltage for a capacitor at elevated temperatures is shown in Fig. 3. The data show that for an operating voltage of 15V, negligible leakage currents occur, even at 400°C. This indicates that this integrated capacitor structure is suitable for the implementation of switched capacitor circuit architectures within an IC, which typically require capacitances of a few pF. However, these architectures require the charge stored on the capacitor to be maintained over a refresh cycle of a few tens of microseconds, which places significant constraints on the DC leakage currents that can be

tolerated. In addition, breakdown voltages significantly in excess of 40V are achieved in these capacitors, confirming their suitability for operation in circuits with a supply voltage of 15V.

Resistance results

The data in Table 1 were extracted from the sheet resistance of the n+ source / drain and p+ source / drain regions using four terminal Van Der Pauw test structures. As expected, the resistance of the n-type regions increases with temperature, reflecting the decrease in bulk mobility due to increased phonon scattering, whilst the more resistive p-type resistance falls rapidly, indicating higher acceptor ionization as the temperature increases [17, 18].

Temperature	23°C	100°C	200°C	300°C	400°C
N+ sheet resistance (Ω/□)	316	330	350	390	435
P+ sheet resistance (Ω/□)	15300	6100	3300	2300	2000

Table 1. Sheet resistance of implanted regions as a function of temperature.

The room temperature contact resistance data shown in Figs 4 & 5, was extracted from contact via-chain to N+ and P+ source/drain structures and has been measured after 7,500 hours of a on-going reliabilty test at a soak temperature of 300°C. The voltage across the contact chains is monitored and the contact chain resistance determined. The data shows evidence of noise originating in the measurement system, however the data clearly shows that there is no catastrophic failure of any contact in any chain and that the variation in contact resistance is less than 5% after more than 7,500 hours at 300°C.

High temperature CMOS capacitor characteristics

Both lateral n-type and p-type MOS devices were fabricated in a short loop CMOS process which using epitaxial layers doped with nitrogen for n channel (1.50×10^{17} cm^{-3}) and aluminium for p-channel

(1.02×10^{17} cm^{-3}) respectively. This approach focuses only on the influence of critical gate dielectric processes [19], with nominated total effective oxide thickness of 33 to 36nm, on the device characteristics because there are no implants other than N+ and P+ contact regions. Both MOS devices are operating in the bulk epilayer. In order to investigate the stability and temperature dependence of oxide parameters, 1 MHz Capacitance-Voltage characteristics were measured as a function of temperature. As can be observed from the data in Fig. 6, the C-V curves for the nMOS device show no variation in the depletion region as the temperature increases. A noticeable shift in the characteristics is observed for the p-type MOS sample at both 200°C and 300°C, which indicates the presence of unstable effective oxide charge or significant levels of electron trapping at the SiO_2/SiC interface.

From the C-V data, parameters including flatband voltage (V_{FB}), threshold voltage (V_{TH}) and effective charge (N_{EFF}) have been extracted to assess the effectiveness of the process in realizing high quality nMOS and pMOS dielectrics. The data in the figure show the normalised capacitance (C/Cox) in the region where V_{FB} separates the accumulation region from the depletion region and V_{TH} demarcates the depletion region from the onset of inversion. From the data absolute values of $|\Delta V_{FB} - V_{TH}|$ can be determined as 7.26V for nMOS and 6.49V for pMOS. This indicates that the observed variation in V_{FB} is linked to the reduction in threshold voltage and this shift in flatband voltage from the theoretical value for the pMOS is greater than that observed in the nMOS characteristics. This shift in V_{FB} indicates the charge density in the gate oxide for the pMOS device is greater than that in the nMOS structure and can be described using the effective charge density (N_{EFF}) [20].

High temperature CMOS transistor characteristics

The characteristics of the transistors have been measured at temperatures between 23°C and 400°C. Typical characteristics for an nMOS device with gate width of 20µm and gate length of 2µm are shown by the data in Figs. 7 and 8. The data in Fig. 8 show that the drain current increases with temperature with the gate voltage held at 15V with respect to the source. This increase in the drain current (I_D) is consistent with the reduction in transistor threshold voltage that can be observed from the data in Fig. 7 and this results in an increase in the gate overdrive for a given gate – source bias. The increase in gate overdrive arising from the reduction in threshold voltage is more pronounced in the pMOS data shown in Figs. 9 and 10.

Logic circuits

Packaged devices have been aged for extended time periods under functional bias, as shown by the illustration in Fig. 11. This high temperature "micro-oven" system [15] has been designed and built to enable testing and stressing of units assembled in these package types, which are capable of greater than 300°C operation. At pre-determined time intervals, the devices are removed from the thermal chamber and characterized at room temperature. The 20 QUAD input NAND gates were tested at 300°C for a total soak times of 2,900 hours in the above described micro-oven. All 20 devices remained functional after this period with key parameters including the propagation delays and output sink current capabilities showing only minor variation as summarised by the data in Table 2. However there is a visible degradation of output source current. This degradation is related to the effect of carrier trapping on the threshold voltage of the pMOS transistors, which is significantly larger than the V_T shift for the nMOS devices. This results in a reduction in the gate overdrive voltage for the pMOS devices in the circuit and therefore the drain current reduces. The increase in propagation delay through the NAND gate circuit is also dominated by the observed reduction in the drain current characteristic of the pMOS transistors where the reduced drive leads to an increase in rise time and hence has the effect of increasing propagation delay. The characteristics of the nMOS transistors are significantly less affected and so the output sink currents of the NAND gate are only marginally reduced. The above observations show evidence of the well-known SiC MOS transistor V_T instability, due to near interface trapping [21, 22, 23].

Parameter at room temperature	0 hours	2,900 hours
Propagation Delay TPHL (ns)	56.66	75.72
Propagation Delay TPLH (ns)	44.12	56.35
Output Sink Current (mA)	6.14	6.14
Output Source Current (mA)	-5.49	-2.76

Table 2. NAND gate parametric shifts after 2,900 hours at 300°C of an average of 5 devices

Detailed work has started to identify the longer term reliability of the transistors and resulting circuits. Five NAND logic gates were first measured to screen functionality at room temperature. The propagation delay is expected to increase at 300°C during the initial soak test and this can be observed in the data shown in Fig. 12. The key parameters extracted from the data are summarised in Table 3. The NAND gate functions are implemented with buffer circuits on the inputs and outputs. These buffers employ inversion stages involving both pull-up and pull-down transistors. Monitoring the propagation time of the NAND function enables the extraction of the key performance metrics for the transistors, including threshold voltages and on-state resistances and the effect of any changes during operation. The data presented shows a stable ageing process throughout the 2,500 hours as they are held at 300°C.

NAND gate	Propagation delay output high to low (ns)						
Temp (˚C) tested at:	RT	300	300	300	300	300	300
Hours aged:	0	0	1	500	1,000	1,500	2,500
6017 NAND gate A	136.4	-	-	168	162	151	146
6017 NAND gate B	124.9	-	-	151	164	148	148
6017 NAND gate C	151.4	-	-	144	154	156	152
6017 NAND gate D	153.5	-	-	147	156	152	154
6017 NAND gate E	137.9	155	168	161	166	154	152

Table 3. NAND gate propagation delay in 2,500 hours.

Analogue Integrated circuits

A monolithically integrated, all silicon carbide 555 timer, as shown as a schematic diagram in Fig 13, has been fabricated. The data in Fig 14 show the variation of the output frequency, for a timer configured to oscillate at 1.8Hz to drive a multiplexer circuit, with the supply voltage for a packaged timer operating at room temperature. The data show that for a supply voltage greater than a minimum threshold (7V), the variation in frequency is below 0.2Hz (9% of the initial value) for the remainder of

the supply voltage range investigated. The monotonic decrease in frequency arises from the increased power losses in the pMOS devices as the drain-source bias increases. The variation in oscillation frequency for the timer operating with a 15V supply as a function of temperature is shown by the data in Fig. 15. Here the data show that the variation is below 1% for the entire temperature range investigated, indicating that this circuit design is suitable for use in applications across a wide temperature range.

The mixed signal CMOS manufacturing process is optimised to enable fully functional circuits on a single 15V supply [24] .The 4:1 analogue Multiplexer (MUX) CMOS switch shown by the schematic in Fig 16, with switching decoded from a 2 bit binary word, has been fabricated. Figs. 17 and 18 show the on-state switch resistance and the off-state leakage current as a function of applied bias for temperatures between 23°C and 400°C. The MUX utilises both pMOS and nMOS devices to enable operation over the full 15V power supply range. The MUX demonstrates a channel leakage below 50nA at 10V as well as an ON resistance below 500Ω, both at 300°C. The low intrinsic carrier concentration in SiC allows the multiplexer to exhibit very low switch leakage at elevated temperatures in comparison to more conventional silicon based technologies.

Figure 19 shows a schematic representation of the test circuit used to determine the performance of the MUX in a typical application. Here a self-switching thermocouple multiplexer is tested, where the sensing electronics are switched to sequentially measure the temperature sensed on four different type-K thermocouples. The 5 packaged silicon carbide ICs forming the multiplexer circuit are held at a constant 300°C. The schematic block diagram in Fig. 20 shows the 555 timer described above (labeled as RSL 6016) generating a system clock, which drives a digital divider chain of D-type flip-flops (RSL 6022) to reduce the frequency. The output from the flip-flops generates the 2 bit address word for the thermocouple channel to be routed to the computer. The multiplexer switches are a 4 to 1 line analogue MUX where one switch is selected corresponding to the 2 bit address value. As shown by the data in Figs. 21 and 22, the circuit switches sequentially through each of the 4 states under the control of the address word. In the figures, the labels A, B, C and D refer to the points identified in the schematic representation of the circuit given in Fig. 20.

Hybrid Power Module

Packaged in a 32pin hermetically sealed ceramic package, the prototype small form-factor bridge leg power module shown schematically in Fig. 23, consists of two commercially available 1200V SiC Junction Transistors (GeneSiC GA10JT12-CAL) and the CMOS based control circuit. Each power transistor is connected to a driver IC manufactured using the HiTSiC® CMOS process. Commercially sourced high temperature passive devices are also mounted within the hybrid package as shown in Fig. 24.

The prototype module has currently amassed in excess of 1,000 hours of stable operation at 300°C. These tests, performed at low voltage/current demonstrates the stability over temperature, shows turn on and turn off times of 20ns at room temperature, rising to 40ns at 300°C. This increased switching time for the power devices is linked to the deep level acceptors in the base region of the device [25, 26, 27]. The data in figure 25 show the evolution of the rise and fall times of the hybrid module as a function of hold time at 300°C. After the initial increase, the variation in the rise time of the module is below 25% after 1,000 hours, whilst the fall time increases by 50%. Further investigation as to the origin of this asymmetry in the characteristics is ongoing, although initial indications suggest that the decrease in switching frequency is linked to the degradation of the contact metallisation within the power transistor [28].

Conclusions

We report the potential of a silicon carbide based CMOS technology for the realisation of high performance circuits designed for operation between 23°C and 400°C. Based on the HiTSiC® process, these circuits exploit the significant reduction in junction leakage in comparison to conventional semiconductors, including silicon. This reduction in the off state leakage current in analogue switches allows the amplification of the low voltages associated with thermocouple lines even at high temperatures. The capabilities of the technology has been demonstrated with a variety of example circuits, that range from individual transistors and interconnect structures, through to analogue and digital primitives and a fully functional, multi-channel thermocouple amplifier. The silicon carbide CMOS transistors and resulting circuits have demonstrated reliable operation for hundreds of hours at 300°C, albeit with minor variation in key parameters. These shifts in characteristics are dominated by the voltage driven threshold voltage drifts in the transistors, particularly in the PMOS devices. The

circuits reported here take advantage of the wide bandgap of silicon carbide to realise enhanced functionality at temperatures beyond those achievable with conventional semiconductor technologies. A hybrid circuit, combining signal level gate drive circuitry with power switching devices in a single package has been demonstrated that can operate for 1,000 hours at temperatures similar to those found in deep well exploration in the geothermal and oil & gas sectors.

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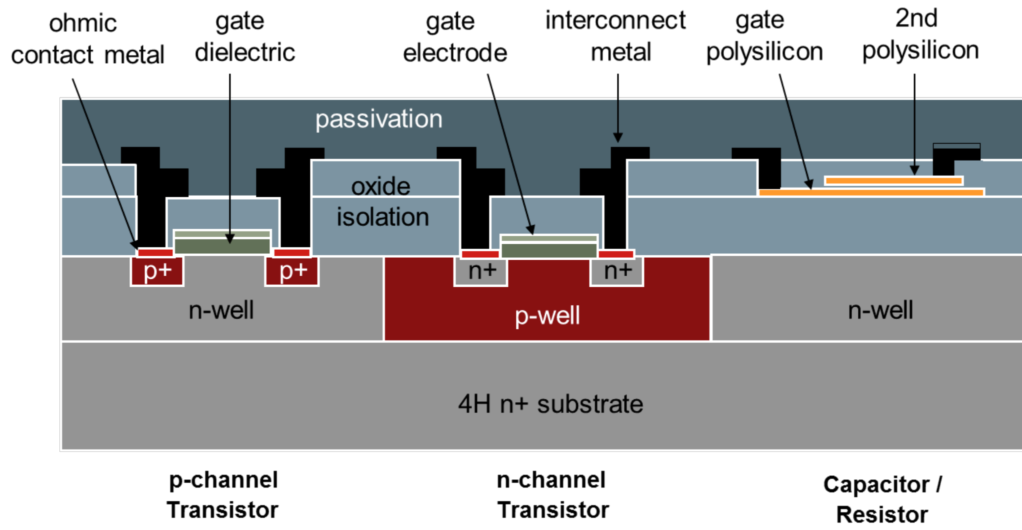
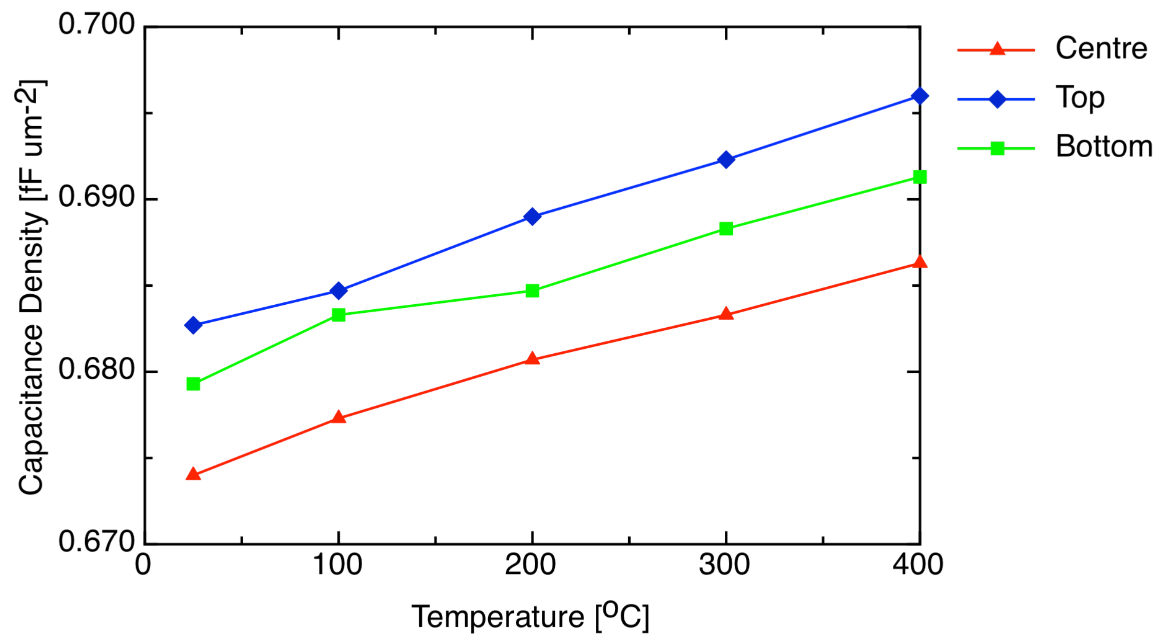
Figure 1



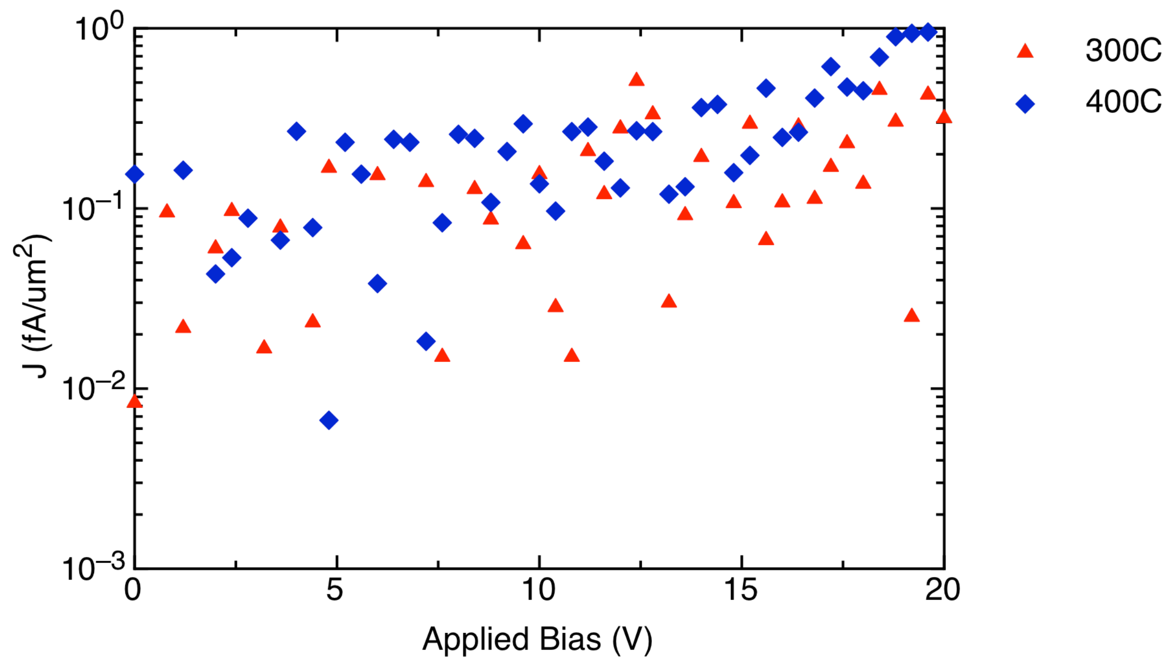
Schematic cross section of HiTSiC® silicon carbide CMOS.

Figure 2



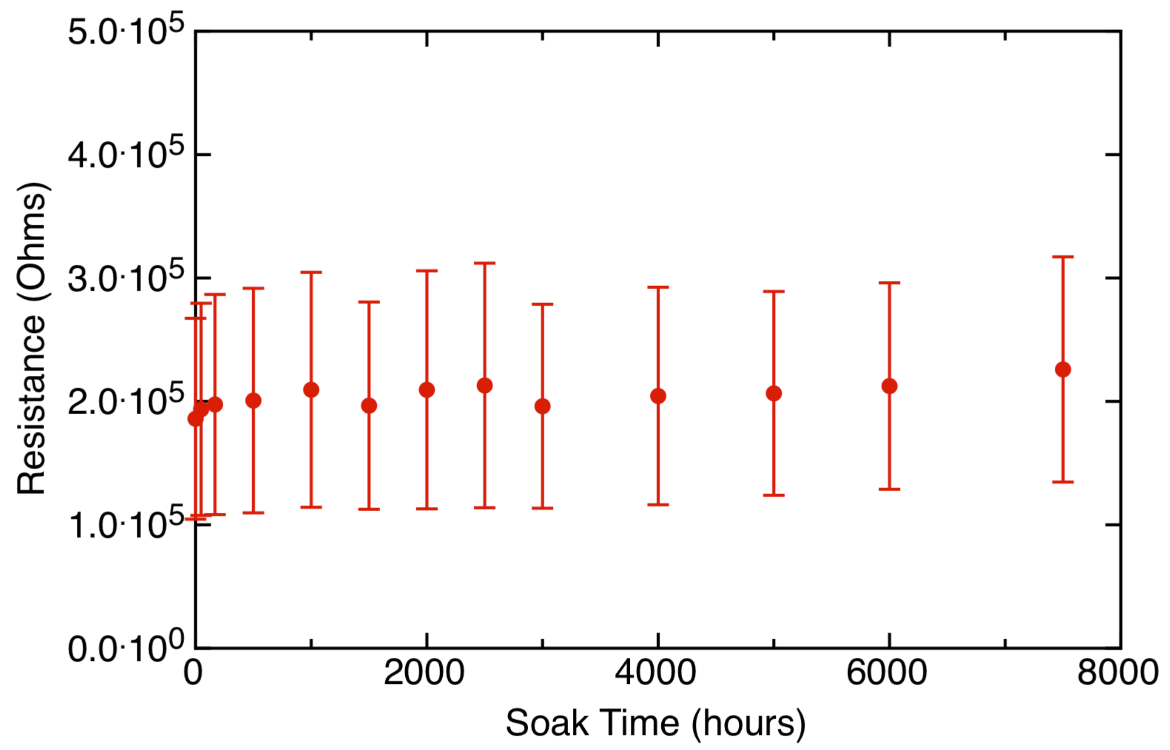
Capacitance vs. temperature over 3 sites on a wafer.

Figure 3



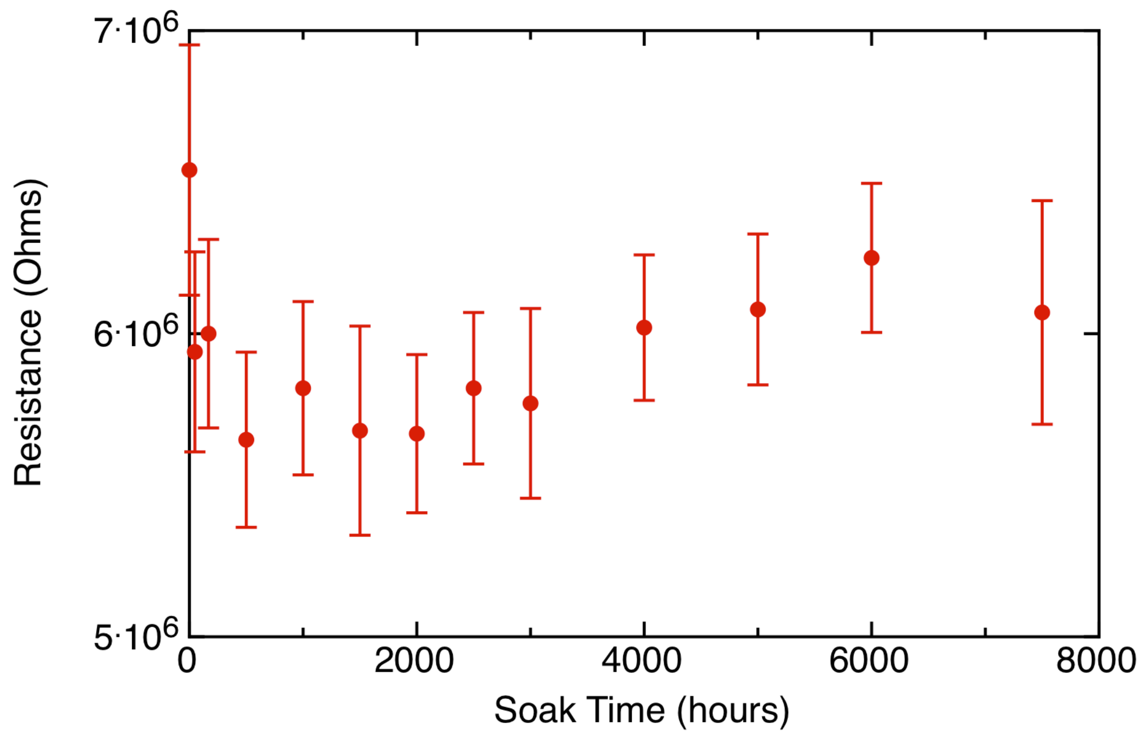
Capacitance leakage current vs. voltage at 300°C and 400°C.

Figure 4.



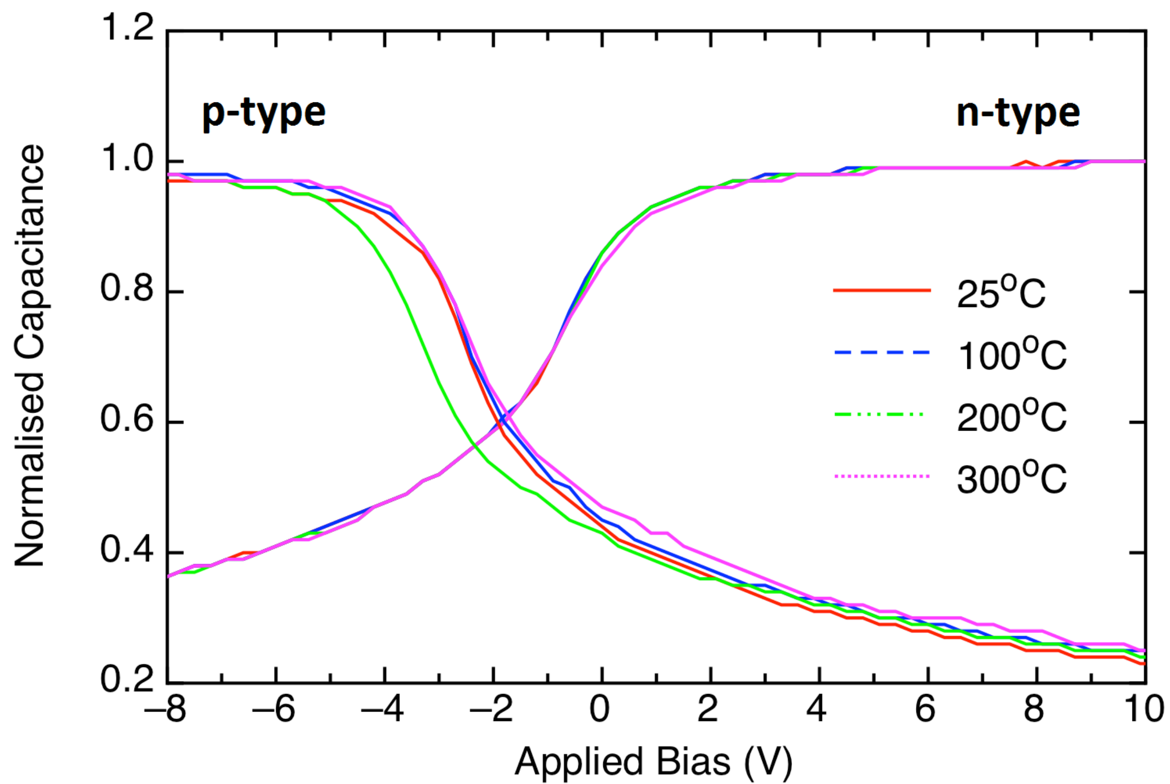
Resistance of 400 metal – N+ contacts connected in series, as a function of soak time.

Figure 5.



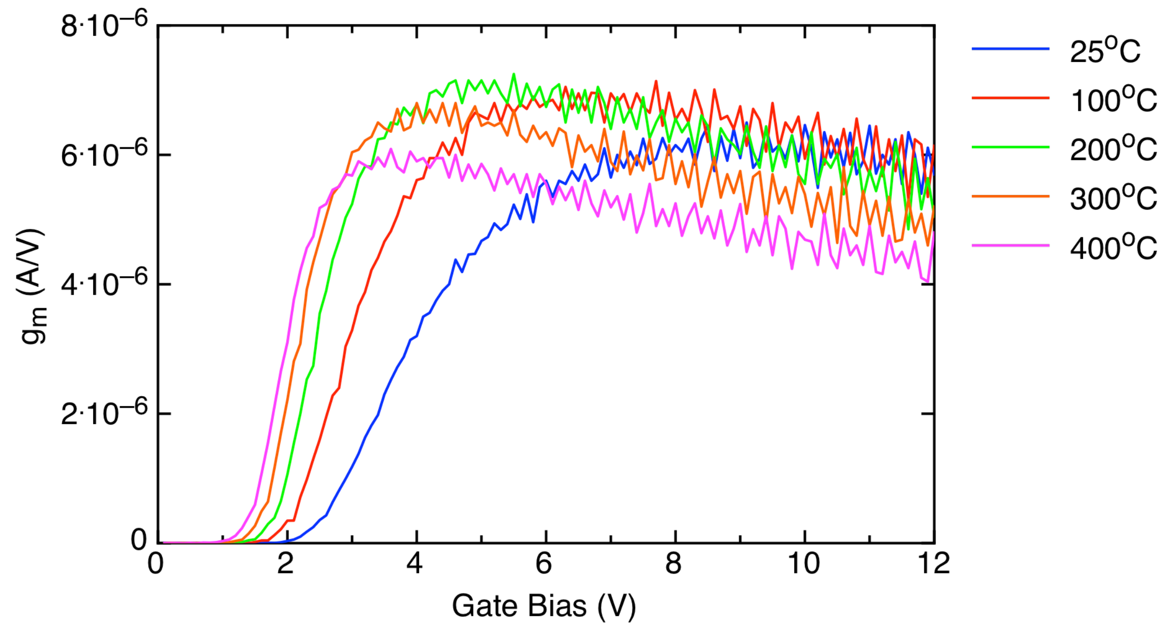
Resistance of 400 metal – P+ contacts connected in series, as a function of soak time..

Figure 6.



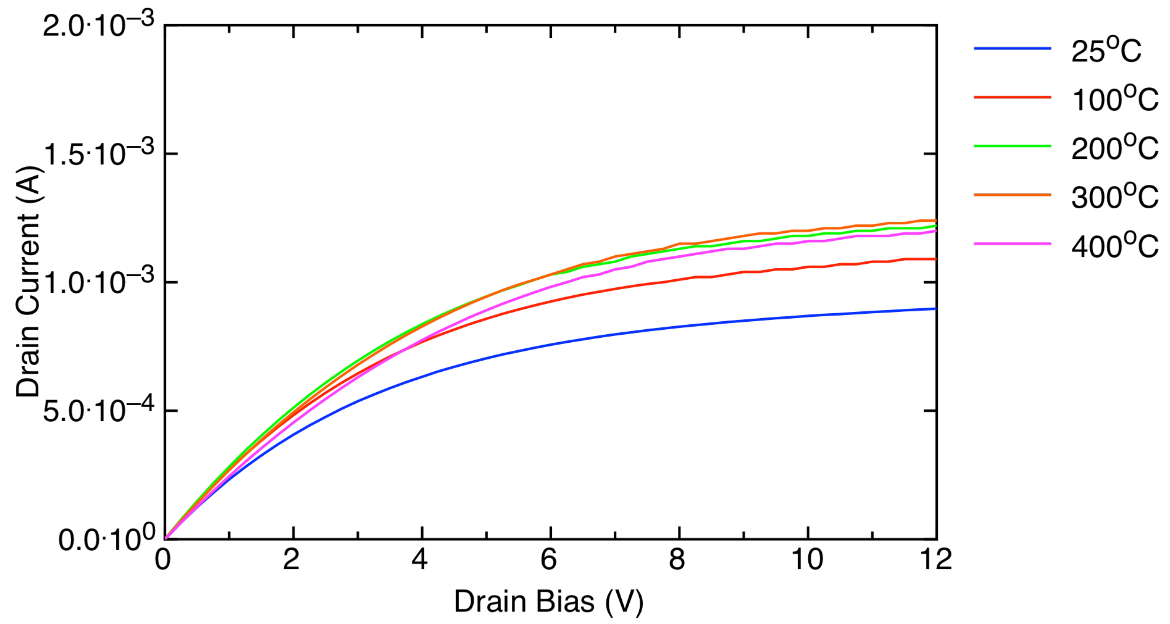
1MHz Capacitance-Voltage characteristics normalised by oxide capacitance, C_{OX}, for n-type and p-MOS capacitors respectively.

Figure 7.



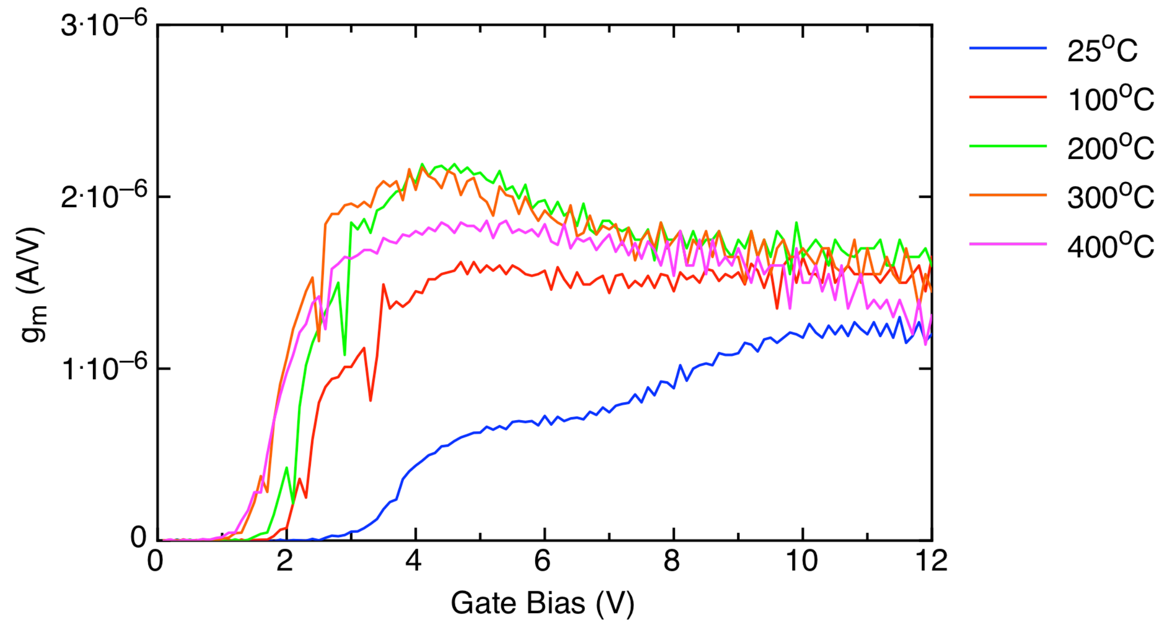
g_m curves of 20 µm x 2.0 µm nMOS transistors at temperatures up to 400°C

Figure 8.



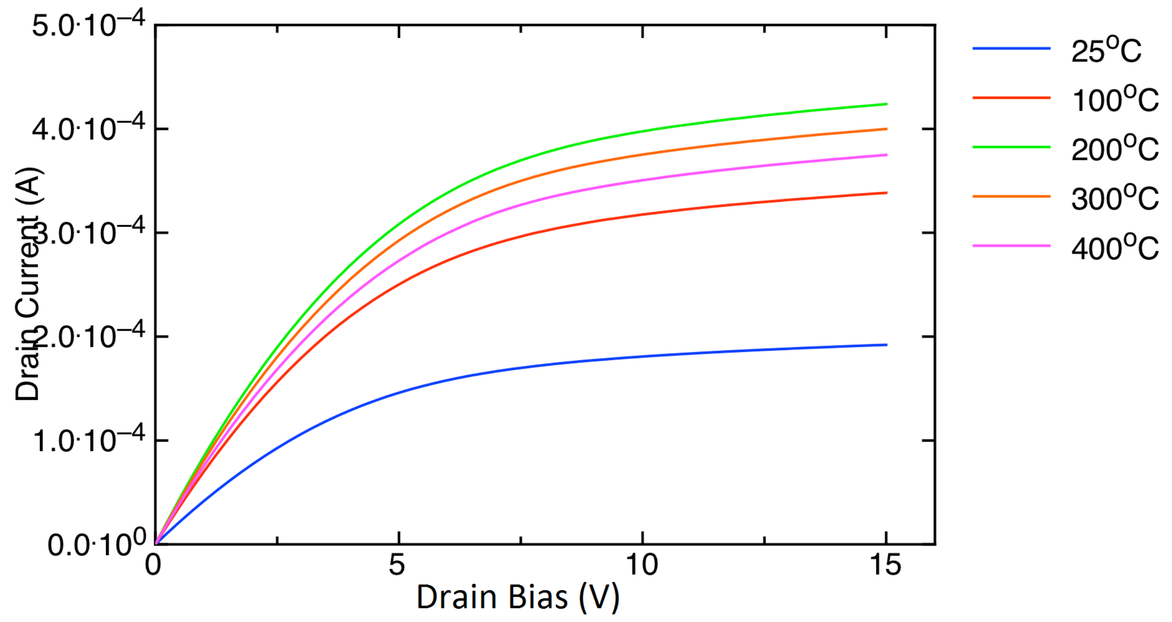
I_D-V_D curves with V_G biased at 15V of 20 µm x 2.0 µm nMOS transistors at temperatures up to 400°C

Figure 9



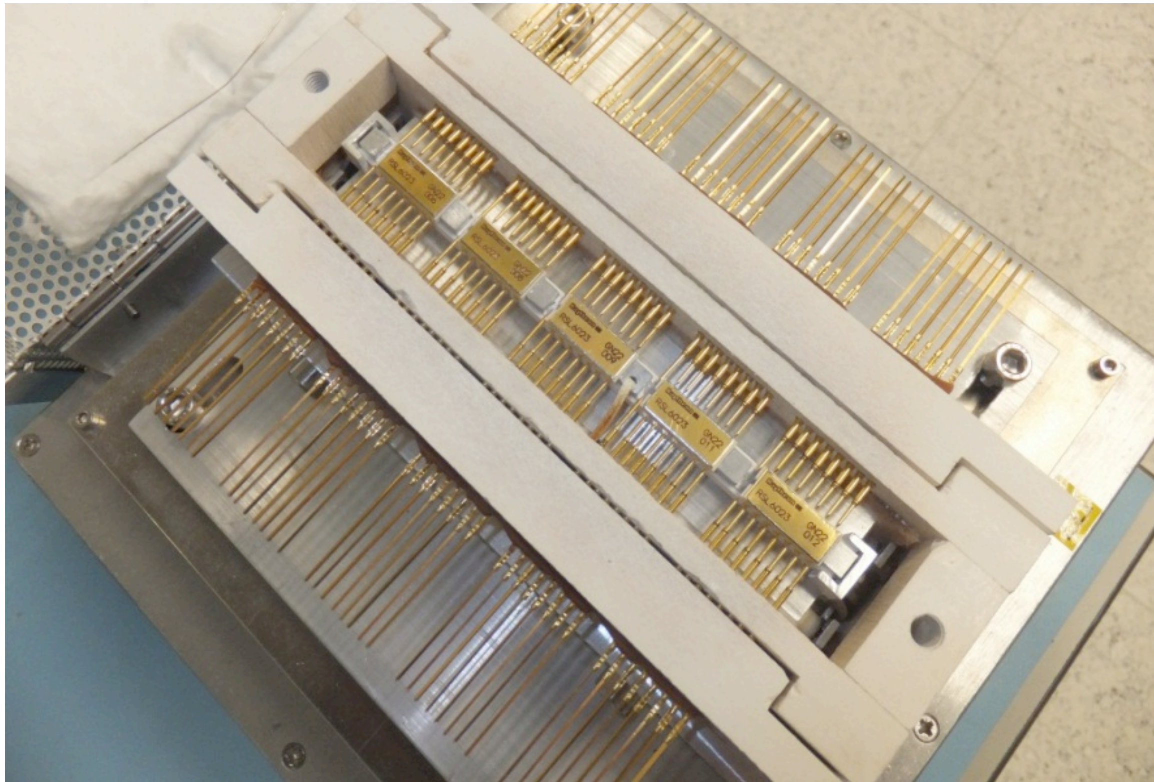
g_m curves of 20 µm x 2.0 µm pMOS transistors at temperatures up to 400°C.

Figure 10.



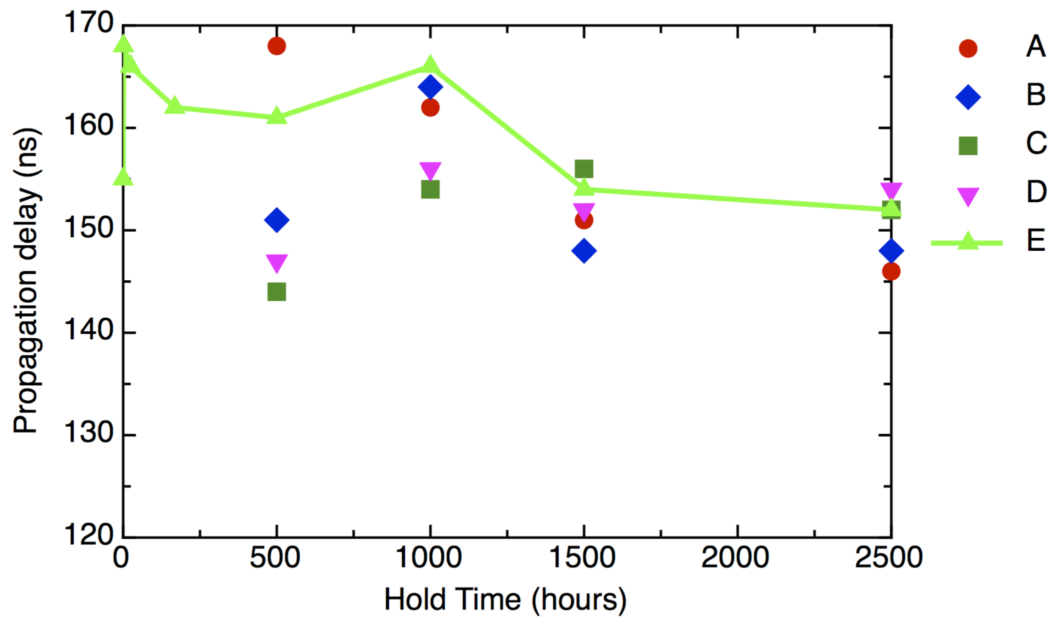
I_D-V_D curves with V_G biased at 15V of 20 μm x 2.0 μm pMOS transistors at temperatures up to 400°C.

Figure 11



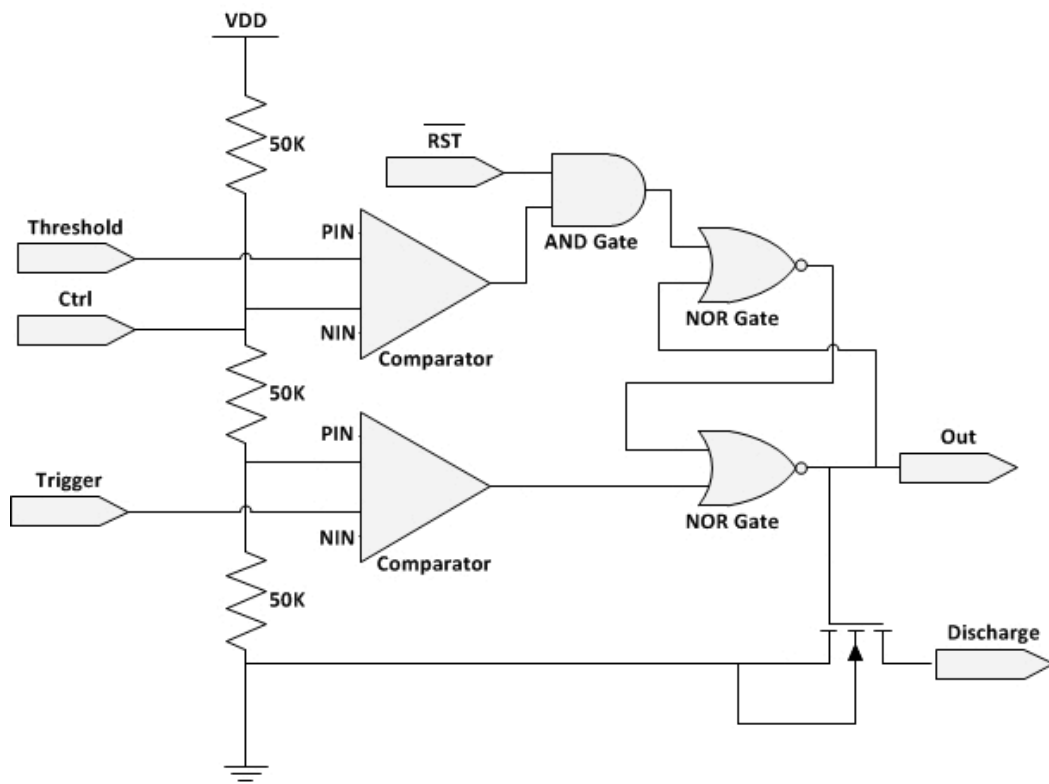
High temperature ceramic dual in line (DIL) packages in the custom-built micro-oven to facilitate testing at 300°C.

Figure 12



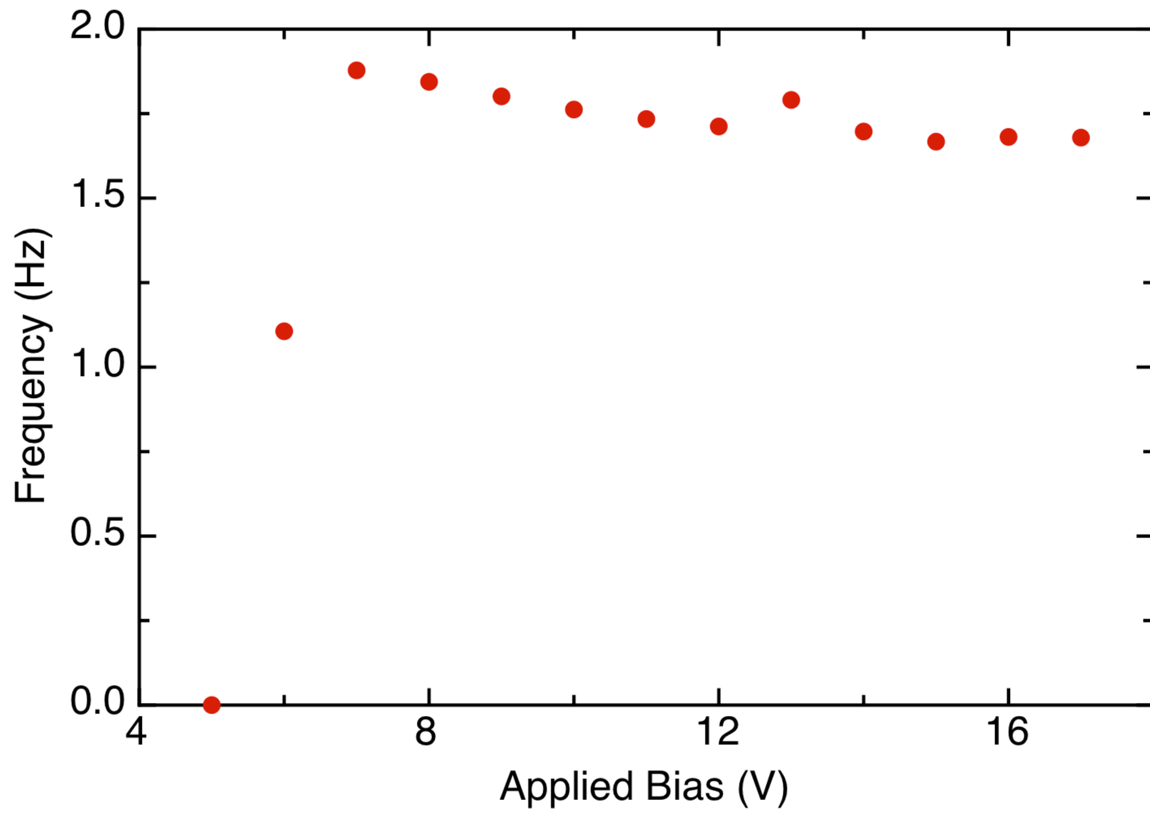
Evolution of NAND gate propagation delay as a function of hold time at 300°C.

Figure 13



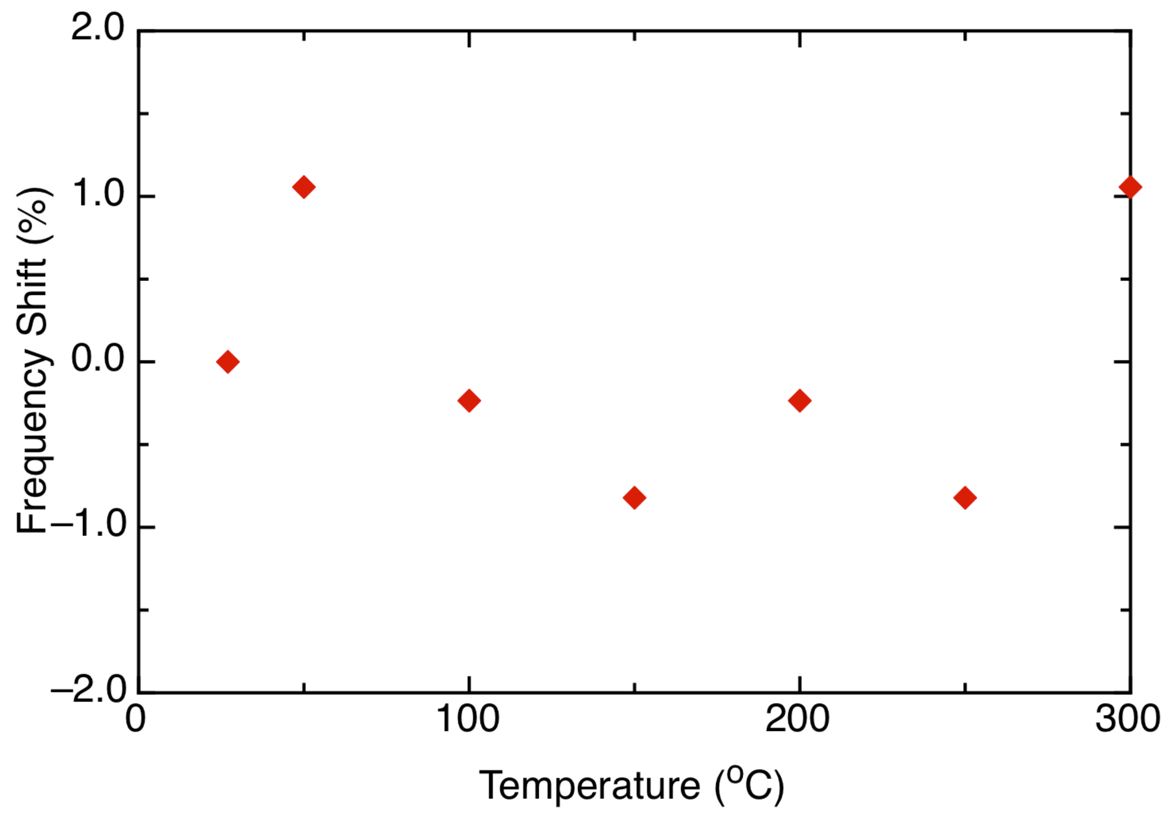
Schematic diagram of the configurable 555 timer.

Figure 14



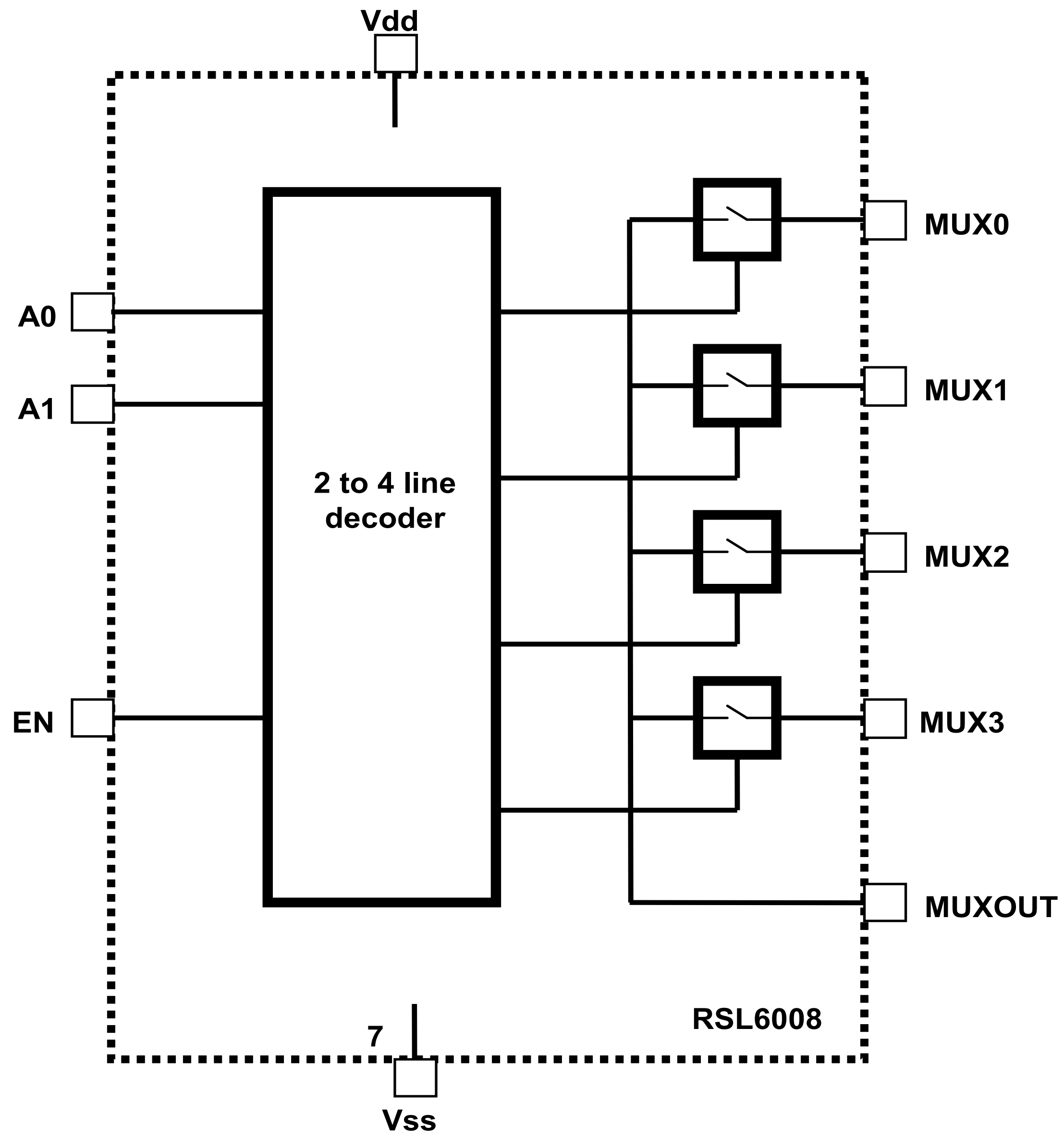
Variation in oscillation frequency as a function of supply voltage

Figure 15



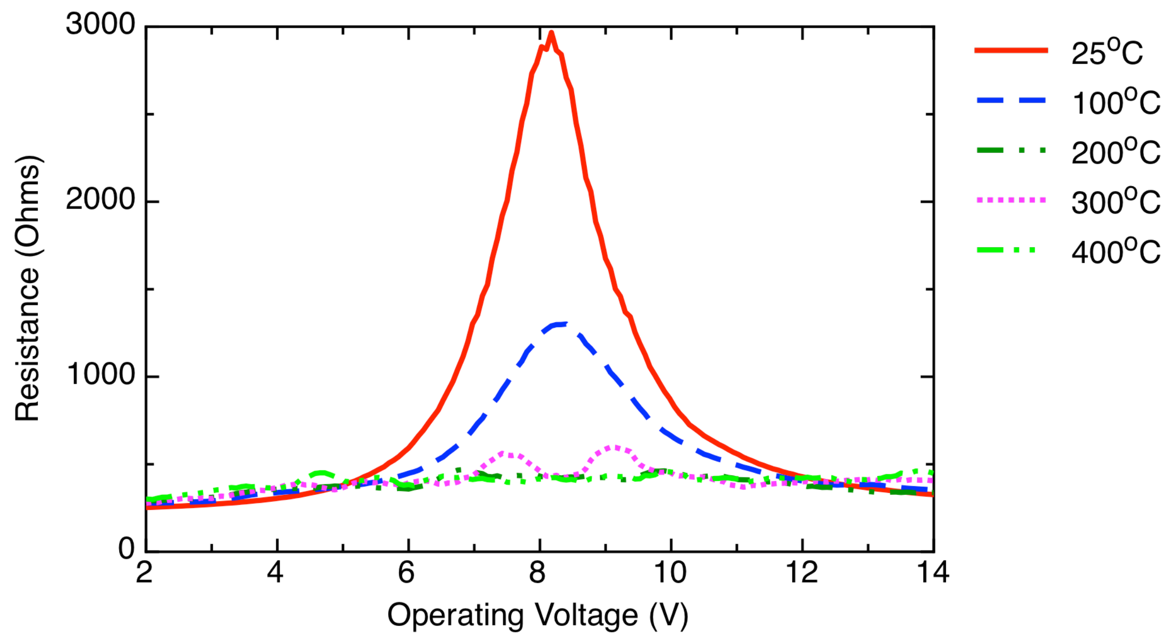
Shift in frequency with temperature for an oscillator operating at 15V

Figure 16



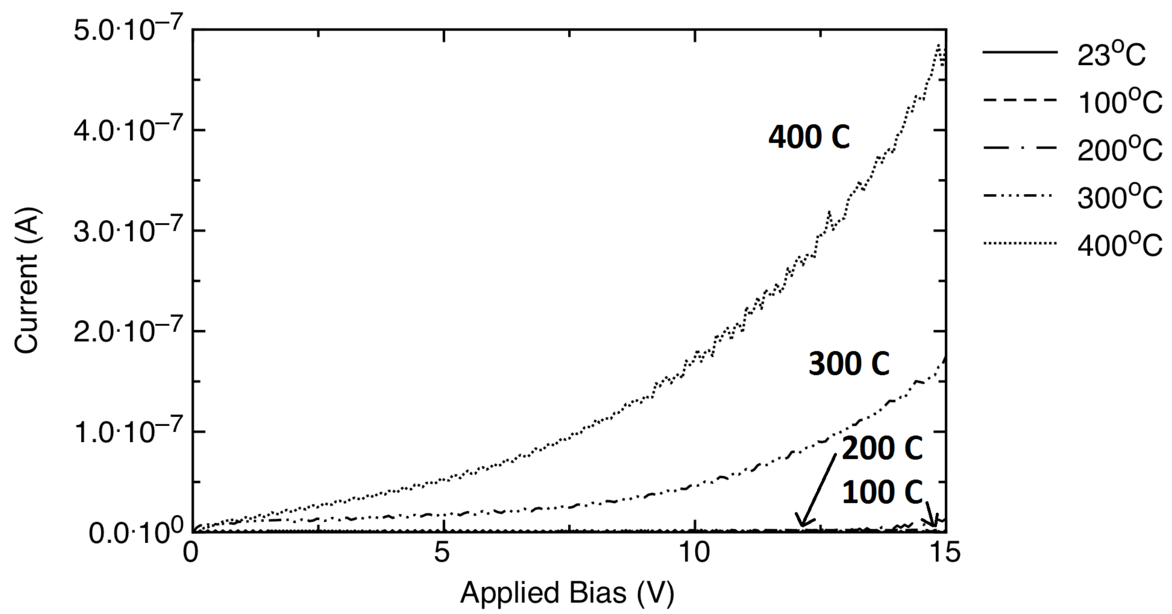
Block diagram of a 4:1 MUX.

Figure 17



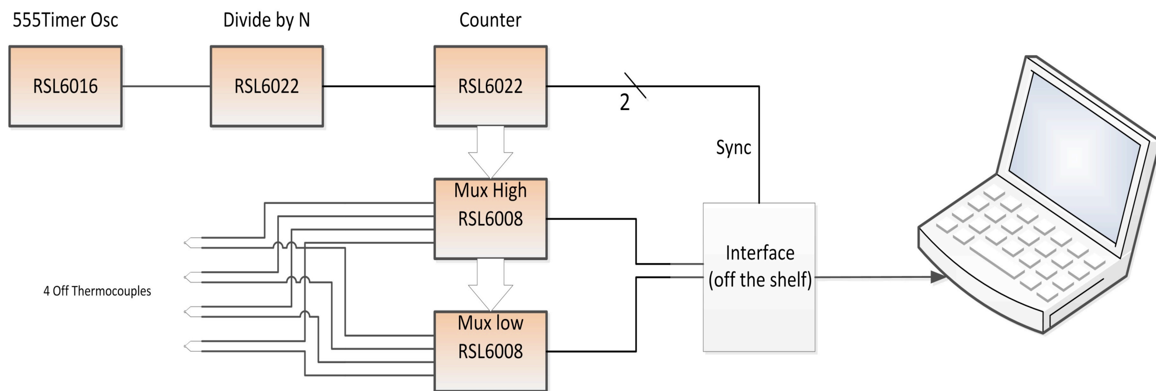
Switch resistance of a 4:1 MUX.

Figure 18



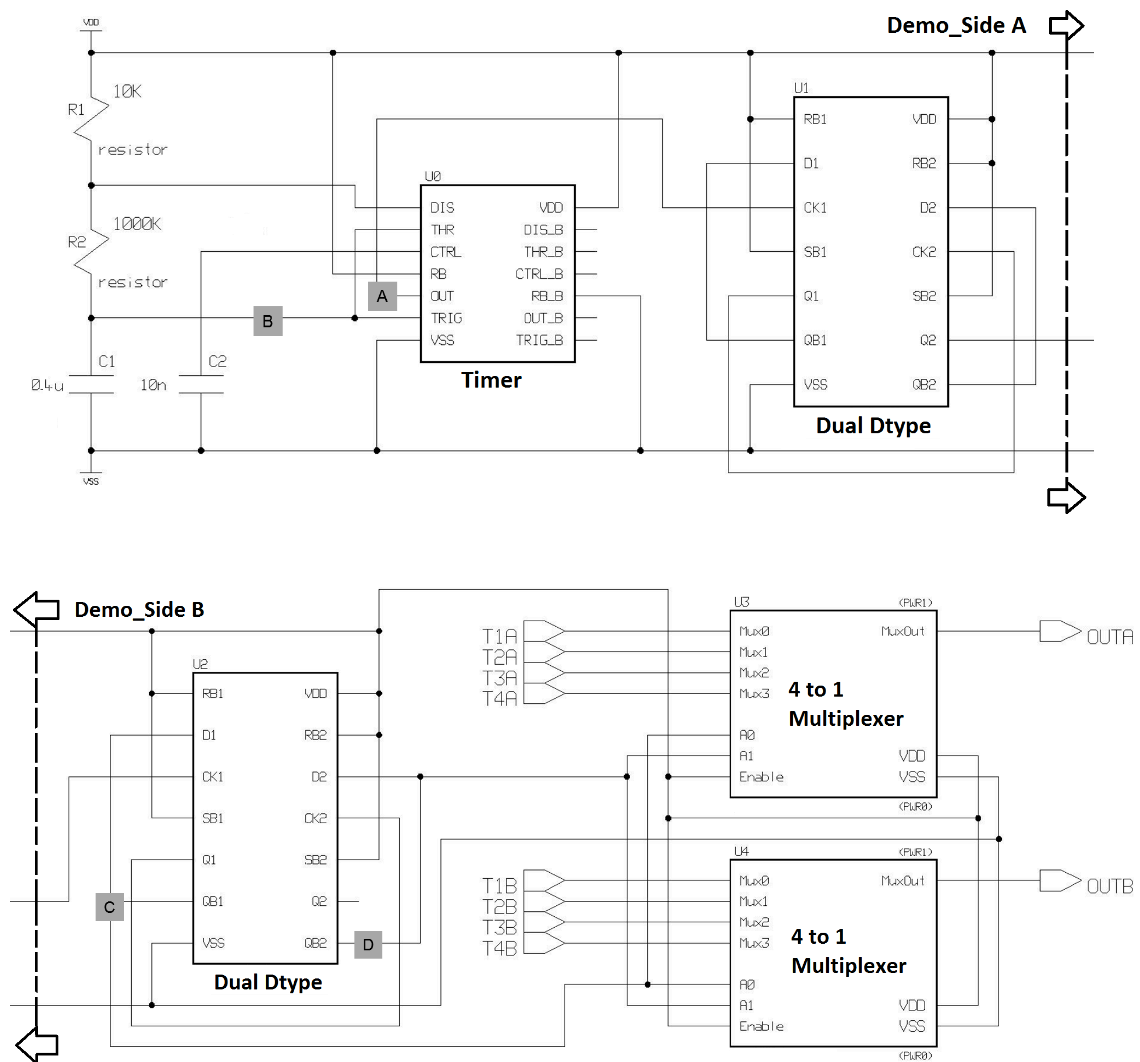
Switch leakage of a 4:1 MUX. Data from room temperature to 200°C are within the noise of the measurement system <1nA.

Figure 19



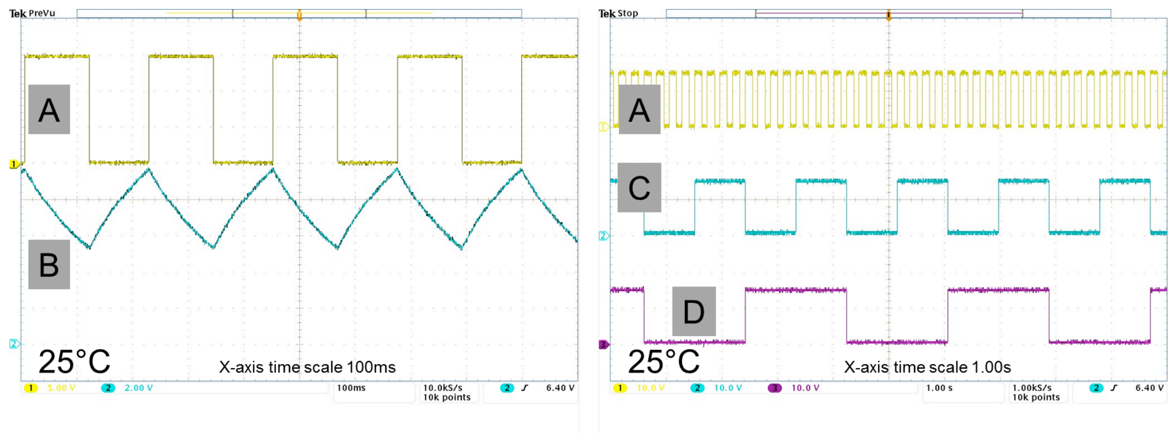
Multiplexer demonstrator schematic diagram which using RSL6016 dual 555 timer, RSL6022 dual D-type flip-flop as both divder and counter, and RSL6008 the 4 to 1 multiplexer for high and low operations.

Figure 20



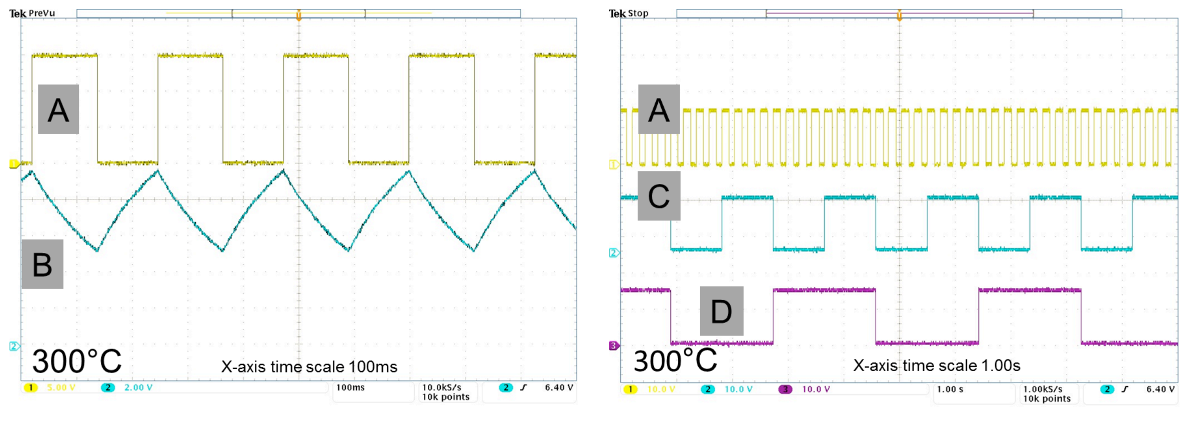
Multiplexer demonstrator schematic diagram with measuring nodes. The circuitry is presented in 2 parts joining by Side A and Side B.

Figure 21



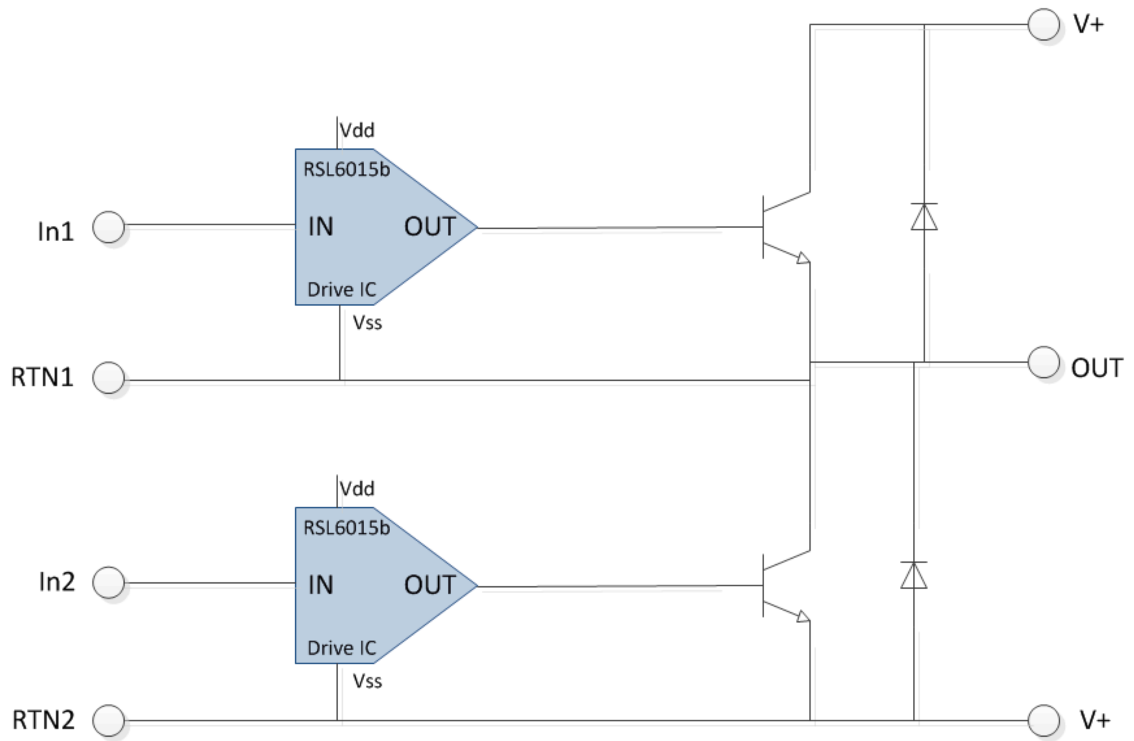
Multiplexer demonstrator inputs and outputs at room temperature.

Figure 22



Multiplexer demonstrator inputs and outputs at 300°C.

Figure 23



Circuit Diagram of a hybrid module using Raytheon RSL6015B drivers.

Figure 24

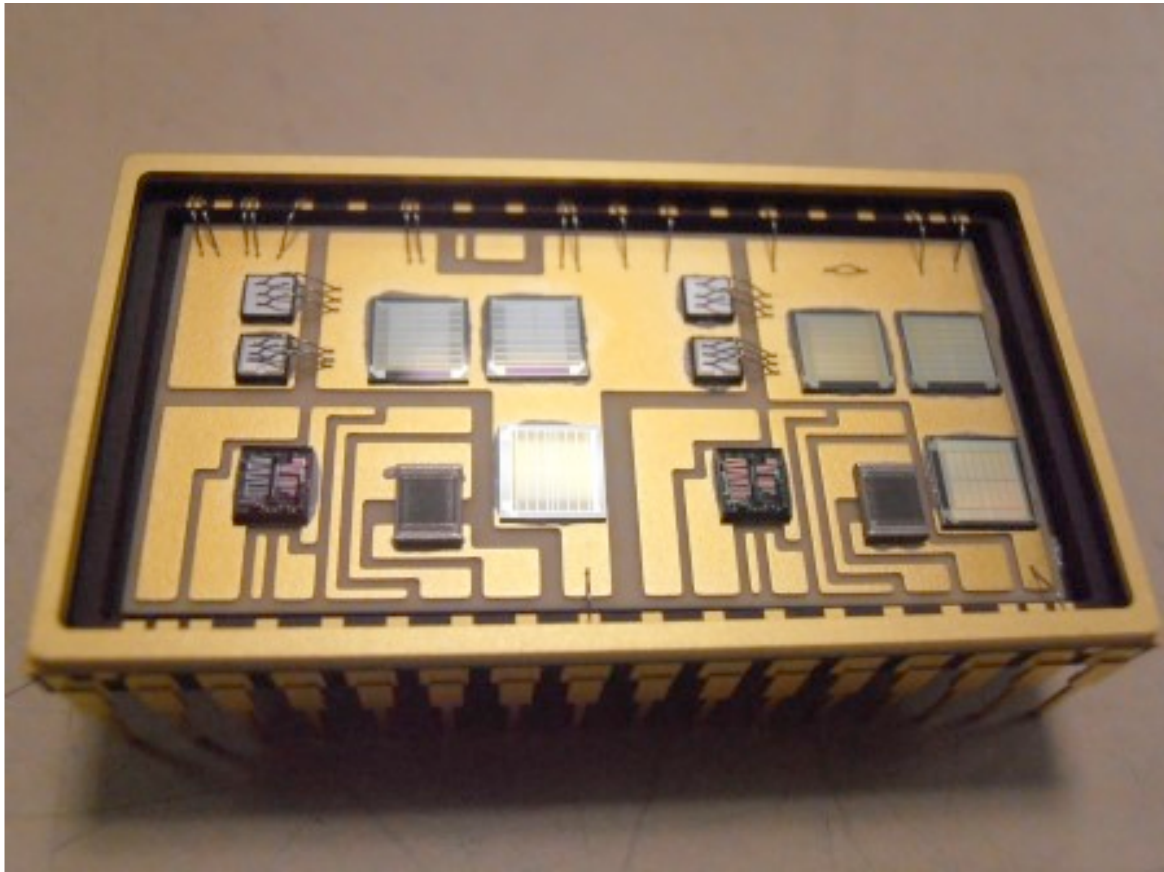
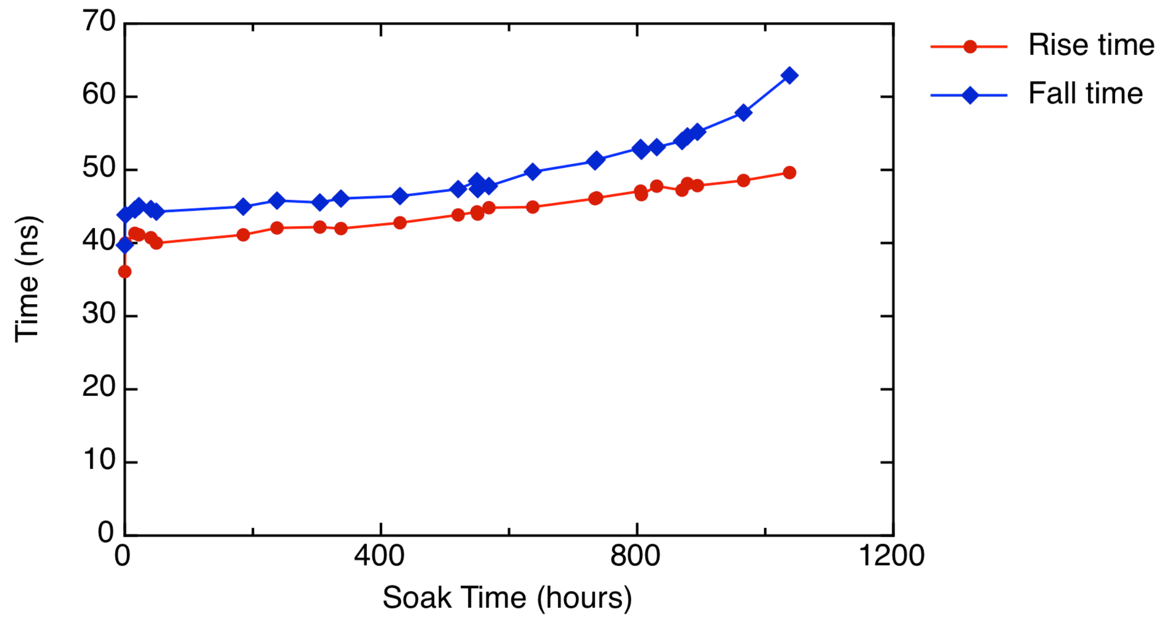


Image of a bridge leg assembly with SiC drivers, transistors and passive devices. The module is packaged in a 32-pin hermetic dual in-line (DIL) ceramic package measuring about 40mm x 23mm.

Figure 25



Rise and fall times of the hybrid module during switching transients