A Quasi-Z-Source Four-Switch Three-Phase Inverter with Null Vector Capability

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Abstract—**In this paper, a novel structure for a four-switch three-phase inverter with the ability of creating a null vector is proposed. This structure utilizes a symmetrical quasi-Z-source network and generates zero output voltage during the shoot-through state, which is similar to the null vector in the conventional six- switch inverter. This vector is used for the remaining time for each switching period. This means that the proposed structure has several advantages over the conventional four-switch inverter, in which two active vectors with opposite directions are necessary for synthesizing a null vector. These two vectors increase the switching losses due to the current circulation through these active states. Moreover, the number of switching states increases because of applying two opposite vectors. However, this problem does not exist in the proposed topology. To decrease the output current distortion and to minimize the number of switching events per each cycle, a new switching pattern is proposed, too. Also, fluctuations of the two split capacitors in the dc-link are considered in the closed-loop modulation method, which balances the output voltages and decreases current THD by 0.7%. To validate the proposed topology and the given pulse width modulation approach, its mathematical analyses are given here, in detail. Also, simulations and experimental verification have been performed on a 1 kW prototype inverter.**

***Index Terms*— Four-switch three phase inverter (FSTPI), pulse width modulation inverters, quasi-Z-source inverter, shoot-through, space vector pulse width modulation (SVPWM).**

I. Introduction

Recently, reliability and cost-efficiency issues have become important preoccupations by the development of modern industries [1], [2]. Using a four-switch three-phase voltage source inverter (FSTPI) can reduce cost, compared to the conventional three- phase six-switch inverter (SSTPI), due to the reduced number of power switches [3]- [5]. Moreover, the FSTPI can be applied as the post-fault rehabilitated state of the SSTPI, when a fault is occurring in one of its phases [6], [7]. Instead of generating six active vectors and two null vectors of the SSTPI structure, the conventional FSTPI inverters produce four main vectors without any null vectors [8]. Consequently, two opposite active vectors are applied when a zero vector is needed to complete the switching period [1], [8]. One of the significant disadvantages of this procedure is increasing the conduction losses of the power semiconductors when active vectors are applied, as compared to utilizing the zero vectors to synthesize the reference voltage. However, the FSTPI is a promising three-phase inverter structure, because of its reduced cost and its post-fault performance. The FSTPI has been reported widely in some researches, in terms of control strategy and inverter operation [8], [9].

On the other hand, Z-source inverters (ZSIs) are attractive for power electronics researchers, due to their wide applications in variable speed control drives, renewable energy, and battery charger systems [10]- [14]. The main feature of the ZSIs is their impedance networks with shoot-through capability that is used to buck or boost the voltage. During the shoot-through state, the upper and lower switches of the ZSIs are simultaneously turned on, while this state is not allowed in the traditional voltage-source inverters (VSI) [15], [16]. However, the conventional ZSI with X-shaped impedance source, proposed by Peng [17], has some drawbacks such as: inrush current during the start-up and also high voltages and currents stresses on the components [18]- [23]. The voltage-fed quasi-ZSI (q-ZSI), proposed in [19] with reduced capacitor voltage stress, draws a continuous current. Due to the presence of the input inductor in the q-ZSI, inrush current is decreased, significantly [24], [25].

Different structures of the FSTPI that utilize quasi Z-source (q-ZS) have been introduced in [3], [2] which function as cost-effective and post fault topology of the SSTPI. These q-ZS structures are generally asymmetrical which eliminate the neutral point of the q-ZS impedance network for connecting the third phase in the FSTPI inverters as depicted in Fig. 1. Generally, the third phase of the FSTPI inverters must be connected to the middle point of the input dc-link, otherwise, the output waveform distortion is increased.

Here, a symmetrical four-switch q-ZSI inverter is proposed that can create a neutral point in the dc-link of the FSTPI. Contrary to the existing FSTPI inverters, the proposed structure can provide a null vector through the shoot-through state. To increase the efficiency of a FSTPI, applying a null vector is much more efficient than using the two active vectors with opposite directions. When the active vectors are utilized to synthesize the reference voltage, the active power circulates in the inverter and increases its conduction losses. In contrast, by applying the null vector, the output voltage of the inverter is zero and power does not flow from the input to the load. Moreover, switching events are reduced due to the completion of the remaining time in each switching period by shoot-through state and the opposite vectors procedure is also eliminated. Here, a Pulse Width Modulation (PWM) approach is also used for generating duty cycles for one null and four active vectors, properly. Moreover, the dc-link capacitors voltage variations are also considered to eliminate the output voltage distortions.

The symmetrical q-ZS FSTPI topology is introduced in Sec. II. Next, the space vector PWM approach and time weights for different vectors are given in Sec. III. Also, an effective approach for eliminating the effects of the dc-link voltage unbalances is given in Sec. IV. The proposed inverter design procedure is given in Sec. V. Then, simulation and experimental results are given in Sections VI. Finally, the work is concluded in Sec. VII.

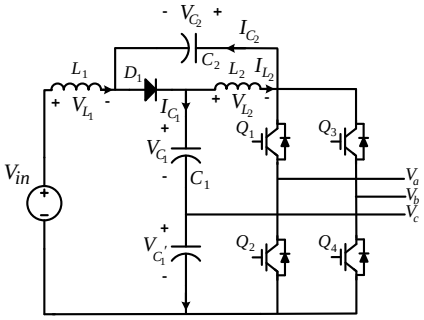


Fig. 1. Conventional q-ZSI FSTPI [2].

II. Proposed Topology

The proposed q-ZS FSTPI topology is illustrated in Fig. 2. Similar to the conventional q-ZSI, this balanced topology has two different operation modes on its dc side: the non-shoot-through state, and the shoot-through state, where both switches are conducting simultaneously at least in one of the phases. During the shoot-through state, two legs of the inverter are short circuited and equivalent circuit viewed from the midpoint of two dc-link capacitors is symmetrical. During this state, V_C reaches zero and causes a null vector for a three-phase output load. Converter's controller utilizes the shoot-through time interval to buck or boost the inverter dc-bus and adjusts the desirable output voltage for the load.

Initially, it is assumed that C_1 and C_2 are large enough and the same voltages are applied to them, i.e., $V_{C_1} = V_{C_1'} = \bar{E}/2$. Here, $\bar{E}$ denotes the average dc-link voltage of the inverter. Moreover, it is assumed that $L_1 = L_1'$, $L_2 = L_2'$ and $C_1 = C_1'$. The equivalent circuits for both operation states (i.e., shoot-though and not-shoot-through states) are depicted in Fig. 3. Considering Fig. 3 (a), during the non-shoot-through interval (T_1), two diodes (i.e., D_1 and D_2) are turned on and we have the same equations as in the conventional q-ZSI converter. Also, from Fig. 3 (b), during the shoot-through state time interval (T_0), the two output legs of the FSTPI provide zero state, similar to the conventional six-switch three-phases q-ZSI converter. However, the load's third phase is connected to the midpoint of the capacitors (V_Z), as depicted in Fig. 3 (b). There are two symmetrical q-ZSI parts on upper and lower sides of the proposed FSTPI inverter that cause similar voltages on the axis of symmetry and consequently, $V_Z = 0$. Therefore, voltage of the third phase is also zero and unlike in the existing topologies in the literatures so far such as [2], [3] and [8], the proposed four-switch converter can indeed provide a null vector as well. In other words, the proposed q-ZSI provides a zero vector in each switching period during T_0 time interval.

From Fig. 3, by applying the state space average analysis method [26], maximum voltages values across the electrolytic capacitors can easily be derived as follows:

$$V_{C_1} = V_{C_1'} = \big((1-D)/\big(2(1-2D)\big)\big)V_{in} \qquad (1)$$

$$V_{C_2} = V_{C_2'} = \big(D/\big(2(1-2D)\big)\big)V_{in} \qquad (2)$$

Here, shoot-through duty ratio is $D = T_0/(T_0+T_1)$. Also, T_0 and T_1 are shoot-through and non-shoot-through states time intervals, respectively.

The dc-link peak voltage value is also given as:

$$V_{pn} = V_{C_1} + V_{C_1'} + V_{C_2} + V_{C_2'} = V_{in}/(1-2D) \qquad (3)$$

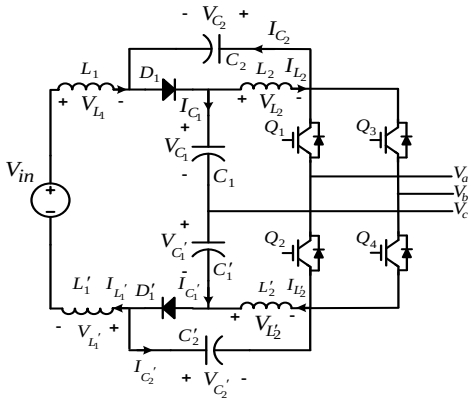


Fig. 2. Proposed q-ZSI FSTPI topology

III. Space Vector Modulation

Output voltage quality of the FSTPI inverter depends on the dc-link voltage fluctuation and the generated PWM pattern to control the three phase balanced currents. To properly choose the switching sequence by using a space vector modulation approach, the phase quantities are usually transformed to the α-β components of the Clark stationary reference frame [26]. Depending on the motor winding connections, there are two different kinds of connections for the load (i.e., Wye and Delta), that affect the generation of the IGBTs PWM gate-drive pulses. Here, these connections are studied for investigating the effects of motor structure on the PWM pattern. A three-phase induction motor, with Wye connected windings, is shown in Fig. 4 (a). The induction motor is assumed to be symmetrical and has no neutral connection. The line-to-neutral output voltages of the FSTPI inverter, i.e., v_a ,v_b, and v_c are given by pole voltages v_{a0}, v_{b0} and v_{N0} as follows:

$$\begin{cases} v_a = v_{a0} - v_{N0}; v_{a0} = (2q_1 - 1)\bar{E}/2 \\ v_b = v_{b0} - v_{N0}; v_{b0} = (2q_2 - 1)\bar{E}/2 \\ v_c = -v_{N0} \end{cases} \qquad (4)$$

Where, q_1 and q_2 are binary variables. Here, state '1' means that the upper switch in the corresponding leg is "on" and its

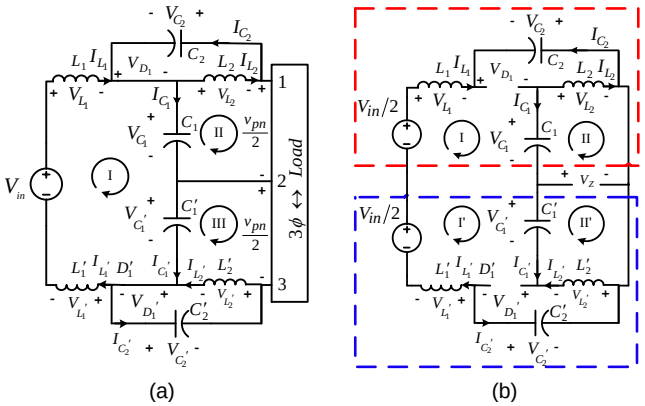


Fig. 3. Equivalent circuits of the proposed q-ZSI FSTPI with continuous input current during the two different states (a) non-shoot-through state and (b) shoot-through state.

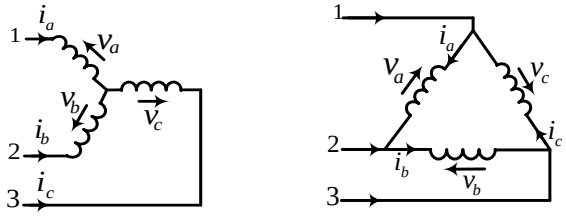


Fig. 4. Voltage vector distributions in the q-ZSI FSTPI: (a) the Wye windings connection and (b) the Delta windings connection.

complementary switch is "off". Also, '0' means the lower switch is "on" and the upper one is "off". Phase-to-ground voltages for the two legs of the inverter can be written as a function of q_1 and q_2. Similar to the conventional Z-source inverter, both switches S_1 and S_2 can be simultaneously turned on and the resulting zero shoot-through time interval can be used to boost or buck the dc-bus voltage. Similar to the other balanced three-phase systems, v_{N0} is the voltage difference between the neutral point of the load (i.e., N) and the dc-bus midpoint of the capacitors.

The proposed structure has 4 non-shoot-through states that generate four vectors ($V_1, V_2, V_3,$ and V_4), and one shoot-through state that causes a zero vector (V_5). According to the Clark transformation, α-β component of these four vectors are given in Table I. The four aforementioned vectors splits the α-β plane to four sections, as depicted in Fig. 5(a), where vectors V_1 and V_2, are in opposite directions of V_3 and V_4, respectively. Amplitudes of the even pair vectors (i.e., V_2 andV_4) are $\sqrt{3}$ times larger than the amplitudes of the odd pair vectors (i.e., V_1,V_3).

Delta windings connection of the induction motor is shown in Fig. 4 (b). Amplitudes of these vectors are $\sqrt{3}$ times higher than the Wye connection ones. Moreover, they are rotated counterclockwise by $\pi/3$ radians around the origin of the α-β plane coordinates, as compared to Fig. 5 (a). Using a similar analysis, the vectors distribution of the delta connection of the load is depicted in Fig. 5 (b).

For the sake of brevity, all space vector mathematical analyses are only given for the Wye connection, here. However, similar relationships can straightforwardly be obtained for the delta configuration of the load, by applying few changes in the load structure analyses.

Let's assume the voltage value that must be realized, V_{ref}, is located in one of the four regions, the area between the two standard vectors, as illustrated in Fig. 5 (a). If the complete switching period, T_s, is available to realize the V_{ref} value by the FSTPI, then the following relation must be satisfied:

$$V^*_{refj} = \sum_{i=1}^{5} d_{ij} V_i, \qquad (5)$$

$$d_{ij} = T_{ij}/T_s \quad \text{and} \quad \sum_{i=1}^{5} d_{ij} = 1 \qquad (6)$$

Here, T_{ij} is the switching time and d_{ij} is duty cycle for vector V_i with suffix $i\epsilon\{1,\dots,5\}$, and $j\epsilon\{1,\dots,4\}$ denote the region number. Now the problem is how to find these time weights for any given V^*_{refj} value for each region. It should be mentioned that in the conventional three-phase inverter when time weights are determined to satisfy (5) and (6), one of the null vectors is used for the rest of the switching period to completely fulfill T_s. In the FSTPI, there are two vectors in each region. Controller assigns the two nearest vectors for every desired reference value that effectively synthesize the desired output voltage. These two vectors are enough for the output voltages corresponding to the reference voltage. However, each switching cycle is $1/f_s$, and the extra time should be divided evenly between the two vectors with opposite directions. Nevertheless, in the proposed topology, V_5 behaves like a null vector under the ideal condition, where $V_{C_1} = V_{C_1'}$. As shown in Table I, this vector boosts the dc-link peak voltage value across the input of the inverter by:

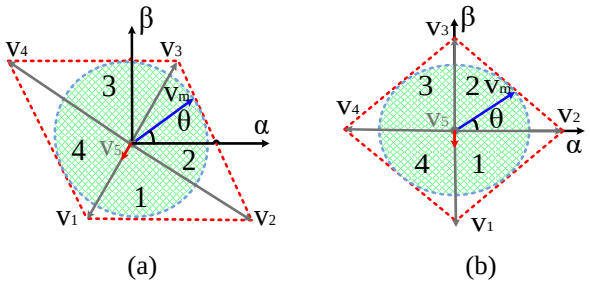


Fig. 5. Voltage vector distributions in the q-ZSI FSTPI: (a) the Wye windings connection and (b) the Delta windings connection.

TABLE I
IDEAL VECTORS OF THE PROPOSED INVERTER FOR THE WYE CONNECTION

(S_1,S_2,S_3,S_4)	Vectors	(V_α, V_β)
(0,1,0,1)	V_1	$(-1/2\sqrt{6}, -1/2\sqrt{2})V_{dc}$
(1,0,0,1)	V_2	$(\sqrt{3}/2\sqrt{2}, -1/2\sqrt{2})V_{dc}$
(1,0,1,0)	V_3	$(1/2\sqrt{6}, -1/2\sqrt{2})V_{dc}$
(0,1,1,0)	V_4	$(-\sqrt{3}/2\sqrt{2}, -1/2\sqrt{2})V_{dc}$
(1,1,1,1)	V_5	(0,0)

$$\beta = \frac{1}{1-2(t_5/T_s)}; d_\beta = \frac{1}{2}\left(1-\frac{1}{\beta}\right) \qquad (7)$$

So, the value of T_5 is directly obtained from the desired Z-source boost gain, and the remaining switching time is completed with V_5 or other vectors in the opposite direction, depending on the shoot-through control method. d_β is effect of β on the time coefficients of each vectors time weights. As shown in Fig. 6, three carrier-based methods can be used to control the shoot-through time interval. The simple boost control uses two straight lines as references, and assigns a fixed duty cycle for shoot-through during each switching period. The voltage gain for the simple boost shoot-through control is given in (7). The constant boost control uses two sinusoidal envelope curves as references and the voltage gain in the steady state is:

$$\beta = \frac{1}{\sqrt{3}\left(1-(t_5/T_s)\right)-1}; d_\beta = 1-\frac{1}{\sqrt{3}}\left(1+\frac{1}{\beta}\right) \qquad (8)$$

In these two control methods, in the inactive part of the switching period, both shoot-through and zero vectors must be applied. Since zero vectors are not possible for conventional FSTPI, opposite vectors should be used to fill the remained time. One of the major concerns of using opposite vectors is that they increase switching events in each switching period. In contrast, the maximum boost control uses the desired three-phase voltage envelop as a reference. In the inactive part of the switching cycle, only the shoot-through state is applied, as shown in Fig. 6. the shoot-through state in the proposed FSTPI behaves similarly to the null vector in SSTFI, it can be applied to the entire inactive time period. The voltage gain for the maximum boost method can be expressed as follows:

$$\beta = \frac{\pi}{3\sqrt{3}\left(1-(t_5/T_s)\right)-\pi}; d_\beta = 1-\frac{\pi}{3\sqrt{3}}\left(1+\frac{1}{\beta}\right) \qquad (9)$$

Due to the fact that the number of switching events per cycle is less in the maximum boost approach, in this paper, the proposed converter is evaluated using this method.

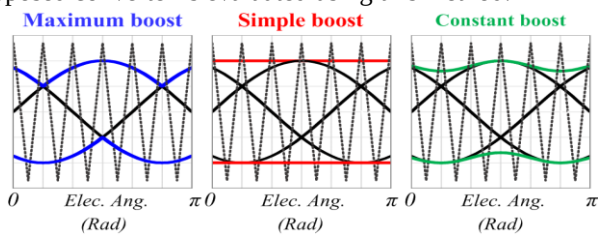


Fig. 6. Different boost control methods for a q-ZSI.

Assuming ideal condition ($V_{C_1} = V_{C_1'} = \bar{E}/2$) keep for different regions of the SVM diagram, It can be shown that switching time weights for all five vectors can be identified by applying (5) and (6). The time weight of each vector for each region is given as follows:

1) Region 1: $-2\pi/3 \le \theta \le -\pi/6$

In this region, the two nearest vectors are V_1 andV_2 that they are used to achieve the desired reference voltage. The vector V_5 is used for the remaining switching time and its time weight coefficient is given in (9). Also, duty cycles of the others vectors are calculated as follows:

$$d_{11} = -\sqrt{6}M\sin(\theta + \pi/6) \quad (10)$$

$$d_{21} = -\sqrt{2}M\sin(\theta - \pi/3) \quad (11)$$

2) Region 2: $-\pi/6 \le \theta \le \pi/3$

The two main vectors in this region are V_2 and V_3, while V_1 and V_4 are not used here. Using (8), the duty cycles values of different vectors in the active state are:

$$d_{22} = -\sqrt{2}M\sin(\theta - \pi/3) \quad (12)$$

$$d_{32} = \sqrt{6}M\sin(\theta + \pi/6) \quad (13)$$

3) Region 3: $\pi/3 \le \theta \le 5\pi/6$

The two main vectors are V_3 and V_4, here. For the conditions given in (8) and (9), the duty cycles for these vectors are:

$$d_{33} = \sqrt{6}M\sin(\theta + \pi/6) \quad (14)$$

$$d_{43} = \sqrt{2}M\sin(\theta - \pi/3) \quad (15)$$

4) Region 4: $5\pi/6 \le \theta \le -2\pi/3$

V_1 and V_4 are used to achieve the desired value, while V_3 and V_2 are not used in this region. Also, duty cycles can be obtained as follows:

$$d_{14} = -\sqrt{6}M\sin(\theta + \pi/6) \quad (16)$$

$$d_{44} = \sqrt{2}M\sin(\theta - \pi/3) - d_\beta \quad (17)$$

IV. Improved Space Vector PWM with Unbalanced DC-Link

Despite the assumption that $V_{C_1} = V_{C_1'}$, actual voltages of C_1 and C_1' may be different in practice. As a result of the third phase being connected to the midpoint of the two series connected capacitors in the FSTPI, low frequency currents cause V_{C_1} and $V_{C_1'}$ to fluctuate with the output voltage frequency. Moreover, dc-link oscillations are caused by the uncontrollable input rectifiers that are mainly utilized in some applications, such as three-phase motor drives. So, the dc-link voltage might be different from the expected value, as mentioned before. Therefore, under real conditions, the voltages across $C_1$and C_1' will have some oscillations which lead to unbalances in the three-phase output voltages. Clearly, instantaneous actual value of $V_{C_1'}$ and V_{C_1} should be taken into account for generating exact duty cycles value in (10)-(17). According to the given values for vectors in Table II, α-β components of all main vectors depend on the instantaneous voltages of C_1' and C_1.

Since, practically $V_{C_1} \neq V_{C_1'}$, there will be non-zero components for the vector V_5, in the α-β plane. Depending on whether $V_{C_1} > V_{C_1'}$ or $V_{C_1} < V_{C_1'}$, two vectors are created with different directions for this vector. When, $V_{C_1} > V_{C_1'}$, V_5 is in line with V_1 , as shown for the Wye windings connection in Fig. 7 (a) and for the delta windings connection in Fig. 7 (b). Under this condition, V_3 duty cycle should be increased, in order to compensate the effect of the V_5 vector on the output of the FSTPI. While, regarding to the condition $V_{C_1} < V_{C_1'}$, V_5 will be on the opposite direction of V_1 and it's time duration grows up for eliminating the effect of V_5.

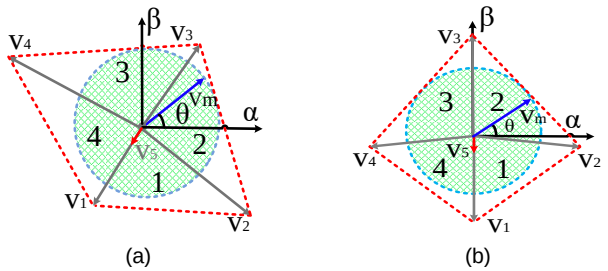


Fig. 7. Voltage vector distributions in q-ZSI FSTPI: (a) Wye windings connection and (b) Delta windings connection.

Furthermore, there are two parts for switching times of V_1 and V_3. Similar to the previous section, the first part of the switching time for these two main vectors, are used to satisfy the desired reference in regions from 1 to 4. However, the second part of V_1 and V_3 switching times, d_{1c} and d_{3c} respectively, are applied to compensate the effect of V_5. Their values are given as follows:

$$d_{1c} = T_{1c}/T_s = 1/2\left(1 - V_{C_1'}/V_{C_1}\right)(1 - 1/\beta) \quad (18)$$

$$d_{3c} = T_{3c}/T_s = 1/2\left(V_{C_1'}/V_{C_1} - 1\right)(1 - 1/\beta) \quad (19)$$

Therefore, to obtain the exact time duration of each vector, (5) and (6) must be met by considering new vectors, as shown in Fig. 7 (a). Here, the time coefficients for the two cases of $V_{C_1} > V_{C_1'}$ and $V_{C_1} < V_{C_1'}$ are given, according to the Table II. Considering Fig. 7 (b), similar analyses are performed to obtain the duty cycles in the delta windings connection.

A. Mode 1: $V_{C_1} > V_{C_1'}$

When $V_{C_1} > V_{C_1'}$, according to Table II, V_5 has the same direction of vector V_3. Therefore, to compensate the effect of V_5, vector V_1 is applied in the opposite direction during the T_{1c} .

1) Region 1:$-2\pi/3 \le \theta \le -\pi/6$

In this region, the two nearest vetors to fulfil the appropriate reference are V_1 and V_2, and by replacing the given values in Table II into (5) and (6), d_{11} and d_{21} are obtained. As mentioned earlier, shoot-through duty cycle (i.e.,T_5) given in (9), is determined by the voltage gain (β). For eliminating the effect of shoot-through vector (i.e., V_5), V_1 duty cycle is increased by d_{1c}. Depending on the reference region, there are two different states to achieve this. In the first case, V_1 is one of the main vectors and its time weight is increased by d_{1c}. Nevertheless, in the second case V_1 isn't one of the main vectors in regions 2 and 3, as mentioned in Fig. 7. Thus, d_{1c} is subtracted from V_3 time weight, which is one of main vectors in

TABLE II
MODIFIED VECTORS FOR THE WYE CONNECTION OF THE LOAD

Vectors	(V_α, V_β)
V_1	$\left(-1/\sqrt{6}, -1/\sqrt{2}\right)V_{\dot{C}}$
V_2	$\left(\sqrt{2/3}\left(V_{C_1} + V_{C_1'}/2\right), -1/\sqrt{2}\,V_{C_1'}\right)$
V_3	$\left(1/\sqrt{6}, -1/\sqrt{2}\right)V_{C_1}$
V_4	$\left(-\sqrt{2/3}\left(V_{C_1'} + V_{C_1}/2\right), -1/\sqrt{2}\,V_{C_1}\right)$
V_5	$\left(\sqrt{1/6}\left(V_{C_1} - V_{C_1'}\right), 1/\sqrt{2}\left(V_{C_1} - V_{C_1'}\right)\right)$

this region. In the switching events where d_{1c} is greater than the time coefficient of V_3 and resulting duty cycle sign is negative, then V_1 is applied instead of V_3. Duty cycles for the main vectors to achieve the desired voltage in this region are:

$$d_{11} = -\frac{\sqrt{2}V_{ref1}}{V_{C_1'}}\sin\theta - \frac{\sqrt{2}V_{ref1}}{V_{C_1}+V_{C_1'}}\sin\left(\theta-\frac{\pi}{3}\right)+d_{1c} \quad (20)$$

$$d_{21} = \left(\sqrt{2}V_{ref1}/\left(V_{C_1}+V_{C_1'}\right)\right)\sin\left(\theta-\frac{\pi}{3}\right) \quad (21)$$

2) Region 2: $-\pi/6 \le \theta \le \pi/3$

The two main vectors in this region are V_2 and V_3 that are used to generate the desired reference value. Similar to region 1, V_1 with weight d_{1c} is applied to compensate the effect of vector V_5 in the shoot-though state. This vector is applied for all the remaining time. The corresponding voltage gain is given in (9), too. Consequently, weight coefficients for the two main vectors in this region are obtained as follows:

$$d_{22} = \left(\sqrt{2}V_{ref2}/\left(V_{C_1}+V_{C_1'}\right)\right)\sin\left(\theta-\frac{\pi}{3}\right) \quad (22)$$

$$d_{32} = \frac{\gamma_2 V_{C_1'}}{V_{C_1}+V_{C_1'}}\sin\left(\theta-\frac{\pi}{3}\right)+\gamma_2\sin\theta-d_{1c} \quad (23)$$

$$\gamma_2 = \sqrt{2}V_{ref2}/V_{C_1} \quad (24)$$

3) Region 3: $\pi/3 \le \theta \le 5\pi/6$

The main vectors in this region are V_3 and V_4, which are used to achieve the desired value, as defined in Table II. These vectors are placed in (5) and (6) to derive the duty cycle coefficients. Again, V_1 with gain d_{1c} compensates the effect of V_5. The required quantities for generating PWM signals in this region are given as follows:

$$d_{33} = -\frac{\gamma_3 V_{C_1}}{\sqrt{3}\left(V_{C_1}+V_{C_1'}\right)}\sin\left(\theta-\frac{\pi}{3}\right)+\gamma_3\sin\theta-d_{1c} \quad (25)$$

$$\gamma_3 = \sqrt{2}V_{ref3}/V_{C_1} \quad (26)$$

$$d_{43} = \left(\sqrt{2}V_{ref3}/\left(\sqrt{3}\left(V_{C_1}+V_{C_1'}\right)\right)\right)\sin\left(\theta-\frac{\pi}{3}\right) \quad (27)$$

4) Region 4: $5\pi/6 \le \theta \le -2\pi/3$

Two main vectors in this region are V_1 and V_4. Here, V_1 with d_{1c} weight is used to eliminate the effect of V_5. Accordingly, the coefficients of the vectors in this region are obtained as follows:

$$d_{14} = \gamma_4\sin\theta - \frac{\gamma_4 V_{C_1}}{V_{C_1}+V_{C_1'}}\sin\left(\theta-\frac{\pi}{3}\right)+d_{1c} \quad (28)$$

$$\gamma_4 = \sqrt{2}V_{ref4}/V_{C_1'} \quad (29)$$

$$d_{44} = -\left(\sqrt{2}V_{ref4}/\left(V_{C_1}+V_{C_1'}\right)\right)\sin\left(\theta-\frac{\pi}{3}\right) \quad (30)$$

B. Mode 2: $V_{C_1} < V_{C_1'}$:

In this case, V_5 and V_1 have the same directions, as mentioned in Table II. Therefore, V_3 with d_{3c} duty cycle must be applied to compensate the effect of V_5.

1) Region 1: $-2\pi/3 \le \theta \le -\pi/6$

The main vectors for all regions under the operation mode 2 are similar to the ones introduced for operation mode 1, except the direction of V_5 which is in the inverse direction. So, the added time for compensating the effect of V_5 for each region (i.e., T_{3c}), must be subtracted from T_1 and must be added to T_3. Here, the d_{21} weight coefficient is given in (21) and d_{11} is:

$$d_{11} = -\frac{\sqrt{2}V_{ref1}}{V_{C_1'}}\sin\theta - \frac{\sqrt{2}V_{ref1}}{V_{C_1}+V_{C_1'}}\sin\left(\theta-\frac{\pi}{3}\right)-d_{3c} \quad (31)$$

2) Region 2: $-\pi/6 \le \theta \le \pi/3$

Two adjacent vectors in this region are V_2 and V_3, by replacing the d_{22} given in (22) and following d_{32} constant in (8) and (9).

$$d_{32} = \frac{\gamma_2 V_{C_1'}}{V_{C_1}+V_{C_1'}}\sin\left(\theta-\frac{\pi}{3}\right)+\gamma_2\sin\theta+d_{3c} \quad (32)$$

3) Region 3: $\pi/3 \le \theta \le 5\pi/6$

V_3 and V_4 are two main vectors near the reference to access the desired value. Moreover, V_3 is used for the remaining time interval in each switching period to compensate the shoot-through effects. Two vectors duty cycle values are given in (27) for d_{43} and following constant for d_{33}:

$$d_{33} = -\frac{\gamma_1 V_{C_1}}{\sqrt{3}\left(V_{C_1}+V_{C_1'}\right)}\sin\left(\theta-\frac{\pi}{3}\right)+\gamma_3\sin\theta+d_{3c} \quad (33)$$

4) Region 4: $5\pi/6 \le \theta \le -2\pi/3$

From (8) and (9), the duty cycles for vectors V_1 is obtained as follows:

$$d_{14} = \gamma_4\sin\theta - \frac{\gamma_4 V_{C_1}}{V_{C_1}+V_{C_1'}}\sin\left(\theta-\frac{\pi}{3}\right)+d_{1c} \quad (34)$$

V_1 time constant similar to mode 1 is given in (30).

Applying the null vector instead of the active vector reduces the conduction losses of the switches. Conducting losses of the power switch during applying opposite vectors is obtained as follows for four switches [27]:

$$P_{on} = \frac{1}{2}\left(V_{CE}.\frac{\hat{I}}{\pi}+r_{CE}.\frac{\hat{I}^2}{4}\right)+M.cos\varphi.\left(V_{CE}.\frac{\hat{I}}{8}+\frac{1}{3\pi}.r_{CE}.\hat{I}^2\right) \quad (35)$$

Where $\hat{I}$ is the maximum value of current passing through the power switch when it is conducting, $V_{CE_{sat}}$ is the collector-emitter saturation voltage of the switches and r_{CE} is the resistance of the IGBT terminals. In the proposed q-ZSI inverter P_{on} reduces significantly when V_5 is applied instead of two opposite vectors.

There are different procedures for generating switching patterns in SVM modulation technique [2], [3]. Proper modulation technique improves the inverter performance by reducing the number of switching events and improves the inverter's efficiency, as well as its reliability. Moreover, one of the advantages of an optimized modulation technique is reduction of the harmonic contents for the output current and voltage of the inverter.

Selecting the appropriate priority for the vector sequence, causes each power switch mode to change once per each switching cycle as clearly shown in Fig. 8. In the proposed method, the switching states of Q_3 and Q_4 are remained

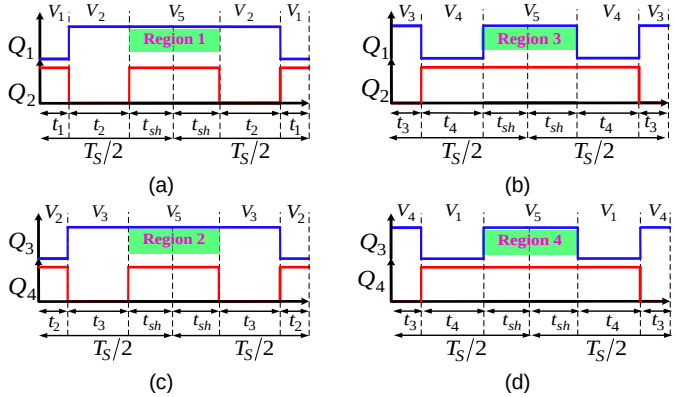


Fig. 8. The proposed switching patterns for 4 regions in the α-β plane: (a) region 1, Q_3=0& Q_4=1, (b) region 3, Q_3=1& Q_4=0, (c) region 2, Q_1=1& Q_2=0, and (d) region 4, Q_1=0& Q_2=1.

unchanged in 1 and 3 regions, as depicted in Fig. 8 (a) and (b), respectively. Moreover, in Fig. 8 (c) and (d), Q_1 and Q_2 maintain their states in regions 2 and 4, which reduces the switching events as well.

The switching period is divided into two symmetrical parts, where T_5 is considered at the middle of T_s. This time is used to define the corresponding weight for V_5, when all four switches of the inverter are turned on simultaneously for applying a shoot-through state on the inverter output. Along the region 1, $T_4 = T_3 = 0$ and two main vectors (i.e., V_1 and V_2) are applied to the remainder of the switching period, as shown in Fig. 8 (a). In this switching algorithm, switches states in the first leg (i.e., Q_1 and Q_2) are changed only once during each half switching period, and the states of the switches in the second leg (i.e., Q_3 and Q_4) are remaining unchanged. A proper sequence for T_3, T_4, and T_5 is depicted in Fig. 8 (b) during region 3, while V_1 and V_2 are not applied along these regions. Similar switching sequences for regions 3 and 4 are shown in Fig 8 (c) and (d).

The q-ZSI closed-loop control is generally developed based on sate-space-averaging method and a small signal model [28] is used with some modifications for dynamic response analysis of the impedance network of the proposed structure in Fig. 2. This structure is actually two symmetrical q-ZSIs that operate, simultaneously. The shoot-through duty cycle to the output capacitor voltage transfer function is [28]:

$$G_{v_{c_1}d} = G_{v_{c_2}d} = \left(\hat{v}_{c_1}(s)/\hat{d}(s)\right)\Big|_{\substack{\hat{v}_{in}(s)=0 \\ \hat{i}_{load}(s)=0}} \tag{36}$$

$$G_{v_c d} = \frac{LI_{11}s + rI_{11} + (1-2D)V_{11}}{LCs^2 + rCs + (1-2D)^2} \tag{37}$$

Where, r denotes the parasitic resistance of the inductors, $L = L_1 = L_2$, $C = C_1 = C_2$, $I_{11} = I_{pn} - 2I_L$, and $V_{11} = V_{C_1} + V_{C_2}$. This transfer function zero and poles are respectively given as:

$$\begin{cases} z = -\dfrac{1}{L}\left(r + \dfrac{(1-2D)V_{11}}{I_{11}}\right) \\ p_{1,2} = -\dfrac{r}{2L}\left(1 \pm \sqrt{1 - \dfrac{4L}{C}\left(\dfrac{1-2D}{r}\right)^2}\right) \end{cases} \tag{38}$$

By increasing the capacitance value, i.e., C, only the given poles are shifted vertically toward the real axis. But, increasing the inductance value, i.e., L, causes both zero and poles to move towards the imaginary axis. Beside the compensating circuit, by changing the inductance and capacitance values the transfer function zero and poles positions can be properly chosen if it is necessary to achieve the desired overshoot or undershoot amplitude and settling time values. To achieve a stable behavior, an inner current controller is utilized, which its open-loop transfer function is given, as previously derived in [28]:

$$G_{i_l d} = (K_2(1-2D)I_{11} + K_1V_{11})/K_2[K_1 + (1-2D)^2] \tag{39}$$

Where, $K_1 = LCs^2 + RCs$, $K_2 = Ls + R$, and R is the equivalent series resistance of the capacitors. Considering (37) and (39), a dc-link voltage control approach for the proposed q-ZSI structure is given in Fig. 9.

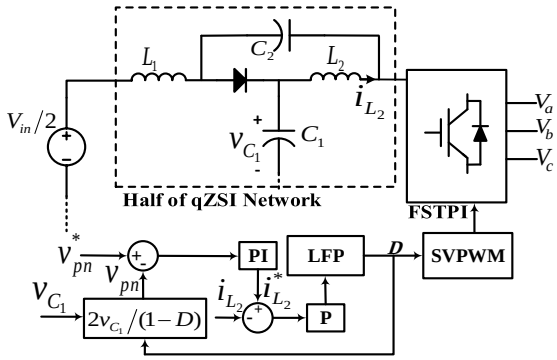


Fig. 9. Proposed q-ZSI closed-loop control block diagram.

Some features of the proposed structure and other existing FSTPI are compared in term of efficiency, number of elements, voltage, and current stress in Table III. Although, voltage boost isn't allowed in [3] and [4], but its effect should be considered to provide the same output power value. On the other hand, to compare different topologies in Table I, the input voltages are not the same, but the output power and switching frequency values for all of these topologies are 1 kW and 10 kHz, respectively. All of the employed devices, i.e. diodes, IGBTs, and inductors are the same for the given four topologies in Table III. Moreover, all of the passive components are designed and simulated based on the same magnetic characteristics and conduction losses. Although, the number of elements increased in the proposed FSTPI converter, some benefits such as: shoot-through protection and reduction of conduction losses are acquired. Semiconductors elements are the most vulnerable part of the power electronic converter and increasing the number of semiconductors reduces the reliability of the inverter. Proposed inverter has smaller number of elements than [2] and [27] that is more reliable. Proposed structure in [3] and [4] isn't able to increase the dc-link voltage for operation after the fault conditions. Moreover, conduction losses are relatively high, due to the use of active vectors to complete the switching cycle.

TABLE III
DIFFERENT TOPOLOGIES COMPARISON

Reference	Voltage gain(G)	Efficiency (%)	Number of IGBTS	Number of Diodes	Number of capacitors	Number of inductors	IGBT voltage stress	IGBT current stress	Capacitors Voltage stress	Diode voltage stress
[2]	$\frac{1}{1-2D}$	92.4	4	5	4	4	$\frac{V_{in}}{1-2D}$	$\frac{2P_{out}}{3V_{in}}\left(D + \frac{2(1-D)}{\pi G\cos\varphi}\right)$	$\frac{1-D}{2(1-2D)}V_{in}$	$\frac{D}{(1-2D)}V_{in}$
[3]	Not allowed	95	4	-	2	-	V_{in}	$\frac{\pi P_{out}}{3V_{in}\cos\varphi}$	$V_{in}/2$	-
[4]	Not allowed	94.5	6	-	2	1	V_{in}	$\frac{\pi P_{out}}{3V_{in}\cos\varphi}$	$V_{in}/2$	-
[27]	$\frac{1-D}{\sqrt{3}(\kappa(1-D)-1}$ $\kappa=\left(1+\frac{1-n}{2(1+n)}\right)$	92	4	4	5	5	$\frac{\sqrt{3}G}{1-D}V_{in}$	$\frac{\sqrt{3}G-(1-D)}{\sqrt{3}GD}\frac{P_{out}}{V_{in}\cos\varphi}$	$\left(\sqrt{3}G-1\right)V_{in}$	$\frac{(\sqrt{3}G)}{1-D}V_{in}$
Proposed FSTP	$\frac{\pi}{3\sqrt{3}(1-D)-\pi}$	95.1	4	2	4	4	$\left(\frac{3\sqrt{3}G}{\pi}-1\right)V_{in}$	$\frac{2P_{out}}{3V_{in}}\left(D+\frac{2(1-D)}{\pi G\cos\varphi}\right)$	$\frac{1-3D\sqrt{3}/2\pi}{2\left(1-3D\sqrt{3}/\pi\right)}V_{in}$	$\frac{\pi DG}{3\sqrt{3}}V_{in}$

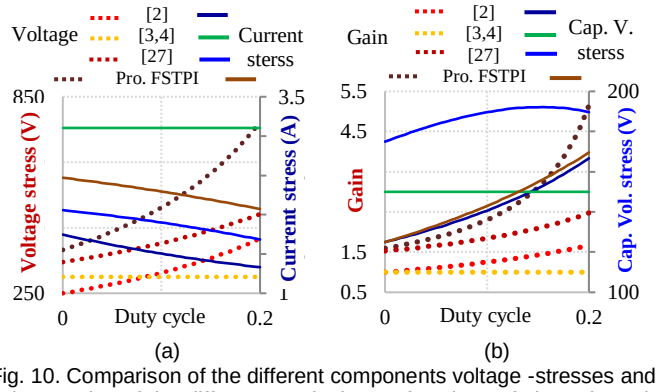


Fig. 10. Comparison of the different components voltage -stresses and voltage-gains of the different topologies as functions of shoot-through duty ratio (a) current and voltage stresses of the IGBTs and (b) voltage-gain and voltage-stresses across the capacitors.

However, reliability increase as result of declining number of utilized elements. In [2] and [27] dc-link boost capability is achieved, but opposite vectors are applied for remained time of every switching cycle and conduction losses increase. Fig. 10 shows a comparison between different q-ZSI topologies in terms of component stress and boost coefficient capability. From Fig. 10 (a) it can be seen that the IGBT current stress in the proposed FSTPI is a relatively higher than the given topologies in [2] and [8]. IGBTs and capacitors are shown in Fig 10 (a) and (b), respectively.

Their values are slightly increasing in [2], [27] as well as in the proposed q-ZSI as shoot-through increases, but in [3] and [4] the voltage stresses remained unchanged due to the inverter constant output voltage. Fig. 10 (b) illustrates the voltage gain versus the shoot-through duty cycle of four q-ZSI FSTPIs. Proposed q-ZSI FSTPI obtains a much higher boost factor compared to the three other q-ZSIs at the same shoot-through duty cycle value.

V. The Proposed Inverter Design Procedure

Here, a design procedure is introduced to properly calculate the inverter parameters, including the inductances and the capacitances values. Generally, in a switching power inverter the switching frequency is limited due to the various aspects, such as: loss limitation and availability of the power switches and diodes. One of the most important concerns for the impedance network in a q-ZSI inverter is minimizing the currents and voltages ripples values. Like the other q-ZSIs, for the given switching frequency, inductances values of the impedance network identify the currents ripples values during the shoot-through state, as depicted in Fig. 3 (b). During this state, the inductors currents rise, linearly. So, their inductances values can be identified, easily.

$$L_1 = L_1' = L_2 = L_2' = V_L D T_s / 2\Delta I \qquad (40)$$

Where, ΔI is each inductor allowed current ripple and V_L is the applied voltage across each inductor. Here, all four inductors are considering the same to simplify the analyses and to achieve a symmetrical topology. For $V_{in} = 250\,V$, $D = 0.07$, and $f_s = 10\,kHz$, the required inductances are equal to $500\,\mu H$ for the given current ripple of $1.75\,A$.

All capacitors in the impedance network of the introduced q-ZS inverter are connected in series during the non-shoot-through state. Therefore, summation of their voltages is limited by the inverter input voltage. The capacitances expressed as follows:

$$C_1 = C_1' = 2I_{C_1}(1-D)T_s/\left(\Delta(V_{C_1} + V_{C_1'})\right) \qquad (41)$$

$$C_2 = C_2' = 2I_{C_2}(1-D)T_s/\left(\Delta(V_{C_2} + V_{C_1'})\right) \qquad (42)$$

In which, I_L is the inductor current average value. Applying a well-balanced three-phase output load to the inverter, its output power and each phase voltage values are also identified, easily.

$$P_{out} = 3 v_a i_a \cos\varphi \qquad (43)$$

$$v_a = M\beta V_{in}/\sqrt{3} \qquad (44)$$

For the desired values of $I_{C1max} = 10\,A$, $I_{C2max} = 12\,A$ and $\Delta(V_{C_1} + V_{C_1'}) = \Delta(V_{C_2} + V_{C_2'}) = 18\,V$, by considering (41) and (42), the capacitances of $C_1 = C_1' = 100\,\mu F$ and $C_2 = C_2' = 120\,\mu F$ are identified. Also, each switch current value during the shoot-through state is identified by:

$$I_{sh} = I_L = P_{out}/V_{in} \qquad (45)$$

Here, v_a and i_a indicate the ac phase values, as depicted in Fig. 4 (a). M and β denote modulation index and boost factor, respectively. During the non-shoot-through state, each switch average current value can be calculated as follows:

$$I_{nst.} = \sqrt{2} I_{ac}/\pi = 4P_{out}/(3\pi V_{in} M\beta\cos\varphi) \qquad (46)$$

Therefore, each power switch average current value is identified, easily.

$$I_{SW} = D I_{sh} + (1-D) I_{nst} = \frac{2P_{out}}{3V_{in}}\left(D + \frac{2(1-D)}{\pi M\beta\cos\varphi}\right) \qquad (47)$$

For the prototype inverter, $\beta = 1.35$, $\cos\varphi = 0.8$ and $180\,V \le V_{in} \le 300\,V$. Therefore, from (46) and (47) each switch nominal current value is equal to 2.5A. Also, the dc-link maximum voltage value which is also applied to each switch is given by:

$$V_{SW} = \beta V_{in} = \left(\left(3\sqrt{3}G/\pi\right) - 1\right) V_{in} \qquad (48)$$

From (48), each switch stress voltage is equal to 338 V.

VI. Simulation and Experimental Results

To validate the proposed FSTPI topology and the introduced switching pattern, the vector control strategy is emulated in MATLAB/Simulink. The q-ZSI inverter is feeding a Wye-connected RL load, as shown in Fig. 4 (a). Some key parameters of the prototype inverter are given in Table IV and a picture of 1 kW prototype inverters is shown in Fig. 11. Here, it is assumed that the dc-link voltage is equally divided between the two split capacitors, i.e., C_1 and C_1'. When the maximum boost control method is used, switching times are given according to (10) - (17). By applying these vectors, when the shoot-through duty ratio is equal to 0.18, the currents and voltages of the three phases load are illustrated in Fig. 12 (a) and (b). Firstly, voltage oscillations across the C_1 and C_1' capacitors are neglected and the PWM signals are applied without any feedback loop from these capacitors voltages. Therefore, three-phase voltages and currents through the load are not identical to each other, can be seen in Fig. 12. This fact causes output voltages to be unbalanced and third phase that is connected to the capacitor's midpoint, isn't similar to others.

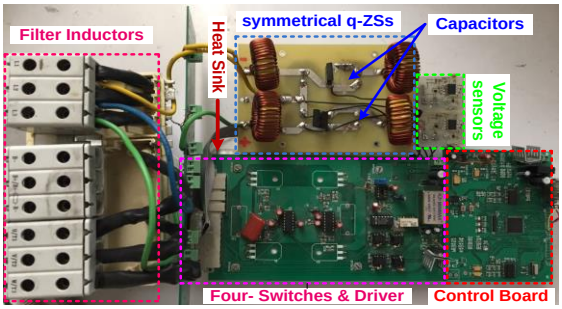


Fig. 11. A photograph of the 1 kW prototype proposed FSTPI.

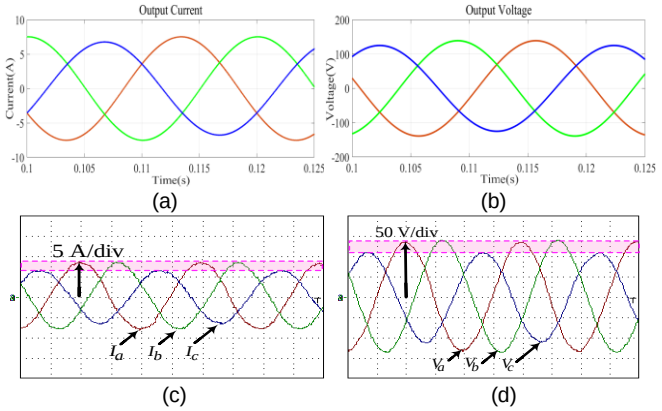


Fig. 12. Simulation and experimental results for the proposed FSTPI inverter by using the conventional PWM and maximum boost control approaches for D = 0.18, time=5 ms/Div. (a) simulation three-phase currents, (b) simulation three-phase voltages, (c) experimental three-phase currents(d) experimental three-phase voltages.

The expimenal results with the same operation condition are shown in Fig. 12 (c) and (d), which are in good agreement with the given simulation results. It can be clearly seen from the given results that three-phase output voltages aren't symetrical, when insantaneous voltages of C_1 and C_1' aren't considered to generate the PWM signals for the inverter.

Fig. 13 (a) shows the voltage fluctuations through the two dc-link capacitors (i.e., C_1 and C_1'). The low frequency ripple on the dc-link voltage depends on the capacitors sizes and output power and affects the FSTPI performance. Voltage ripples on the capacitors and V_a are depicted together in Fig. 13 (b).

As previously mentioned in Sec. IV, the improved SVM modulation approach, analyzed by (20) - (30) and (31) - (34), can be used to compensate effects of the unbalanced dc-link voltages on the inverter performance. Voltages of C_1 and C_1' capacitors are measured for considering the instantaneous differences during switching time generation. Consequently, using this method, output currents and voltages are well-balanced, as depicted in Fig. 14 (a) and (b), respectively. Experimental results for verifying the given procedure are depicted in Fig. 14 (c) and (d) in the step-up mode for D=0.07. As shown clearly, the three phase's currents as well as the voltages are well-balanced, here. Converter behavior for load with power factor of 0.9 and shoot through duty ratio equal to 0.2 is shown in Fig. 15. Voltage and current are increased due to the increased maximum value of V_{pn}. The simulation results, as given in Fig. 15 (a) and (b), confirm the experimental results, shown in Fig. 15 (c) and (d). The load voltage harmonic spectrum for the conventional PWM method, applied to the proposed inverter, is also shown in Fig. 16 (a).

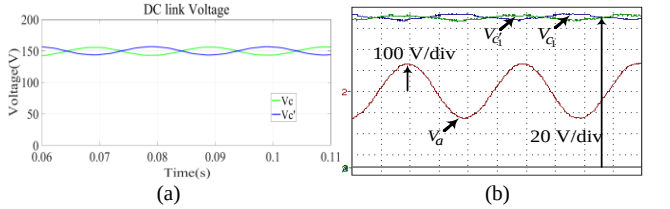


Fig. 13. Dc-link capacitors voltages (C_1 and C_1') when D = 0.18: (a) simulation results and (b) experimental results by including the 3rd phase output voltage (time: 5 ms/Div.)

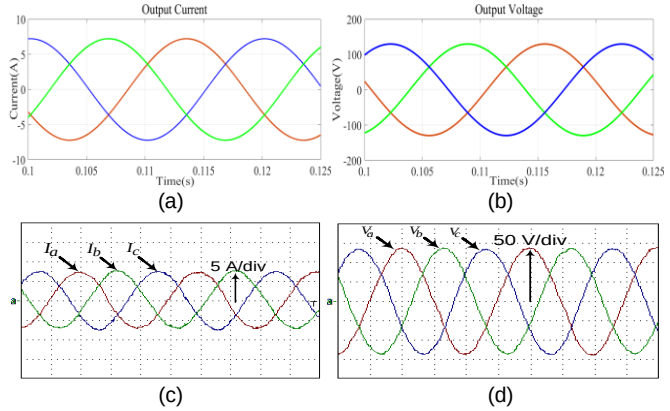


Fig. 14. Different waveforms of the proposed FSTPI inverter by using the given PWM procedure, when D=0.18: (a) simulation output currents, (b) simulation output voltages, (c) experimental output currents, and (d) experimental output voltages.

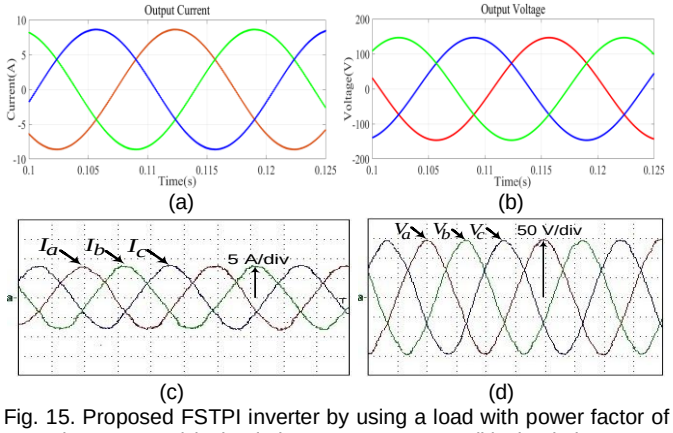


Fig. 15. Proposed FSTPI inverter by using a load with power factor of 0.9, when D=0.2: (a) simulation output currents, (b) simulation output voltages, (c) experimental output currents, and (d) experimental output voltages.

Using this technique provides the current THD value equal to 5.4% and it may cause some problems for peripheral systems, in practice. Fig. 16 (b), shows the harmonic spectrum for the compensated PWM. The output current distortion is less than 5%, as given in Fig. 16 (b). This approach is therefore able to perform according to ANSI C84.1-2020 standards in power quality for electrical consumer. The output current distortion is

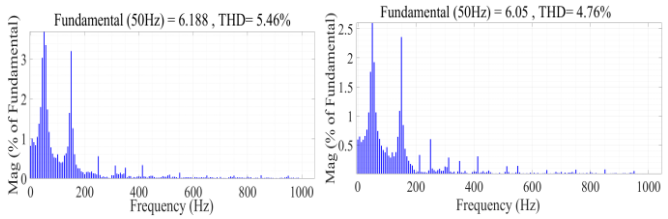


Fig. 16. Output current THD in the proposed inverter with maximum boost control method, (a) conventional PWM signals and (b) compensated proposed PWM approach.

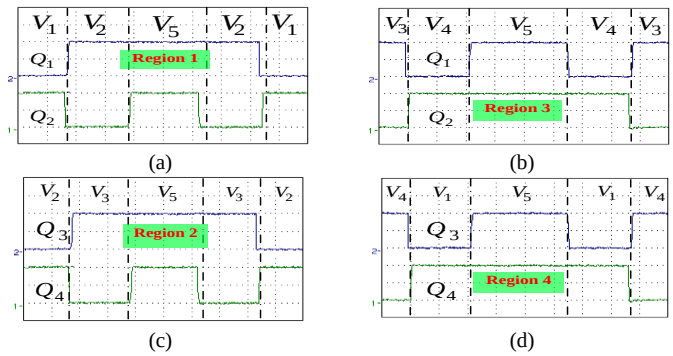
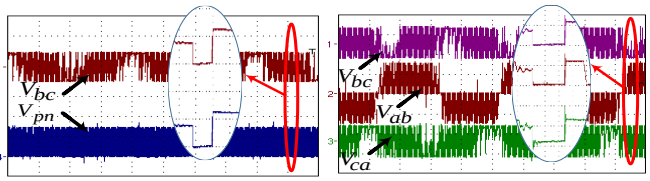


Fig. 17. Implemented switching patterns for the proposed FSTPI inverter in different sectors (5 V/Div. and 5 µs/Div.): (a) Region 1, (b) Region 2, (c) Region 3, and (d) Region 4.



(a) (b)

Fig. 18. Providing the null vector in the q-ZSI inverter through the shoot-though state (200 V/Div. and 5 ms/Div.) (a) line to line output voltage with V_{pn} and b) three-phase line to line voltage before the output filter.

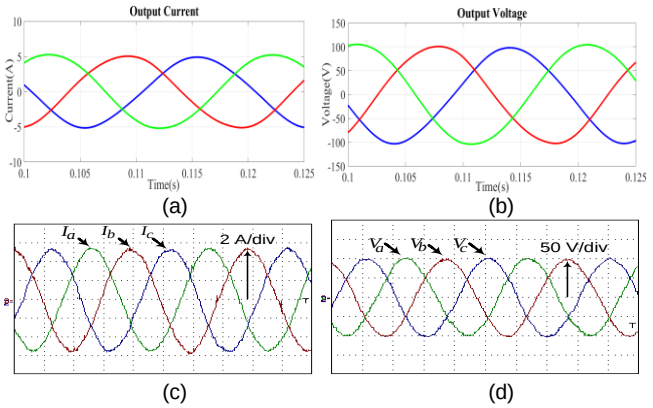
less than 5%, as given in Fig. 16 (b). Quality of the current satisfies IEC61000-2-2 requirements for all electronic equipment that are affected by the electromagnetic noise.

Comparing Figs. 8 and 17, clearly shows that the experimental and theoretical switching gate signals are in good agreement. In Fig. 17 (a) and (c), the experimental null vector in region 1 and 2 is placed at the center of the switching period. Also, the experimental switching pattern for the region 3 and 4, plotted in Fig. 17 (b) and (d), clearly shows that vectors 1, 3, 4, and 5 have been applied successfully to fulfill the reference voltage.

As mentioned before, the proposed four-switch converter is capable of providing a null vector through the shoot through state in which V_{pn}=0 (Fig. 3 (b)). For validating this subject, experimental results are given in Fig. 18. It is clear that during the shoot-through state, both V_{pn} and V_{ab} reach to zero, simultaneously, as shown in Fig. 18 (a). Also, three phases' output voltages, given in Fig. 18 (b), are zero during T_5. Consequently, V_5 behaves like a null vector in conventional six-switches inverter. To compare the performance of both simple boost control and the maximum boost control approaches, experimental and simulation results are shown in Fig. 19. Here, all of the experimental conditions are unchanged for these both cases and the main parameters are given in Table IV. Voltage gain for the proposed q-ZSI FSTPI is given in (7), when the simple boost PWM method is used. Output voltage and current waveforms for a load with power factor of 0.9 and shoot through duty ratio of 0.1 are shown in Fig. 19 (a) and (b). Obtained output voltage in the simple boost case is significantly less than the maximum boost procedure as clearly depicted in Fig. 19 (b). This is because the acquired gain in the simple boost method is less as given in (7). The given closed-loop control approach for the given transfer functions, (37) and (39), is also simulated for the proposed q-ZSI inverter. The inverter performance against disturbances of the input dc voltage and ac load variations are described here, in detail The simulation result for the load step change from R_L=20 Ω to 10 Ω is shown in Fig. 20 (a). It can be seen clearly that when the ac load changes, the dc-link voltage remained constant by adjusting the shoot-through properly, as depicted in Fig. 20 (b). Shoot-through duty cycle value is increased first for compensating the load changes at t=0.4 s. Experimental currents waveforms for a three-phase load are shown in Fig. 20 (c), when R_L decreases from 20Ω to 10Ω. Input voltage changes from 270 V to 300 V during 0.6 s<t<0.75 s time subinterval and the shoo-through value decreases after applying this input voltage disturbance and V_{pn} remains constant without changes, as given in Fig. 20 (d). The shoot-through value variations for compensating the applied input voltage disturbance is also shown in Fig. 20 (b). It can be seen that the dc-link voltage of the q-ZSI is remaining

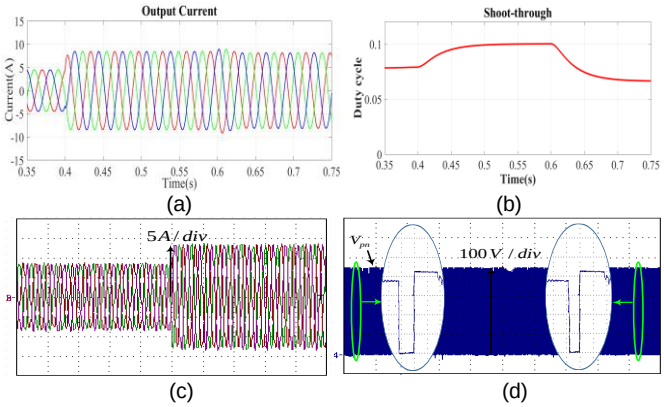
TABLE IV
SOME KEY PARAMETERS OF THE PROTOTYPE INVERTER

Parameter	Value
Load	$1kW, cos\varphi = 0.8$
Switching frequency	$10\ kHz$
DC input voltage	$180V - 300\ V$
C_1, C_1'	$120\ \mu F$
C_2, C_2'	$100\ \mu F$
L_1, L_1', L_2, and L_2'	$500\ \mu H$
Output filter inductor	$1\ mH$
Output filter capacitor	$47\ \mu F$
Power switch (IGBT)	IKQ40N120CH3XKSA1
Power diode	RHRG75120



(a) (b) (c) (d)

Fig. 19. Proposed FSTPI with simple boost procedure and using a load with power factor of 0.9, when D=0.1: (a) simulation output currents, (b) simulation output voltages, (c) experimental output currents, and (d) experimental output voltages.



(a) (b) (c) (d)

Fig. 20. Proposed q-ZSI performance against the input voltage and load disturbances: (a) simulation results for currents under the load disturbance, (b) shoot-through duty cycle, (c) simulation results for currents under the load disturbance, and (d) input voltage disturbance.

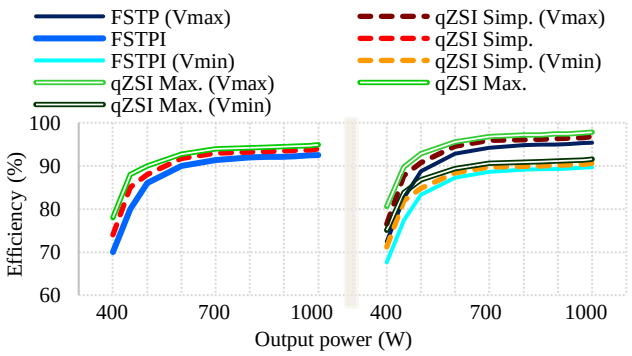


Fig. 21. Different efficiency curves versus output power for minimum, nominal, and maximum input voltage values. For conventional FSTPI, proposed qZSI with simple boost and maximum boost procedures. (V_{max}=300V, V_{min}=180V and V_{rated}=240V).

constant, which demonstrates a reliable performance against the different external disturbances, due to the applied closed-loop control.

Finally, in the simple boost PWM method, the switching events and the current circulation through the opposite vectors are relatively greater than the maximum boost control approach one. Consequently, the switching losses in the maximum boost method are relatively reduced. The proposed inverter efficiency curves have been plotted versus the output power under different conditions, as shown in Fig. 21.

For efficiency analysis of the given converter a power quality analyzer from Chauvin Arnoux company with the manufacturer part number of C.A 8335 is used. Here, the proposed inverter experimental efficiency curves for two different control methods are compared with the conventional FSTPI shown in Fig. 1 which does not apply the null vector. Fig. 21 clearly shows that the inverter efficiency is improved by approximately 4% and 2% for lower and higher power values, respectively. This improvement is mainly due to the null vector applied during the remaining time of each switching period. The proposed inverter efficiency using the maximum boost method is increased by 1.2% compared to the simple boost control method. As the input voltage decreases, the efficiency of the proposed FSTPI is also decreased. However, the efficiency for the proposed topology with maximum boost control method is relatively higher in all input voltage ranges.

VII. Conclusion

A four-switch q-ZS inverter with capability of creating a null vector is introduced, analyzed, simulated, and implemented in the laboratory. The null vector in the SVPWM is applied as a useless vector in the entire excess time of each switching period, and contrary to conventional SVM methods in FSTPIs, two active vectors are not applied in opposite directions. In the maximum boost control procedure, shoot-through state is applied for all of the excess time and there is no need to use the opposite vectors. All active vectors in the space vector diagram result in the flow of current from the input to the output or vice versa Consequently, power losses in the power semiconductors are increased when active vectors are used instead of null vectors. Applying the null vector during the shoot-through state reduces the inverter losses and improves its efficiency, significantly. Moreover, the number of switching events for applying the opposite vectors in each switching cycle is reduced which reduces the switching losses as well. Instantaneous voltage fluctuation on the two split capacitors in the dc-link unbalances the three-phase output voltages. This issue can be overcome by using a closed-loop control approach, easily. A 1 kW prototype inverter has been implemented and experimental results confirm the theoretical analyses and the proposed inverter operation. Inverter efficiency has increased by 4% at lower power and 2% at nominal power values, respectively. Moreover, its output current THD is improved by applying the given control approach and it is less than 5%, due to the applied null vector during the remaining time of each switching period.

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