# HotReRAM: A Performance-Power-Thermal Simulation Framework for ReRAM based Caches

Shounak Chakraborty[§], *Senior Member, IEEE*, Thanasin Bunnam[§], *Member, IEEE*, Jedsada Arunruerk, Sukarn Agarwal, *Member, IEEE*, Shengqi Yu, *Member, IEEE*, Rishad Shafik, *Senior Member, IEEE*, Magnus Själander, *Senior Member, IEEE*

***Abstract*—This paper proposes a comprehensive thermal modeling and simulation framework, *HotReRAM*, for resistive RAM (ReRAM)-based caches that is verified against a memristor circuit-level model. The simulation is driven by power traces based on cache accesses for detailed temperature modeling over time. *HotReRAM* models power at a fine-grain level and generates temperature traces for different cache regions together with detailed analyses of thermal stability, retention time and write latency. Combining *HotReRAM* with *gem5*, a full-system simulator, and *NVSim*, a power simulator, for ReRAM enables temporal and spatial modeling of crucial ReRAM characteristics. This integration allows designers and architects to analyze various cache characteristics within a single cache bank and address thermal-induced issues when designing ReRAM caches. Our simulation results for an 8MiB ReRAM cache show that the spatial thermal variance can be as high as 7K for a single cache bank, whereas the temporal thermal variance is more than 40K. Such temperature variances impact retention time with a standard deviation of $3.9$ to $10.2$ for a set of benchmark applications, where the write latency can increase by up to $14.5\%$.**

***Index Terms*—ReRAM, Memristor, Retention Time, Write Latency/Energy, Thermal Stability, Simulation, VTEAM**

## I. Introduction

HIGH leakage power and low density in conventional SRAM have driven exploration of alternative cache memory technologies, particularly non-volatile memories (NVMs) like ReRAM [1], [2]. ReRAM offers several advantages including low leakage power, high endurance, long retention, comparable access times, and CMOS compatibility [3]. However, its higher write energy compared to SRAM [4] can increase circuit temperature, potentially causing performance degradation and device failure. This necessitates careful consideration of temperature-induced characteristics in ReRAM cache designs, especially under memory-intensive workloads.

S. Chakraborty is with the Department of Computer Science, Durham University, DH1 3LE, UK. E-mail: shounak.chakraborty@durham.ac.uk

T. Bunnam and J. Arunruerk are with the Department of Computer Engineering, Rajamangala University of Technology Thanyaburi, Thailand. E-mail: thanasin.b@en.rmutt.ac.th and jedsada.a@en.rmutt.ac.th.

S. Agarwal is with Department of Electrical Engineering and Computer Science, Indian Institute of Science Education and Research Bhopal, India. E-mail: sukarn@iiserb.ac.in.

S. Yu is with Engineering School, Chongqing University of Posts and Telecommunications, 400065, China, and R. Shafik is with Newcastle University, NE4 7RU, UK. E-mail: yusq@cqupt.edu.cn and rishad.shafik@ncl.ac.uk.

M. Själander is with the Department of Computer Science, Norwegian University of Science and Technology, Trondheim, Norway 7491. E-mail: magnus.sjalander@ntnu.no.

Manuscript received April 00, 2023; revised August 00, 2023.

[§]Equal contribution

Prior arts have shown the detrimental effects of elevated temperatures on ReRAM devices [5], [6]. Higher temperature increases ReRAM cell conductance, impacting circuit functionality and data storage integrity. Additionally, increased write latency at higher temperatures further affects write operations [6]. While researchers have explored mitigating high temperatures in ReRAM caches, *a comprehensive simulation framework considering performance, power, and temperature holistically remains lacking.* To address this gap, we introduce *HotReRAM*, *a comprehensive thermal model for ReRAM caches* built on the HotSpot simulator [7], that simulates temperature using power traces, providing detailed insights into temperature-induced behaviors for in-depth ReRAM cache analysis. *HotReRAM* incorporates the Arrhenius Equation [8] to model the temperature dependence of ReRAM device parameters, enabling accurate simulation of thermal effects on performance metrics such as retention time and write latency.

*HotReRAM offers a comprehensive framework for analyzing the thermal behavior of ReRAM-based caches.* This work introduces a novel approach to thermal analysis of the ReRAM cache by combining two key features. First, *HotReRAM provides unprecedented granularity by simulating temperature variations at the subarray level.* Second, *it accurately models the temperature dependence of critical ReRAM parameters, such as retention time and write latency, using the Arrhenius Equation.* This combination enables a more comprehensive and precise evaluation of thermal effects on ReRAM cache performance. By integrating with HotSpot [7], gem5 [9], and NVSim [4], *HotReRAM provides a detailed thermal profile of the cache, including temperature variations at the subarray level.* This fine-grained analysis allows for the identification of potential hotspots and enables designers to optimize cache performance and reliability. *HotReRAM accurately models the impact of temperature on critical cache characteristics such as retention time and write latency, as validated against circuit-level simulations using the thermal-integrated VTEAM model* [3]. This reveals significant spatial and temporal thermal variations that can impact performance by up to 14.5%. *HotReRAM*[1] is *the first open-source thermal simulator for NVMs, providing comprehensive temperature-induced behaviors.*

## II. HotReRAM: Proposed Simulation Model

This section details the ReRAM cache model in *HotReRAM*, capturing temperature dependent ReRAM characteristics. Fig-

[1]available at https://github.com/shounakdurham/HotReRAM.git

ure 1 illustrates the architecture of a ReRAM-based cache, consisting of an input multiplexer (for selecting the appropriate input voltage), a 4 KiB ReRAM crossbar (512-bit data) with 6-bit address word lines, a comparator bank and an output multiplexer (for selecting the output data). The 'RW' signal controls read or write operations. For a read operation, 'RW' is set to 1. This applies 'Vread' to the bitline input ('BLi'), causing current to pass through the selected 1T1R cells. The resulting output current ('BLo') generates a voltage at 'Rs', which is then decoded by comparators [10], that compare the sensed voltage to a reference voltage, producing binary values for tag comparison and data output. For a write operation, 'RW' is set to 0, and 'Vwrite' or '-Vwrite' is applied to 'BLi' based on the input data, switching the memristor to low or high conductance states, respectively.

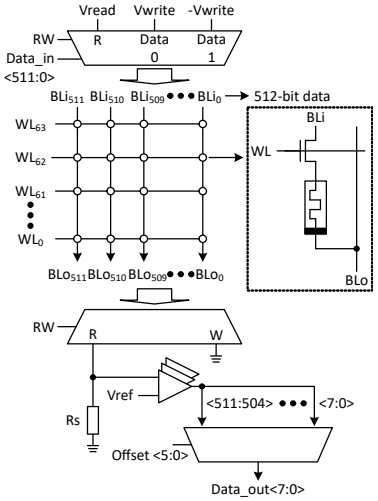


Fig. 1. ReRAM based Cache Design: Representation of a sub-array of LLC. Note that the 20-bit tag was implemented using the same architecture.

Our ReRAM-based LLC is physically distributed but logically shared among cores. Each bank is partitioned into sub-banks, mats, and subarrays, with each subarray containing a cell array and peripheral circuitry (row decoder, word line driver, etc.). Figure 2 illustrates this structure for a 1 MiB 16-way set associative LLC. *HotReRAM* models power and temperature at the subarray level (4 KiB), providing higher accuracy for analyzing temperature-dependent ReRAM properties. *This granularity enables precise modeling of power and thermal profiles across different cache locations, capturing the uneven distribution of cache accesses.* By employing NVSim [4], periodic power traces are generated at this granularity, to be used by *HotReRAM* to generate temperature traces.

Component temperature depends on its power consumption, heat transfer with adjacent components, and ambient heat abduction [12]. Joule heating establishes the relationship between power consumption and temperature: $T = T_0 + P \cdot R_{th}$, where $T$ is the current temperature, $T_0$ is the initial temperature, $P$ is power consumption, and $R_{th}$ is thermal resistance [13]. Due to the higher vertical thermal resistance of ReRAM devices, we primarily consider $R_{th}$ as the vertical thermal resistance.

Temperature fluctuations influence ReRAM device behavior, affecting memristance, data integrity, and performance. *HotReRAM* addresses the lack of comprehensive thermal modeling in existing memristor models [14], [14]–[16] by providing an

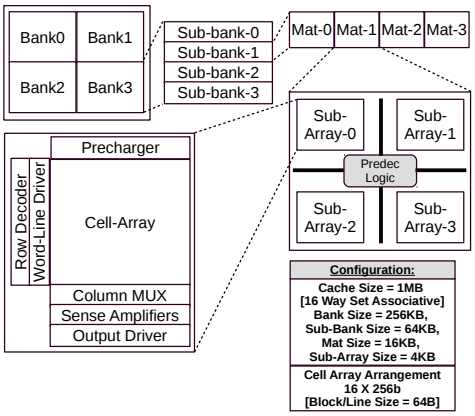


Fig. 2. LLC layout used in *HotReRAM* [11], where circuit design of each sub-array is illustrated in Figure 1.

architectural-level thermal simulation framework to analyze performance, power, and temperature in ReRAM-based architectures. Thermal stability ($\Delta$) of ReRAM is represented as: $\Delta = \frac{E_a}{k_B \cdot T}$, where $E_a$ is activation energy, $k_B$ is the Boltzmann constant, and $T$ is temperature in Kelvin. Higher temperatures reduce thermal stability, impacting conductivity ($\sigma$) and retention time ($\tau$): $\sigma = \sigma_0 \cdot exp(-\Delta)$ and $\tau = \tau_0 \cdot exp(\Delta)$, where $\sigma_0$ and $\tau_0$ are initial conductivity and retention time, respectively, and the write latency ($t_w$) is derived using a prior model [6].

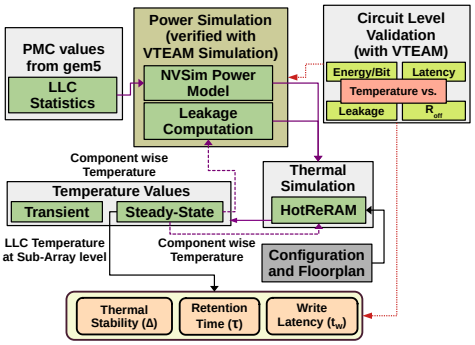


Fig. 3. *HotReRAM* with Thermal-integrated VTEAM, gem5 and NVSim.

## III. Simulating Power-Performance-Temperature

Now, we describe how *HotReRAM* simulates the power-performance-temperature characteristics of ReRAM-based caches. The simulation flow involves collecting performance traces from gem5 [9], generating power traces using NVSim [4], and feeding these traces to *HotReRAM* to simulate temperature and ReRAM's thermal behaviors.

### A. Generating Performance-Power Traces

Performance traces are generated by executing PARSEC benchmark applications [17] in gem5 (full system mode) [9]. These traces include LLC performance monitoring counters (access counts, hits, misses, etc.) at the subarray level. The collected stats are then used as input to NVSim to simulate the power consumption of each subarray in the ReRAM-based LLC. To balance accuracy and computational complexity, the subarray size (4 KiB) is configurable based on the overall LLC size. The power traces from NVSim are then fed to *HotReRAM* to generate temperature traces, including both transient and steady-state values. Floorplan details are obtained using NVSim and HotFloorPlan (from HotSpot) [7] to ensure accurate thermal modeling.

### B. HotReRAM: Proposed Thermal Model

*HotReRAM* incorporates the LLC floorplan and technology-specific thermal parameters (capacitance and resistance for memristor and CMOS devices). It utilizes the default cooling system configuration from HotSpot 6.0. Figure 3 illustrates the integration of *HotReRAM* with NVSim and gem5. To validate the thermal model, we also modeled the LLC circuitry in the thermal-integrated VTEAM (TiVTEAM) framework, that is used to validate the accuracy of the ReRAM device model and its thermal behavior at the circuit level, ensuring the basic components of HotReRAM are sound. Performance monitoring counter (PMC) values from gem5 (read count, write count, miss count, and allocations) are used to calculate the total energy consumption at the periodic interval of $0.33\mu$S, capable of capturing essential thermal dynamics while managing complexity [12]. Note that, the dynamic energy usage for different individual operations are derived from NVSim. Since ReRAM caches have different read and write energy characteristics compared to SRAM, we calculate read and write dynamic energy separately, including energy consumed for tag operations and LLC misses. These energy values are used to derive total dynamic energy consumption:

$$Dyn\_En_{Rd}^{Total} = (Dyn\_En_{Rd}^{Tag} + Dyn\_En_{Rd}^{Data}) \times \#LLC\_Rd \quad (1)$$

$$Dyn\_En_{Wr}^{Total} = (Dyn\_En_{Rd}^{Tag} + Dyn\_En_{Wr}^{Data}) \times \#LLC\_Wr \quad (2)$$

$$Dyn\_En_{Miss}^{Total} = Dyn\_En^{LLC\_Miss} \times \#LLC\_Miss \quad (3)$$

$$Dyn\_En_{Allc}^{Total} = (Dyn\_En_{Wr}^{Tag} + Dyn\_En_{Wr}^{Data}) \times \#LLC\_Allc \quad (4)$$

$$\begin{aligned} Dyn\_En^{Total} = {} & Dyn\_En_{Rd}^{Total} + Dyn\_En_{Wr}^{Total} \\ & + Dyn\_En_{Miss}^{Total} + Dyn\_En_{Allc}^{Total} \end{aligned} \quad (5)$$

These dynamic energy values are calculated at the subarray level and converted to dynamic power consumption. A leakage computation framework is then employed, utilizing subarray level leakage data from NVSim. To address limitations in NVSim's leakage model (limited temperature range and granularity), we use piece-wise linear approximation [12] to estimate leakage power for any temperature value. This approach provides a good balance between accuracy and computational cost. The derived leakage and dynamic power values for each subarray are then fed to *HotReRAM*, along with the LLC floorplan and previous temperature values, to generate transient and steady-state temperature values. The steady-state temperature is used to calculate thermal stability, retention time, and write latency by employing prior models [14], [15].

## IV. Simulation Results

This section presents the simulation results, including circuit-level validation and architectural analysis.

### A. Circuit Level Validation

We validated the functionality of *HotReRAM* (illustrated in Figure 1) using UMC 65nm technology with our TiVTEAM model [3]. The original VTEAM model, renowned for its ability to accurately estimate the characteristics of various memristor devices [14], was enhanced to include temperature-dependent behavior. This modification involved incorporating temperature responses extracted from real device experiments conducted on a fabricated self-directed channel (SDC) memristor [18]. By ensuring that both the temperature parameters and memristor characteristics [19] were derived from the same type of SDC device, our approach guarantees consistency, accuracy, and reliability in our simulations. Reading voltage ('Vread') was set to 200mV, while writing voltages ('Vwrite' and '-Vwrite') were set to 900mV and -300mV, respectively, to avoid unintended switching [20]. Figure 4 shows the simulation waveforms, demonstrating successful write and read operations. The simulation results of the temperature effects on performance are depicted in Figure 5, Figure 6, Figure 7, and Figure 8. Energy/bit slightly increases with temperature due to increased transistor current and leakage. Write latency for logic 1 increases non-linearly with temperature due to lower OFF memristance at higher temperatures. Leakage power increases with temperature, while OFF resistance decreases non-linearly.

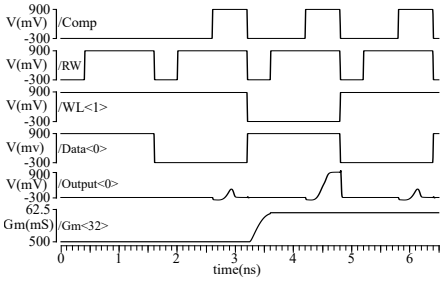


Fig. 4. Simulation waveform. At 3.2ns, $WL$ <1> signal selects word#1 (active low) for writing logic 1. Then, $-Vwrite$ will be connected to 1T1R cells causing conductance ($Gm$) switching from $LOW$ conductance to $HIGH$ conductance. The $Output$ signal confirms logic 1 is stored and read correctly.

### B. Simulation Setup

We used gem5 (full system mode) [9] to simulate a four-core x86 CMP with private L1 caches and a shared 8MiB ReRAM L2 cache (configuration detailed in Table II), where the entire cache is physically divided into 8 slices of 1MiB each that resembles the configuration shown in Figure 2. Energy parameters were obtained from NVSim [4] (Table I). We compared the ReRAM cache with iso-capacity/iso-area SRAM caches. Thermal modeling parameters are listed in Table III. To evaluate performance, power, and thermal behavior, we integrated NVSim [4], and *HotReRAM* with gem5. Performance traces from gem5 fed into NVSim generated power traces ($0.33\mu$s interval, assuming stable CMP temperature [12]). Our leakage model (Section III-B) addressed limitations in NVSim. The CMP floorplan (Figure 9) was generated using HotFloorPlan. We evaluated the framework using multi-threaded PARSEC benchmarks [17] with varying read/write intensities (Table IV).

### C. ReRAM-LLC Analysis

We analyzed the temporal and spatial thermal variations in the ReRAM LLC using *HotReRAM*. Figure 10 shows the variation in read, write, and writeback counts for a randomly selected mat (mat 25) during the execution of *Blackscholes*. Spikes in write operations cause an increase in power consumption and temperature, as shown in Figure 11. Due to the

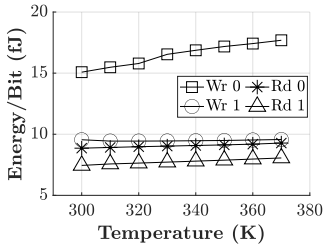


Fig. 5. Temperature vs. Energy/Bit

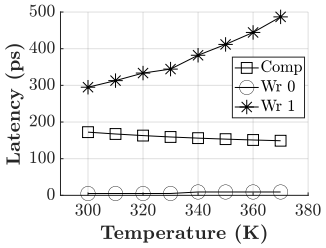


Fig. 6. Temperature vs. Latency

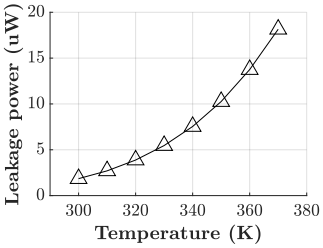


Fig. 7. Temperature vs. Leakage

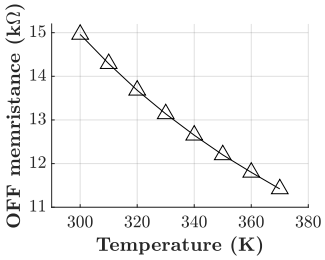


Fig. 8. Temperature vs. $R_{off}$

TABLE I
TIME, ENERGY, AND AREA VALUES FOR SRAM (ISO-AREA (A)/ISO-CAPACITY (C)) AND RERAM CACHES ($4/8MiB$, $64B$ BLOCK, 16-WAY)

| Memory Device | SRAM | | ReRAM |
|---|---|---|---|
| **Cache Size** | 256KiB | 8MiB | 8MiB |
| **Feature Size (C/A)** | 65nm-CMOS(A) | 65nm-CMOS(C) | 65nm |
| **Wr Energy (nJ) (per access/bit)** | 0.011 | 0.082 | 0.103 |
| **Rd Energy (nJ) (per access/bit)** | 0.011 | 0.082 | 0.031 |
| **Leakage Power (at 350K)** | 556 mW | 10,826 mW | 2,065 mW |
| **Rd Latency (ns)** | 0.33 | 0.67 | 0.98 |
| **Wr Latency (ns)** | 0.33 | 0.67 | 6.61 |
| **Area** | 19.07 $mm^2$ | 208.5 $mm^2$ | 17.98 $mm^2$ |

TABLE II
*HotReRAM*: SYSTEM CONFIGURATION

| System Component | Configuration |
|---|---|
| **CPU** | x86 quad-core, @2GHz |
| **L1 SRAM I/D-Cache** | 32KiB, 64B cache block, 4-way, LRU, MESI |
| **L2 ReRAM Cache** | 8MiB, 64B cache block, 16-way, Non MRU, MESI |
| **Main Memory** | 8GB DRAM |

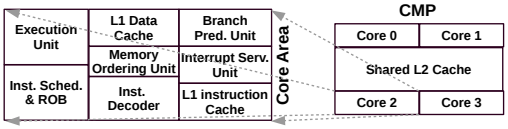


Fig. 9. Floorplan of the four core based CMP

thermal characteristics of ReRAM, the temperature remains elevated even after the write activity drops. But, sustained elevated temperature still keeps the power high due to increased leakage power through a positive feedback loop along with higher write energy. Figure 12 shows the temporal variation in thermal stability ($\Delta$) and write latency ($t_w$) for mat 25. Higher temperatures reduce $\Delta$, leading to increased $t_w$ and a drop in $\tau$. The maximum spatial thermal variance across all mats during *Blackscholes* execution ranged from 3-7K (Figure 13). Figure 14 shows the maximum temperature of the ReRAM LLC across all benchmarks, ranging from 355-359K. Iso-area SRAM has lower maximum temperatures (331-335K) due to its smaller capacity, while iso-capacity SRAM exhibited temperatures between 343-350K. ReRAM LLC showed a higher average spatial thermal variance compared to both SRAM configurations (Figure 15), which is in line with the expected behavior of ReRAM caches, where uneven access patterns lead to significant temperature variations. The standard deviation of retention time ($\tau$) for all benchmarks ranged from 3.9-10.2 (Figure 16), influenced by temperature variations, highlighting the importance of thermal management in ReRAM caches. The maximum percentage increase in write latency ($t_w$) ranged from 7.1-13.9% (Figure 17).

TABLE III
PARAMETERS FOR THERMAL MODELING IN *HotReRAM* [21]

| Layer | Thermal Conductance (W/mK) | Heat Capacitance (J/$m^3$K) | Depth ($\mu$m) |
|---|---|---|---|
| **Heat Sink** | 400.00 | $3.55 \times 10^6$ | 6,900 |
| **Heat spreader** | 400.00 | $3.55 \times 10^6$ | 1,000 |
| **TIM** | 4.0 | $4.00 \times 10^6$ | 20 |
| **Core/SRAM cache** | 100.0 | $1.75 \times 10^6$ | 150 |
| **ReRAM cache** | 5.0 | $1.92 \times 10^5$ | 200 |

TABLE IV
BENCHMARK APPLICATIONS (R: LARGE READ MPKI, W: LARGE WRITE MPKI AND M: COMPARABLE READ AND WRITE MPKI)

| Benchmark-Suites | Applications |
|---|---|
| **PARSEC [17]** | Blackscholes (M), Bodytrack (M), Canneal (W), Dedup (R), Fluidanimate (R), Freqmine (M), Streamcluster (M), Swaptions (R), X264 (W) |

## V. PRIOR WORK

Thermal simulators for MPSoC, such as HotSpot [7], ISAC [22], LUTSim [23] and 3D-ICE [24], have been developed to address thermal management challenges in CMPs. However, these simulators primarily focus on conventional CMOS-based designs and do not consider the thermal implications of emerging memory technologies like ReRAM. The performance and lifetime of ReRAM devices are significantly affected by temperature [5], [6]. These researches have also shown the impact of temperature on ReRAM functionality, highlighting the importance of maintaining thermal stability ($\Delta$) for consistent performance. Furthermore, the increasing size of on-chip LLCs exacerbates thermal challenges due to spatial and temporal variations in access patterns, leading to uneven power density and temperature distribution [12]. Existing thermal simulators lack the capability to capture these variations accurately. *HotReRAM* addresses these limitations by providing a comprehensive thermal model for ReRAM-based MPSoCs. It captures spatial and temporal thermal variations across large LLCs and analyzes key ReRAM properties (thermal stability, retention time, and write latency) at the sub-array level granularity [11]. *HotReRAM leverages NVSim for area and power analyses, HotFloorPlan for CMP floorplanning [7], and gem5 for performance simulation [9], creating a complete performance-power-thermal simulation framework for exploring NVM technologies.*

## VI. CONCLUSIONS

This paper introduced *HotReRAM*, a comprehensive thermal modeling and simulation framework for ReRAM-based caches. Validated against a circuit-level model, *HotReRAM* enables fine-grain power and temperature analyses, capturing

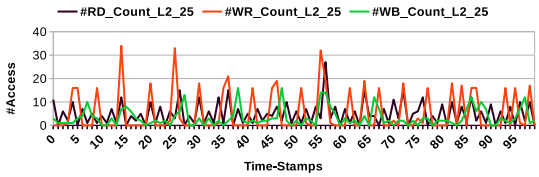


Fig. 10. Read, Write Allocate and Write Back counts for Mat 25 (Black)

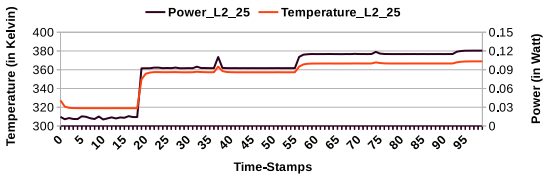


Fig. 11. Temporal Variation in Power and Temperature for Mat 25 (Black)

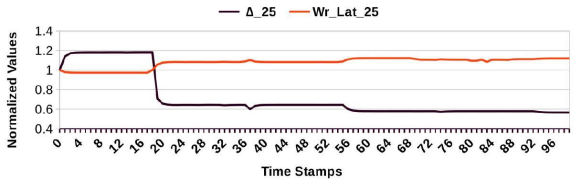


Fig. 12. Temporal Variation in Thermal Stability ($\Delta$) and Write Latency ($t_w$) for Mat 25 (Black)

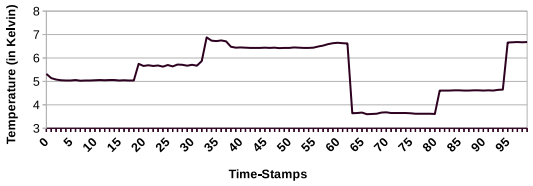


Fig. 13. Spatial Thermal Variance across all Mats (Black)

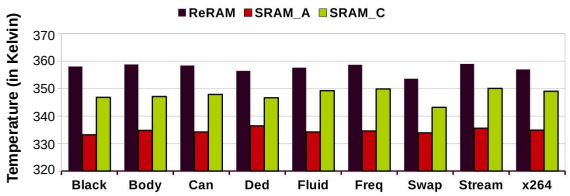


Fig. 14. Maximum Mat Temperature

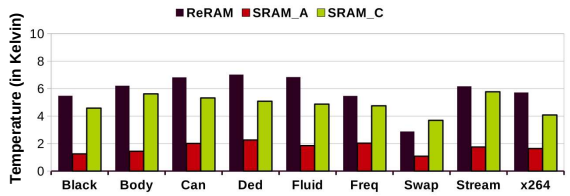


Fig. 15. Average Spatial Thermal Variance

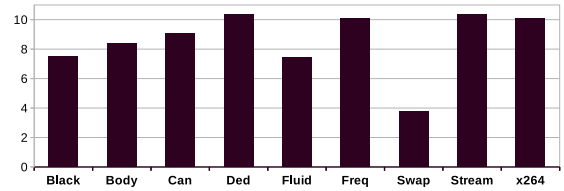


Fig. 16. Standard Deviation in Retention Time for ReRAM LLC

both spatial and temporal thermal variations. Integration with gem5 and NVSim allows for detailed modeling of key ReRAM characteristics, including thermal stability, retention time, and write latency. Our results demonstrate significant thermal variances within an 8MiB ReRAM cache, impacting retention

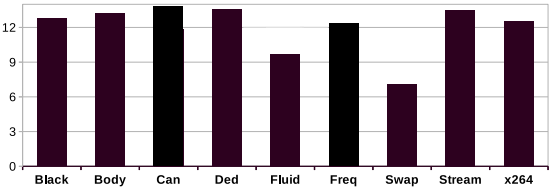


Fig. 17. Maximum percentage increase in Write Latency for ReRAM LLC

time and write latency. *HotReRAM* provides designers and architects with crucial insights to understand and address thermal challenges in ReRAM caches, optimizing performance and reliability. While *HotReRAM* offers a comprehensive analytical framework for ReRAM caches, our future work could involve validating HotReRAM against real hardware along with the impact of process variations.

## ACKNOWLEDGMENTS

This work is funded by *Marie Curie Individual Fellowship (MSCA-IF), EU (Grant Number 898296)*, and *OPS MHESI, TSRI and RMUTT, Thailand (Grant No. RGNS 65-092)*.

## REFERENCES

[1] R. Shafik *et al.*, "Real-Power Computing," *IEEE Trans. on Comp.*, 2018.
[2] H. Abunahla and B. Mohammad, "Memristor Device Overview," in *Memristor Technology: Synthesis and Modeling for Sensing and Security Applications*. Springer International Publishing, 2018.
[3] T. Bunnam, "Memristor-based design solutions for mitigating parametric variations in iot applications," Ph.D. dissertation, School of Engineering, Newcastle University (UK), 2021.
[4] X. Dong *et al.*, "NVSim: A Circuit-Level Performance, Energy, and Area Model for Emerging Nonvolatile Memory," *IEEE TCAD*, 2012.
[5] H. Shin *et al.*, "A thermal-aware optimization framework for ReRAM-based deep neural network acceleration," in *ICCAD*, 2020.
[6] M. V. Beigi and G. Memik, "THOR: THermal-aware Optimizations for extending ReRAM Lifetime," in *IPDPS*, 2018.
[7] R. Zhang *et al.*, "HotSpot 6.0: Validation, acceleration and extension." in *University of Virginia, Tech. Report CS-2015-04*, 2015.
[8] S. R. Logan, "The origin and status of the arrhenius equation," *Journal of Chemical Education*, 1982.
[9] N. Binkert *et al.*, "The gem5 simulator," *SIGARCH CAN*, 2011.
[10] S. Chevella *et al.*, "A low-power 1-v supply dynamic comparator," *IEEE Solid-State Circuits Letters*, vol. 3, 2020.
[11] S. Thoziyoor *et al.*, "CACTI 5.1," in *Tech. Report, HP Lab.*, 2008.
[12] S. Chakraborty and M. Själander, "WaFFLe: Gated Cache-Ways with Per-Core Fine-Grained DVFS for Reduced On-Chip Temperature and Leakage Consumption," *ACM TACO*, 2021.
[13] Y. Koo *et al.*, "Accelerated retention test method by controlling ion migration barrier of resistive random access memory," *IEEE EDL*, 2015.
[14] S. Kvatinsky *et al.*, "VTEAM: A General Model for Voltage-Controlled Memristors," *IEEE TCAS II: Express Briefs*, 2015.
[15] I. Messaris *et al.*, "A Data-Driven Verilog-A ReRAM Model," *IEEE TCAD*, 2018.
[16] R. Berdan *et al.*, "A memristor SPICE model accounting for volatile characteristics of practical reram," *IEEE EDL*, 2013.
[17] C. Bienia *et al.*, "The PARSEC benchmark suite: Characterization and architectural implications," in *PACT*, 2008.
[18] T. Bunnam *et al.*, "Empirical temperature model of self-directed channel memristor," in *IEEE SENSORS*, 2020.
[19] B. Garda and Z. Galias, "Modeling sinusoidally driven self-directed channel memristors," in *ICSES*, 2018.
[20] T. Bunnam *et al.*, "Pulse controlled memristor-based delay element," in *PATMOS*, 2017.
[21] M. V. Beigi and G. Memik, "TAPAS: Temperature-aware Adaptive Placement for 3D Stacked Hybrid Caches," in *MEMSYS*, 2016.
[22] Y. Yang *et al.*, "Adaptive multi-domain thermal modeling and analysis for integrated circuit synthesis and design," in *ICCAD*, 2006.
[23] C. Pan *et al.*, "I-LUTSim: An iterative look-up table based thermal simulator for 3-D ICs," in *DAC*, 2013.
[24] A. Sridhar *et al.*, "3D-ICE: Fast compact transient thermal modeling for 3D ICs with inter-tier liquid cooling," in *ICCAD*, 2010.