# DUAL POLARITY MULTI-LEVEL BOOST DC-DC CONVERTER

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**Keywords:** HIGH-GAIN, BIPOLAR, DC-DC, HIGH-FREQUENCY, NON-ISOLATED

## Abstract

With the shift in focus to DC collection networks, for renewable applications, comes the opportunity to explore the potential of DC links for bipolar DC collection networks. These networks provide greater transmission efficiency compared to their AC counterpart and do not require frequency or phase matching techniques. While DC links for unipolar networks have been realised within the literature, there has been limited focus on DC links that are compatible with bipolar networks. With their inherent cable redundancy, bipolar collection networks are an attractive option for renewable applications where cables are difficult to access. A demonstration unit of a scalable bipolar DC-DC converter is presented and experimentally validated. The unit utilised the combination of 2N-1 and inverting 2N Cockcroft Walton topologies in tandem, as this design facilitates a simultaneous positive and negative output, that operates with a single switch. The similar designs of the 2N-1 and 2N topologies enable balanced voltage output, minimising the need for voltage-balancing techniques. The efficiency of the demonstration unit was shown to be 98 % during steady-state operation.

## 1 Introduction

Innovations in the renewable energy sectors have led to a surge of DC-DC converter topologies to accommodate new generator designs while minimising power losses [1]. To minimise transmission losses, high-gain, low-loss power converters have been a key component for the integration of renewable energy systems [2–4].

Due to their increased efficiency and safety, DC collection networks are becoming an appealing alternative to AC networks [5]. This has resulted in the need for high-performance DC link technologies. With the need for transmission at MVDC and HVDC, high-gain power converters are required. Current designs rely on transformers with large voltage step-up ratios. In addition to the commonly discussed leakage inductance causing voltage spikes, the mechanical stress of the transformer related to the physical size and mass introduces additional design constraints. For novel generation technologies such as wave energy converters, the additional mechanical stress may impede technological development. With this, transformerless high-gain DC-DC converters offer an alternative power-dense solution.

One of the largest unexpected costs for offshore wind farms arises from cable failure resulting in downtime and revenue losses. [6, 7]. Bipolar DC collection networks provide line redundancy by using positive, negative, and neutral lines. This redundancy could mitigate the downtime currently caused by cable failures. As a result, DC links capable of facilitating bipolar networks can feed into a solution that promotes high availability power generation within offshore wind farms.

A bipolar high-gain DC-DC converter could operate as a DC link in a bipolar collection network, minimising the constraints imposed by current transformer-based power converter designs. Multiple technologies that explore the facilitation of transformerless bipolar LVDC networks have been previously presented in the literature [8–11]. However, most bipolar MVDC network facilitation research focuses on the utilisation of transformers for voltage gain [12–15]. Hence, there is the opportunity to explore a DC-DC converter capable of stepping up low-voltage generation sources, such as those utilised in renewable generation, into bipolar MVDC networks without utilising transformer.

The Cockcroft Walton voltage multiplier is a scalable, transformerless topology capable of producing significant voltage gains. Both individually inverting and non-inverting designs have been realised [16, 17]. However, the ability to utilise both designs simultaneously in a single switch topology has not been fully explored. A converter that incorporates both designs would be able to produce a bipolar output with a scalable gain while using simple control techniques. Such a design could integrate rectified low-voltage renewable sources into a bipolar MVDC collection network. This paper presents a bipolar DC-DC boost converter, that utilises Cockcroft Walton multipliers to achieve scalable voltage gain with simultaneous positive and negative voltage output.

The paper is organized as follows: Section II explores the design of the proposed bipolar converter Section III experimentally validates a demonstrator version of the proposed converter and Section IV provides concluding statements.

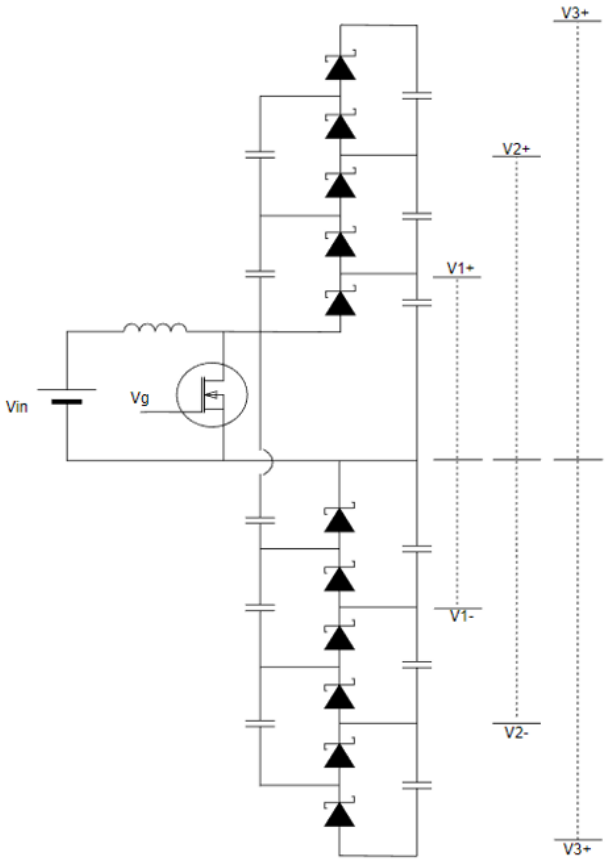


Fig. 1 Combined 2N-1 and inverting 2N topologies, circuit diagram for bipolar boost applications

## 2 Proposed Converter

3-level, 2N-1 and inverting 2N topologies were utilised to achieve a high-gain bipolar output, while only requiring a single active switch.

Figure 1 presents the proposed design utilising 11 capacitors and diodes in addition to a single inductor and switch, which produce a single input, multiple output design with a common ground.

### *2.1 Modes of Operation*

During operation, the topologies operate in 2 states; Mode 1 where the switch is conducting, and Mode 2 where the switch is blocking. Before reaching steady state, the capacitor ladder is fully charged by switching between Modes 1 and 2. During both Modes, the lowest level uncharged capacitor is charged through the input voltage, inductor and previously charged capacitors. Once fully charged, the capacitor's corresponding diode begins blocking. The next capacitor in the ladder will begin charging during the next switch cycle.

*2.1.1 Positive 2N-1:* During Mode 2 operation, the lowest level uncharged output (odd-numbered) capacitor is charged by the input voltage, inductor voltage, and charged oscillating (even-numbered) capacitors via the corresponding odd-numbered diode. During Mode 1 operation, the lowest level uncharged oscillating capacitor is charged by the charged output capacitors via the corresponding even-numbered diode. Figure 2 shows the equivalent circuits used for analysis during 2N-1 operation.

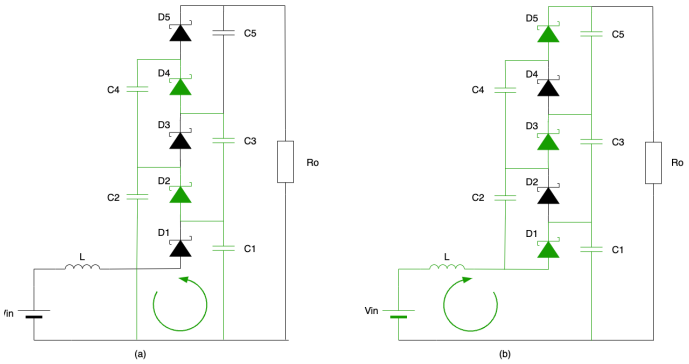


Fig. 2 Equivalent 2N-1 circuit for (a) Mode 1 switch conduction, (b) Mode 2 switch blocking

*2.1.2 Negative Inverting 2N:* During Mode 2 operation, the lowest level uncharged oscillating (even-numbered) capacitor is charged by the input and inductor voltages and the charged output (odd-numbered) capacitors via the previous capacitor's (N-1) corresponding diode. During Mode 1 operation, the lowest level uncharged output capacitor is charged by the charged oscillating capacitors via the previous capacitor's diode. Figure 3 shows the equivalent circuits used for analysis during 2N operation.

*2.1.3 Proposed Converter Operation:* During operation, the 2N-1 and inverting 2N topologies build up charge independently. Additionally, the topologies discharge during alternating modes. During Mode 1 operation, the negative inverting 2N

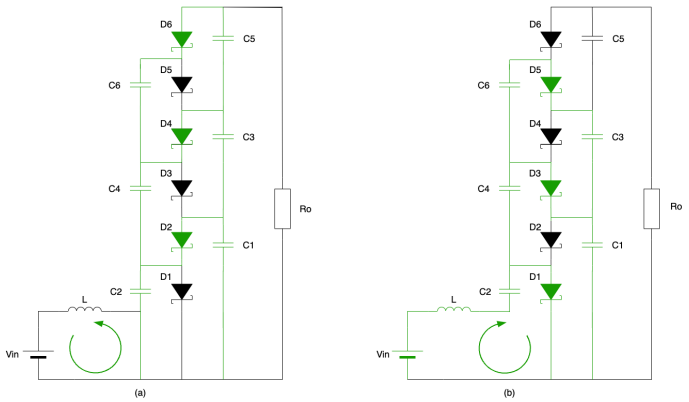


Fig. 3 Equivalent 2N circuit for (a) Mode 1 switch conduction, (b) Mode 2 switch blocking

topology discharges into the load. The positive 2N-1 topology discharges into its load during Mode 2.

### 2.2 Proposed Converter Analysis

Following a similar analysis used in [17] the ideal gain for the proposed converter design may be expressed as:

$$\frac{V_O}{V_{in}} = \pm\frac{N}{1-D} \tag{1}$$

where $V_O$ is the output voltage, $V_{in}$ is the input voltage, $N$ is the number of levels, and $D$ is the duty ratio.

Reduction in the output voltage arising from the forward voltage of the diodes, the equivalent series resistance of the inductors and capacitor voltage drops must be considered for practical applications [17, 18]. Assuming that the voltage losses associated with diodes and inductor resistances are insignificant compared to the magnitude of the output voltage, only capacitor voltage drops need to be considered. Assuming all capacitors are identical, the general voltage drop equation presented in [18] may be incorporated to predict the non-inverting gain:

$$\frac{V_{O+}}{V_{in}} = \frac{N}{1-D} - \frac{(4N^3+3N^2-N)}{6fCR_{O+}} \tag{2}$$

where $V_{O+}$ is the non-inverting output voltage, $R_{O+}$ is the output resistance, $f$ is the switching frequency and $C$ is the capacitance.

For analytical purposes, the Inverting 2N topology is functionally identical to the 2N-1 topology. Therefore, the same method may be utilised resulting in the following expression for, the inverting gain:

$$\frac{V_{O-}}{V_{in}} = -\frac{N}{1-D} + \frac{(4N^3+3N^2-N)}{6fCR_{O-}} \tag{3}$$

where $V_{O-}$ is the inverting output voltage, $I_{O-}$ is the inverting output current and $R_{O-}$ is the inverting topology load.

As the multiplier ladders operate independently, assuming equal output resistances, Equations 2 and 3 may be combined to express the proposed converter output gain.

$$\frac{V_O}{V_{in}} = \pm\frac{N}{1-D} \mp \frac{(4N^3+3N^2-N)}{6fCR_O} \tag{4}$$

*2.2.1 Inductor:* As the inductor current is largely dependent on the output resistance, for the same output power, the utilisation of 2 voltage-multiplying topologies effectively doubles the inductor current, compared to the operation of the conventional single inductor topology. The average inductor current may be given as:

$$< I_L >= \frac{2N^2V_{in}}{(1-D)^2R_O} \tag{5}$$

where $< I_L >$ is the average inductor current. With this, the average steady-state inductor voltage may be determined with

$$\begin{aligned} < V_L >= D(V_{in} - I_L R_{EsrL}) + (1-D)(V_{in} \\ -I_L R_{EsrL} - V_{C1} - V_D) = 0 \end{aligned} \tag{6}$$

where $< V_L >$ is the average inductor voltage, $V_{C1}$ the voltage across $C_1$ and $V_D$ the diode forward voltage.

*2.2.2 Capacitor:* For an ideal voltage multiplier, the expected voltage output at each stage may be determined utilising Equation 1 and the voltage sharing characteristic of Cockcroft Walton multipliers, where $V_{C1} = V_{C2} = V_{C3}$, to give:

$$V_C = \pm\frac{1}{1-D} \tag{7}$$

For practical applications, the impact of capacitor voltage drop should be considered. At each stage on the voltage multiplier, assuming equal capacitance, the voltage drop analysis from [18] may be utilised. The voltage drops at each output stage of the voltage multiplier may be given as:

$$\Delta V_{Ck} = \mp\frac{I_{O+}(N+k+1)(N-k)}{2fC} \tag{8}$$

where $N$ is the total number of stages and $k$ is the given stage. With this, the capacitor voltage of any stage in the ladder may be calculated:

$$V_{Ck} = \pm\frac{V_{in}k}{1-D} - \Delta V_{Ck+} \tag{9}$$

where $V_{Ck}$ is the voltage of a given capacitor stage referenced to ground.

Although not explored here, with the proposed topology the ability to produce a bipolar, multilevel output offers the potential to modify the design to realise a DC-AC converter by treating the output capacitors as if they were the input capacitors of a half-bridge inverter and adding a switching device between each stage.

*2.2.3 Diode:* During operation, for the non-inverting topology, The odd numbered diodes conduct during Mode 1, creating charge pathways for output capacitors. During Mode 2 even numbered diodes conduct, creating charge pathways for smoothing capacitors. Following these charge patterns the maximum diode voltages, $V_{Dk}$ , may be determined as:

$$V_{Dk} = V_{Ck} \tag{10}$$

Assuming that the average capacitor current per switching cycle is zero it may be deduced that:

$$I_D = I_{O+} \tag{11}$$

Utilising the same method outlined for the inverting topology for diode characteristics, based on Figure 3:

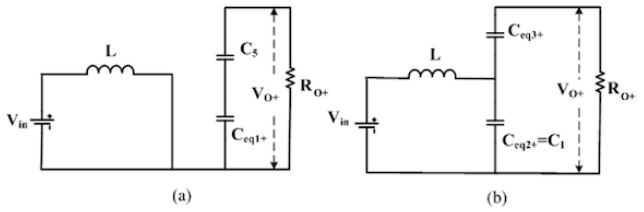


Fig. 4 Reduced-Order equivalent 2N-1 circuit for (a) Mode 1 switch conduction, (b) Mode 2 switch blocking

$$V_{Dk} = -V_{Ck} \tag{12}$$

$$I_D = I_{O-} \tag{13}$$

*2.2.4 Switch:* Utilising the same analysis for the capacitor voltages, the switch drain-source voltage may be expressed as:

$$< V_{DS} >= V_{C1} = \frac{1}{1-D} - \frac{I_{O+}(N+2)(N-1)}{2fC} \tag{14}$$

and the drain-source current is calculated as:

$$I_{DS} = I_L - I_{D1+} - I_{D1-} \tag{15}$$

where $I_{DS}$ is the drain-source current, $I_{D+}$ and $I_{D-}$ the current in the positive and negative diodes, respectively.

*2.2.5 State-space representation:* The dynamic equations governing the inductor current and capacitor voltages in the proposed converter result in a state-space model characterized by 7 state variables. However, to reduce the complexity of the system, a simplified equivalent circuit, as depicted in Figures 4 and 5 can be employed to derive a reduced-order model of the converter with 3 control variables. This assumes that the voltages across the output capacitors are balanced and equal, resulting in.

$$V_{c_1\pm} \approx V_{c_3\pm} \approx V_{c_5\pm} \approx \frac{V_{O\pm}}{3} \tag{16}$$

where $V_{O\pm}$ is the output voltage for each polarity of the proposed converter. Moreover, it is assumed that all the capacitors have equal capacitance values, $C_1$ = $C_2$ = $C_3$ = $C_4$ = $C_5$ = $C$.

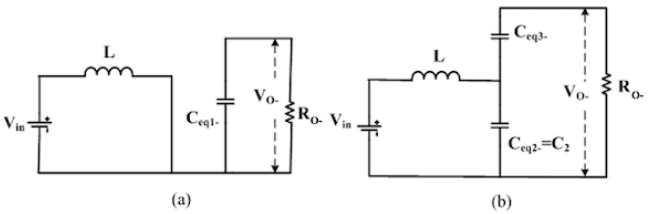


Fig. 5 Reduced-Order equivalent 2N circuit for (a) Mode 1 switch conduction, (b) Mode 2 switch blocking

The dynamic equations for inductor current and output voltages for Mode 1 operation can be obtained as follows.

$$L\frac{di}{dt} = V_{in} \tag{17}$$

$$C_{eq1+}\frac{dV_{O+}}{dt} = \frac{-3V_{O+}}{R_{O+}} \tag{18}$$

$$C_{eq1-}\frac{dV_{O-}}{dt} = \frac{-3V_{O-}}{R_{O-}} \tag{19}$$

where, $C_{eq1+}$ = $C$ and $C_{eq1-}$= 0.66$C$. Similarly, based on the Mode 2 of operation, the dynamics of the system can be represented as,

$$L\frac{di}{dt} = V_{in} - \frac{V_{O+}}{3} \tag{20}$$

$$C_{eq2+}\frac{dV_{O+}}{dt} = i_L - \frac{3V_{O+}}{R_{O+}} \tag{21}$$

$$C_{eq2-}\frac{dV_{O-}}{dt} = -i_L - \frac{3V_{O-}}{R_{O-}} \tag{22}$$

where, $C_{eq2+}$ = $C_{eq2-}$ = $C$. However, neglecting the voltage drop across the diode,

$$V_{O+} \approx -V_{O-} \tag{23}$$

Thus, equation (20) can be reframed as,

$$L\frac{di}{dt} = V_{in} - \frac{V_{O+} - V_{O-}}{6} \tag{24}$$

The state space model of the proposed converter is derived based on the reduced order model equations. Considering the system model '$X$' fed with an input '$U$' generates an output '$Y$', the state space equations of the proposed converter can be represented as,

$$\begin{aligned} \dot{X} &= AX + BU \\ Y &= CX + DU \end{aligned} \tag{25}$$

As the converter exhibits two modes of operation, an average model is utilized for the state-space representation such that,

$$A = A_1 D + A_2(1-D) \tag{26}$$

where, $A_1$ and $A_2$ represent the system matrices when the converter is operated in Mode 1 and Mode 2, respectively with a duty ratio of '$D$'. Similarly, the matrices, [B], [C] and [D] are represented using their average models. By applying the Laplace transform to Equations (17)-(22), the state space model of the proposed converter can be obtained as per the following equation.

$$\begin{bmatrix} \dot{I_L} \\ \dot{V_{o+}} \\ \dot{V_{o-}} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-(1-D)}{6L} & \frac{(1-D)}{6L} \\ \frac{1-D}{C_+} & \frac{-3}{R_{O+}C_+} & 0 \\ \frac{-(1-D)}{C_-} & 0 & \frac{-3}{R_{O-}C_-} \end{bmatrix} \begin{bmatrix} I_L \\ V_{o+} \\ V_{o-} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \end{bmatrix} V_{in} \tag{27}$$

where, $C_+$= $DC_{eq1+}$+(1-$D$)$C_{eq2+}$ and $C_-$= $DC_{eq1-}$+(1-$D$)$C_{eq2-}$.

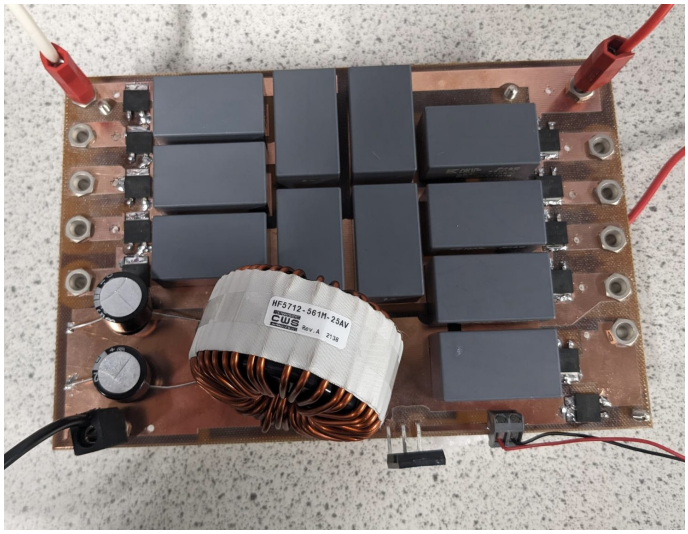

Fig. 6. Experimental Demonstrator unit

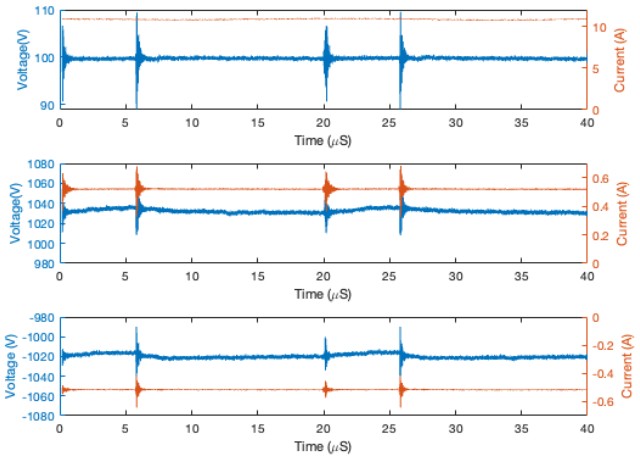


Fig. 7 Input and output voltage and current waveforms of the proposed topology

For positive output, the output matrix is defined as,

$$Y_+ = \begin{bmatrix} 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} I_L \\ V_{o+} \\ V_{o-} \end{bmatrix} \tag{28}$$

For negative output, the output matrix is represented by the following equation.

$$Y_- = \begin{bmatrix} 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} I_L \\ V_{o+} \\ V_{o-} \end{bmatrix} \tag{29}$$

## 3 Experimental validation

To demonstrate the proposed topology a demonstrator unit was developed and experimentally characterised with a predicted voltage gain of 10. The parameters for the converter are outlined in Table 1.

Table 1 Experimental parameters of the proposed converter

| Parameters | Value |
|---|---|
| $V_{In}$ | 100 V |
| $R_{O+}$, $R_{O-}$ | 2 kΩ |
| $L$ | 500 $\mu$ H |
| $C$ | 11 $\mu$F |
| Switching frequency | 50 kHz |
| $D$ | 0.72 |
| $R_{EsrL}$ | 26 mΩ |
| $V_D$ | 0.7 V |

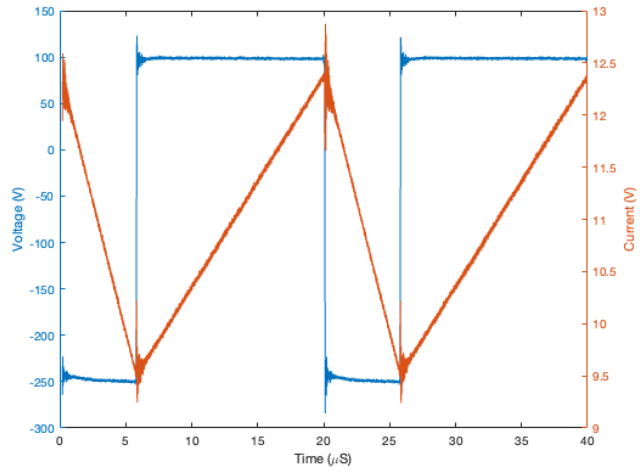


Fig. 8 Input inductor waveforms of the output capacitors of the proposed topology.

### *3.1 Experimental Results*

Based on Figure 7, for a 100 V input, the average output voltages of the proposed converter were 1030 V and -1020 V demonstrating a balanced gain of approximately 10. The output power was calculated as 670 W and 657 W for the non-inverting and inverting branches, respectively. With this, the power efficiency was calculated to 98 %.

The waveforms in Figure 8, show the converter operating in continuous conduction mode. During Mode 1 the voltage across the inductor was 100 V and -251 V during Mode 2 with an average current of 11 A This behaviour is consistent with the operational analysis highlighted in Section 2.2.1.

The data in Figure 9 presents the output capacitor voltages for both the inverting and non-inverting branches of the demonstrator unit. It can be seen that during Mode 1 the positive

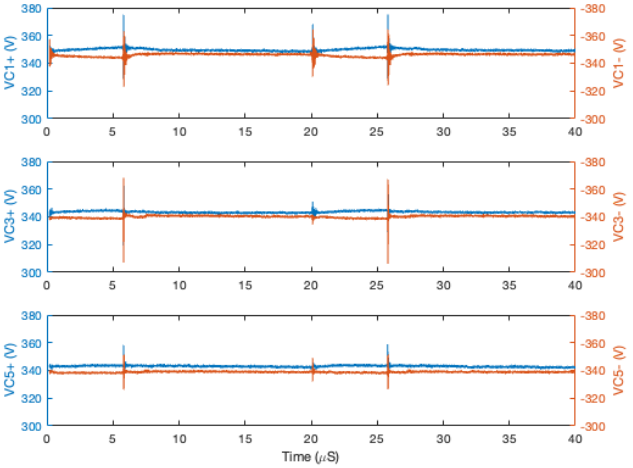


Fig. 9 Output capacitor waveforms of the output capacitors of the proposed topology.

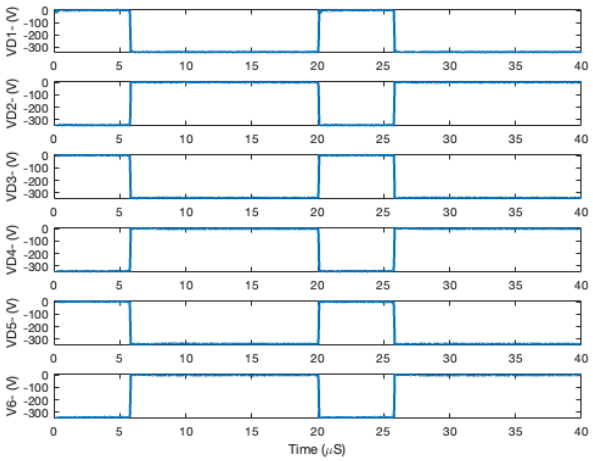


Fig. 11. Inverting diode waveforms of the proposed topology.

output capacitors are charged. Conversely, during Mode 2, the negative output capacitors are charged which is in agreement with the operation description outlined in Sections 2.1.1 and 2.1.2. the average observed voltage of $V_{C1+}$ and $V_{C1-}$ were 350 V and 346 V respectively, highlighting a reduced voltage magnitude on the inverting topology, likely due to the additional diode and capacitor, however, the difference was deemed small enough to justify utilising the method outlined in [18] for the inverting topology. Additionally, a voltage drop of approximately 5V between, both inverting and non-inverting, C1 & C3 and 1V between C3 & C5 was observed supporting the voltage drop analysis described in Section 2.2.2.

Figures 10 and 11 show the diode operating voltages for the non-inverting and inverting multipliers respectively, both sets of waveforms support the operation outlined in Section 2.2.3.

Figure 12 shows the voltage stress across the switching device, When blocking, is approximately 350 V, which is equal to $V_{C1+}$. This demonstrates one of the key benefits of the Cockcroft-Walton voltage multiplier, by limiting the voltage stress across the switching device, a lower blocking voltage switch may be used to generate an output voltage much greater than the rated voltage of the switch.

The data in Table 2 compares the proposed design against similar topologies reported within the literature.

The results show that the proposed topology may produce significant voltage gains similar to that previously shown within the literature, focusing on achieving a high voltage gain [11, 20] while producing a continuous bipolar output with greater efficiency than other reported designs [8, 9]. This demonstrates the proposed topology's potential to operate a DC-link for unipolar LVDC to bipolar MVDC networks.

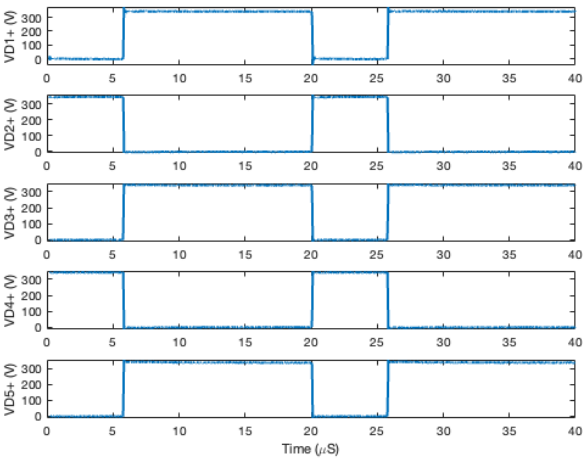


Fig. 10 Non-Inverting diode waveforms of the proposed topology.

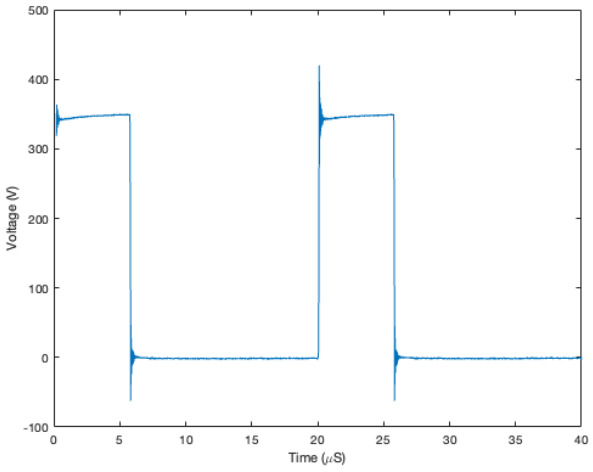


Fig. 12 Drain-Source voltage waveform of the proposed topology.

Table 2 Comparison with similar topologies

| Topology | Voltage Gain | Switch Voltage | Maximum Efficiency |
|---|---|---|---|
| [8] | $\pm\frac{D}{1-D}$ | - | 92% |
| [9] | $\pm\frac{D}{1-D}$ | $V_O + V_{in}$ | 88% |
| [11] | $\pm\frac{1}{1-2D}$ | $\frac{V_O}{2}$ | - |
| [19] | $\frac{2N-1}{(N-1)(1-D)}$ | $\frac{V_O(N-1)}{(2N-1)}$ | 96.2% |
| [20] | $\frac{2(1-D)}{1-2D}$ | $\frac{V_{in}}{1-2D}$ | 94% |
| Proposed | $\pm\frac{N}{1-D}$ | $\frac{V_O}{N}$ | 98% |

## 4 Conclusion

This paper demonstrates a novel DC-DC converter designed to operate as a DC link to a bipolar collection network. A detailed analysis of the proposed topology was presented with a focus on the minimisation of capacitor losses. A demonstrator unit was developed to experimentally validate both operation and analysis, demonstrating a 98% power efficiency. The converter topology was able to produce significant bipolar gains while only requiring a single active switching device, limiting potential failure points and allowing for the use of simplistic control schemes.

## 5 Acknowledgements

The Lead author is a member of the AURA Centre for Doctoral Training, which is supported by the Engineering and Physical Sciences Research Council, project reference: EP/S023763/1 2744310. The second, fourth, fifth and sixth authors aided in this research as part of the Wind2DC project, project reference: EP/X033120/1

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