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# Steady-State Analysis of Class-E/$F_n$ Inverter with MOSFET Nonlinear Output Capacitance at any Grading Coefficient

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**ABSTRACT** In this paper, the analysis and design of a class-E/$F_n$ inverter using analytically expressions is provided for any grading coefficient *m* of the MOSFET body junction diode at 50% duty ratio. Generally, the class-E zero-voltage switching (ZVS) and zero-derivative voltage switching (ZDVS) conditions prepared the switch-mode operation inverter to obtain high power conversion efficiency performance. On the other hand, harmonics tuning and waveforms shaping in the load-network lead to the class-F inverter configuration. The combination of the switch-mode operating with waveforms shaping provides the class E/$F_n$ inverter. The MOSFET nonlinear drain-source parasitic capacitance is highlighted as determinative element in this operation mode. The nonlinearity characteristic of the MOSFET drain-source parasitic capacitance is required to include as the design specification for the satisfaction of the peak switch voltage and output power simultaneously. Furthermore, the grading coefficient *m* has considerably and directly made effects on both the output power capability and maximum operating frequency. The design and implementation of the class-E/$F_3$ inverter using the grading coefficient *m* as an adjustment parameter is performed. The close agreement between the analytical and PSpice simulations proved the effectiveness of the provided theoretical expressions. Therefore, the usefulness of analytical expressions is confirmed by high accuracy obtaining results from the laboratory measurements for the prototype fabricated circuit.

**INDEX TERMS** Class-E/$F_3$ inverter, class-E conditions, class-F operation, waveform shaping, harmonics tuning, grading coefficient of junction capacitance, output power, MOSFET nonlinear drain-source parasitic capacitance, zero-voltage switching (ZVS), peak switch voltage.

## I. INTRODUCTION

High efficiency switch-mode inverters with high-frequency operation are basic module for modern power electronics systems [1]–[5]. plenty, the class-E inverter with a shunt capacitance configuration operate based the switch-mode operation terms as zero-voltage switching (ZVS) and zero-derivative voltage switching (ZDVS) conditions to achieve zero power dissipation in the switching device [6]– [9]. Another technique is waveform shaping that used an infinite number of even-harmonics in the load-network [10]– [12]. This operation mode is an idealized inverse-class-F mode that prepared with a half-sinusoidal voltage waveform and a square current waveform at the switch element output node. The combined mode as class-E/F enforced switching and harmonics tuning simultaneously to increase the efficiency of power inverter [13]– [16]. Since the introduction of the class-E/F inverter with a shunt capacitance topology many applications, such as wireless power transfer (WPT) [17], dc–dc converter [18], high-power-factor inverter [19], and so on were proposed. These implementations are required to use the class-E/F inverter configuration as the basic module for the design of overall power electronics system.

The shunt capacitance of the MOSFET device is a quite important element for the class-E operation mode to achieve

high-efficiency at high-frequency, which becomes much considerable as the operating frequency increases [20], [21]. The MOSFET nonlinear drain-source parasitic capacitance determined the overall required shunt capacitance to satisfy the class-E ZVS and ZDVS conditions. However, the output power and power conversion efficiency are effectively affected by this intrinsically characteristic of the MOSFET. Based on these major criteria, the analysis of the class-E/F inverter with an accurate analytical relationship is critically required to create an intuitive environment for obtaining element values, switch element selection and waveforms equations.

Several design considerations of the class-E/F inverter using a linear external shunt capacitance with the switch element are proposed in [22]–[25]. In these studies, the effect of the MOSFET nonlinear drain-source parasitic capacitance was ignored that leads to a considerable deviation from ZVS and ZDVS conditions. This deviation makes a considerable degradation of power conversion efficiency due to occur an overlap between the switch voltage and current waveforms. Moreover, the design equations based on the linear drain-source capacitance have low accuracy. The effect of MOSFET drain-source capacitance using a simplified nonlinear function that is a special case was studied in [26]. In this case, the design relationships were obtained using some of design charts and a case study for only the fixed grading coefficient *m* of the MOSFET body junction diode that is equal to 0.5. These simplified design charts have low accuracy to estimate of the class-E/$F_n$ inverter performance from output power and safe working area for the MOSFET peak switch voltage point of view. On the other hand, this parasitic shunt capacitance has a nonlinear characteristic as a function of the grading coefficient *m* for the MOSFET body junction diode that makes major effect on the overall performance of the class-E/$F_n$ inverter due to the deviation from ZVS and ZDVS conditions.

It can be concluded from above discussions that the highlighted problem in the design of the class-E/$F_n$ inverter is the simultaneously satisfaction of the arbitrary design parameters. Although, the class-E/$F_n$ inverter with only ZVS condition, i.e., sub-nominal operation is an adequately solution approach [27], but due to the fixed grading coefficient *m* of the MOSFET body junction diode, this design methodology is limited with a considerably design deviations. Moreover, the output power is obtained as a function of the given design specifications such as: dc-supply voltage, load-resistance and peak switch voltage. In some power electronics applications [28]-[31], the output power should be given as design specification to implement of the power converter module. This quite important requirement can be obtained with taken into account the grading coefficient *m* of the MOSFET body junction diode as an adjustment parameter. The smooth rise of the switch current waveform at the turn-on instant is detected by ZDVS condition, while the ZVS condition creates a jump of the switch current waveform at the turn-on instant. These two major phenomena are directly

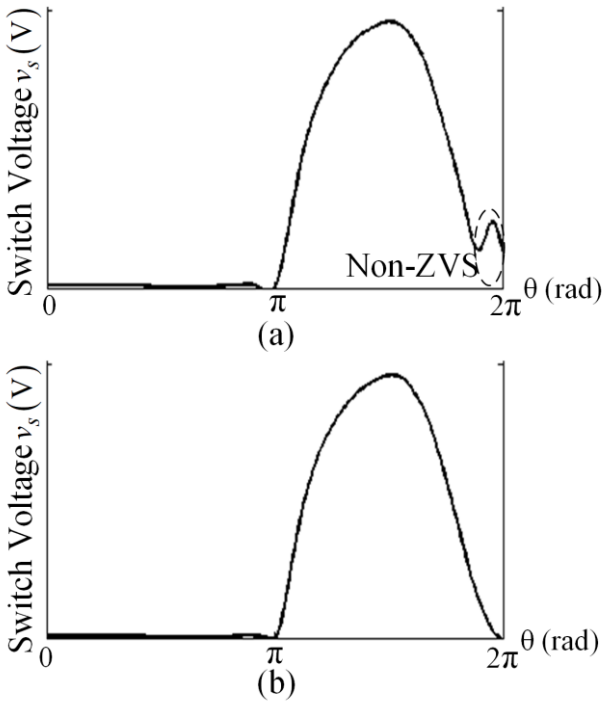


**FIGURE 1. The class-E/$F_3$ inverter waveforms from PSpice-simulation using the elements values [25] for IRF510 MOSFET. (a) For non-zero the MOSFET nonlinear drain-source capacitance. (b) For zero the MOSFET nonlinear drain-source capacitance.**

affected by the grading coefficient *m* of the MOSFET body junction diode.

The circuit simulation of the switch-voltage waveform for the class-E/$F_3$ inverter using the design relationships with only a linear shunt capacitance [25] and a practical PSpice MOSFET model by considering of the nonlinear drain-source parasitic capacitance is depicted in Fig. 1 (a). It can be stated from this plot that the switch-voltage waveform deviated from the class-E ZVS/ZDVS conditions due to neglecting of the grading coefficient *m*. This major drawback leads to power conversion efficiency degradation. Figure 1 (b) depicts the switch-voltage waveform of the PSpice-simulation using the design equations in [25] by omitting the MOSFET nonlinear drain-source parasitic capacitance. In this subfigure, the class-E ZVS/ZDVS conditions are obtained. Hence, the analysis of the class-E/$F_n$ inverter with any grading coefficient *m* is quite important not only for achieving the class-E ZVS/ZDVS conditions but also for considering the output power as design specifications. The really fabricated MOSFETs have a wide range diversity in the grading coefficient *m*, for example, over 90 % of the 914 Spice models manufactured by International Rectifier have a grading coefficient *m* non-equal to 0.5 [32]. Therefore, it is technically required to obtain the design equations using analytical expressions for the class-E/$F_n$ inverter with the MOSFET nonlinear drain-source parasitic capacitance at any grading coefficient *m*.

This paper provides analytical relationships of design equations and waveforms for the class-E/$F_n$ inverter with the MOSFET nonlinear drain-source capacitance at any grading

coefficient $m$ in the duty ratio 0.5. The satisfaction of the given output power and peak switch voltage along with the class-E ZVS/ZDVS conditions are simultaneously done by enforcing the grading coefficient $m$ as an adjustment parameter. The effects of the grading coefficient $m$ on both output power capability and power conversion efficiency are studied. The effectiveness of the obtained theoretically analysis is demonstrated by quantitative converging with both PSpice simulations and laboratory experiments results that extracted from the fabricated prototype circuit.

## II. CLASS-E/Fn INVERTER CIRCUIT DESCRIPTION

Fig. 2(a) depicts the fundamental circuit configuration of an ideal class-E/F$_n$ inverter, which consists of a dc-supply voltage $V_{DD}$, a MOSFET as the switching element $S$, dc-feed inductor $L_{RFC}$, nonlinear shunt capacitance $C_{ds}$, a parallel series resonant filter $L_n$-$C_n$ tuned to $n^{th}$ harmonic of the fundamental operating frequency, and series resonant filter $L$-$C_0$-$R$. The switch is in the on-state for $0 \le \theta < \pi$ and is in the off-state for $\pi < \theta \le 2\pi$, where $\theta$ is the angular time. The MOSFET turns on and off alternatively at $\theta = 0$ and $\pi$.

### A. Circuit Operation Hypothesizes

The following fundamentally hypothesizes are used to accomplish the analytical relationships of design and waveform expression for the class-E/F$_n$ inverter.

1) The shunt capacitance is the MOSFET drain-source nonlinear parasitic junction capacitance, which is described by a nonlinear function as

$$C_{ds} = \frac{C_{j0}}{\left(1+\frac{v_s}{V_{bi}}\right)^m}, \tag{1}$$

where $V_{bi}$ is the built-in potential, whose typical value is in the region from 0.5 to 0.9 V for silicon MOSFETs, $v_s$ is the voltage between the drain and source, $C_{j0}$ is the junction capacitance at $v_s = 0$, and $m$ is the grading coefficient.

2) The MOSFET works as an ideal switch with zero switch on-state resistance and infinite switch off-state resistance.

3) The dc-feed inductance $L_{RFC}$ is large enough to obtain an essentially constant current $I_{DD}$ through the dc-feed inductance.

4) The switch voltage satisfies the ZVS and ZDVS conditions as

$$v_s(\theta = 2\pi) = 0, \tag{2}$$

and

$$\left.\frac{dv_s(\theta)}{d\theta}\right|_{\theta=2\pi} = 0, \tag{3}$$

respectively.

5) The loaded quality factor $Q$ of the output resonant circuit, which is defined as

$$Q = \frac{\omega L}{R}, \tag{4}$$

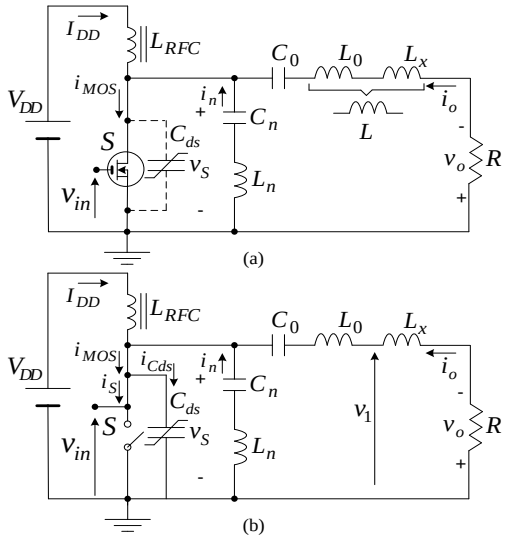


**FIGURE 2. Class-E/Fn inverter with a nonlinear shunt capacitance. (a) Basic circuit topology. (b) Idealized equivalent circuit.**

is high enough to generate a pure sinusoidal output current at the fundamental operating frequency as

$$i_o(\theta) = I_m \sin(\theta + \varphi), \tag{5}$$

where $\varphi$ is a phase shift between the input voltage and output one.

6) The current through the parallel series resonant filter $L_n$-$C_n$ at $n^{th}$ harmonic of the fundamental operating frequency is defined as

$$i_n(\theta) = I_n \sin(n\theta), \tag{6}$$

7) All elements including the MOSFET parasitic capacitances have no parasitic resistance.

Based on the above operation hypothesizes of the class-E/F$_n$ inverter, the equivalent circuit is obtained as shown in Fig. 2(b).

### B. Model and Syntheses Equations

The MOSFET is in the on-state for $0 \le \theta < \pi$, and the current through the shunt capacitance $i_{Cds}(\theta)$ is zero, therefore, we have

$$i_{MOS}(\theta) = i_s(\theta) = I_{DD} + I_m \sin(\theta + \varphi) + I_n \sin(n\theta), \tag{7}$$

The initial condition of the switch current is

$$i_s(\theta = 0) = 0, \tag{8}$$

From (8) and (7), we have

$$I_{DD} = -I_m \sin(\varphi), \tag{9}$$

For $\pi < \theta \le 2\pi$, the MOSFET is in the off-state, and the switch current is

$$i_s(\theta) = 0, \tag{10}$$

Therefore, the current through the MOSFET during the off-state is also expressed as

$$i_{MOS}(\theta) = i_{C_{ds}}(\theta) + i_s(\theta) = \omega \frac{C_{j0}}{\left(1+\frac{v_s}{V_{bi}}\right)^m} \frac{dv_s}{d\theta}, \tag{11}$$

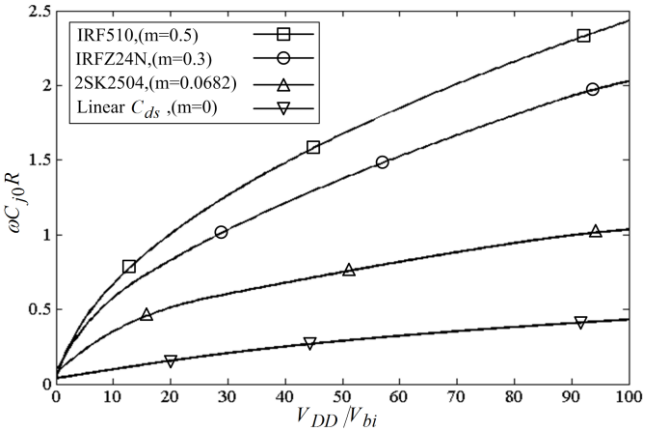


**FIGURE 3.** $\omega C_{j0}R$ **in terms of** $V_{DD}/V_{bi}$ **for different values of the grading coefficient** ***m*** **and linear drain-source capacitance.**

TABLE I
CHARACTERISTICS OF THE MOSFETS

| | *m* | $V_{bi}$ (V) | $C_{j0}$ (pF) | $r(\Omega)$ |
|---|---|---|---|---|
| 2SK2504 | 0.0682 | 0.8 | 217 | 0.1 |
| IRFZ24N | 0.3 | 0.51 | 297 | 0.07 |
| IRF510 | 0.5 | 0.8 | 366.5 | 0. 45 |

where $i_{Cds}$ is the current through the drain-source capacitance $C_{ds}$. We have rewritten (11) as

$$\omega\int_{v_s}^{0}\frac{C_{j0}}{\left(1+\frac{v_s'}{V_{bi}}\right)^m}dv_s' = \int_{\pi}^{\theta} i_{MOS}(\theta')d\theta', \quad \text{for } \pi<\theta\le 2\pi. \tag{12}$$

By substituting (7) in (12), the switch voltage for $\pi<\theta\le 2\pi$ can be calculated as

$$\frac{v_s}{V_{bi}} = \left\{1-\frac{1-m}{\omega C_{j0}V_{bi}}\left[\begin{array}{l} I_{DD}(\theta-\pi)- \\ I_m\left(\cos(\theta+\varphi)+\cos(\varphi)\right)- \\ \frac{I_n}{n}\left(1+\cos(n\theta)\right)\end{array}\right]\right\}^{1/(1-m)} -1. \tag{13}$$

Imposing the ZVS condition in (13) leads to

$$I_{DD} = \frac{2}{\pi}I_m\cos(\varphi)+\frac{2I_n}{n\pi}. \tag{14}$$

The amplitude of the $n^{th}$ harmonic is obtained from the Fourier transform of the switch current as

$$I_n = \frac{1}{\pi}\int_0^{2\pi} i_s(\theta')\sin(n\theta')d\theta' = \frac{2I_{DD}}{n\pi}\left(1-\cos(n\pi)\right). \tag{15}$$

For odd value of $n$ the normalized amplitude of the $n^{th}$ harmonic by the dc-supply current is

$$\frac{I_n}{I_{DD}} = \frac{4}{n\pi}. \tag{16}$$

By substituting (16) into (14), the amplitude of the output current can be calculated as

$$I_m = \frac{\pi I_{DD}}{2\cos(\varphi)}\left(1-\frac{8}{n^2\pi^2}\right). \tag{17}$$

The class-E/$F_n$ inverter is assumed without parasitic resistance that leads to zero power dissipation in the inverter circuit. Therefore, the output power $P_{out}$ is equal to the DC-supply power $P_{DC}$, namely, $V_{DD}I_{DD} = RI_m^2/2$. Thus, from (17), the dc-supply current is given by

$$I_{DD} = \frac{V_{DD}}{R}\frac{2}{\left[\frac{\pi}{2\cos(\varphi)}\left(1-\frac{8}{n^2\pi^2}\right)\right]^2}. \tag{18}$$

From (17) and (18), the amplitude of the output current is given as

$$I_m = \frac{V_{DD}}{R}\frac{2\cos(\varphi)}{\pi\left(1-\frac{8}{n^2\pi^2}\right)}. \tag{19}$$

The dc-supply voltage is the average value of the switch voltage, which can be defined as

$$V_{DD} = \frac{1}{2\pi}\int_0^{2\pi} v_s(\theta)d\theta = \frac{1}{2\pi}\int_{\pi}^{2\pi} V_{bi}\left\langle\left\{1-\frac{1-m}{\omega C_{j0}R}\frac{V_{DD}}{V_{bi}}\times\right.\right.$$

$$\left[\frac{2(\theta-\pi)}{\left[\frac{\pi}{2\cos(\varphi)}\left(1-\frac{8}{n^2\pi^2}\right)\right]^2}-\frac{2\cos(\varphi)}{\pi\left(1-\frac{8}{n^2\pi^2}\right)}\left(\cos(\theta+\varphi)+\cos(\varphi)\right)-\right.$$

$$\left.\left.\left.\frac{8}{n^2\pi\left[\frac{\pi}{2\cos(\varphi)}\left(1-\frac{8}{n^2\pi^2}\right)\right]^2}\left(1+\cos(n\theta)\right)\right]\right\}^{1/(1-m)} -1\right\rangle d\theta. \tag{20}$$

It can be concluded that (20) considered in terms of $\varphi$, $V_{DD}/V_{bi}$, $\omega C_{jo}R$, and $m$. By substituting (9) into (17) the phase shift $\varphi$ is

$$\tan(\varphi) = \frac{2}{\pi\left(\frac{8}{n^2\pi^2}-1\right)}. \tag{21}$$

In this paper, to obtain the analytical expressions for the proposed class-E/$F_n$ inverter, the phase shift $\varphi$ in (21) for a specific value of the third-harmonic, i.e., $n$=3 is -0.610516 (rad). Hence, when the two of three variables such as: $V_{DD}/V_{bi}$, $\omega C_{jo}R$, and $m$ are given as design specifications, the values of another variable can be calculated numerically by solving (20). In this study, three types of MOSFETs are considered such as 2SK2504, IRFZ24N and IRF510 from Rohm and International Rectifier, respectively, which have different grading coefficient $m$. The value of $V_{bi}$ , $m$, and $C_{jo}$ are

specified by selecting of the MOSFET, which are extracted from the SPICE models [32], as prepared in Table I.

Figure 3 plots $\omega C_{jo}R$ in terms of the normalized dc-supply voltage, i.e., $V_{DD}/V_{bi}$ for three types of the MOSFETs with the different grading coefficient $m$, where $m$=0 shows a linear drain-source capacitance. It is seen from this figure that the $\omega C_{jo}R$ increased with the increment of the grading coefficient $m$ for the fixed dc-supply voltage. In this case, the operating frequency can be increased easily without any external auxiliary circuit while the dc-supply voltage is restricted from the output power point of view. Therefore, the proper selection of the grading coefficient $m$ is an efficient way to obtain the required maximum operating frequency.

## III. RESONANT CIRCUIT REACTANCE

The voltage across $L$ and load-resistance $R$ that is depicted in Fig. 2(b), can be calculated as

$$v_1(\theta) = V_1 \sin(\theta + \varphi_1), \tag{22}$$

where

$$V_1 = V_m \sqrt{1 + \left(\frac{\omega L_x}{R}\right)^2}, \tag{23}$$

and

$$\varphi_1 = \varphi + \arctan\left(\frac{\omega L_x}{R}\right). \tag{24}$$

The reactance of the series resonator $L_0$-$C$ at the operating frequency is zero. Hence, we can implement Fourier's formula as

$$\frac{1}{\pi}\int_0^{2\pi} v_s(\theta)\cos(\theta + \varphi_1)d\theta = 0. \tag{25}$$

From the expansion of (25), the expression for $\varphi_1$is obtained as

$$\tan\varphi_1 = \frac{\int_\pi^{2\pi} v_s(\theta)\cos\theta d\theta}{\int_\pi^{2\pi} v_s(\theta)\sin\theta d\theta}. \tag{26}$$

Therefore, (24) can be rewritten as

$$\frac{\omega L_x}{R} = \tan(\varphi_1 - \varphi). \tag{27}$$

Figure 4 depicts $\omega L_x/R$ in terms of $V_{DD}/V_{bi}$ for three types of the MOSFETs and a linear drain-source capacitance. It is seen from Fig. 4 that $\omega L_x/R$ becomes zero at $V_{DD}/V_{bi}$ =12.4 and 8.6 for $m$=0.5 and 0.3, respectively, which means that the resonant frequency is the same as operating frequency. Moreover, for $m$=0.0682 and $m$=0 the value of $\omega L_x/R$ reaches to zero for $V_{DD}/V_{bi}$ =0. These two different behaviors shows that the design range is restricted for MOSFETs with nonlinear characteristics and higher values of grading coefficient than linear ones. The value of $\omega L_x/R$ increases as $m$ decreased, because the value of the series capacitance in the output series resonant filter decreased as the grading coefficient $m$ increases.

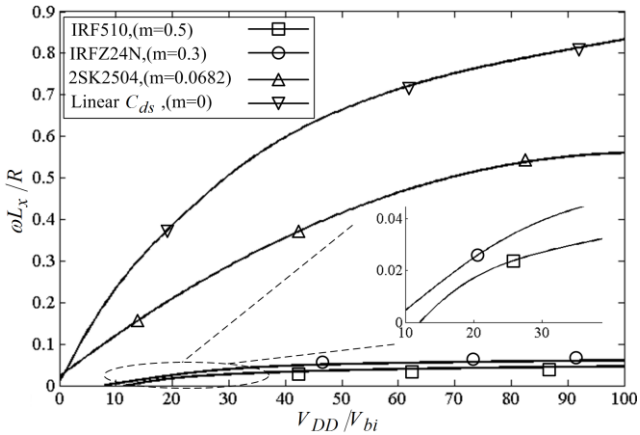


**FIGURE 4.** $\omega L_x/R$ **in terms of** $V_{DD}/V_{bi}$ **for different values of the grading coefficient** ***m*** **and linear drain- source capacitance.**

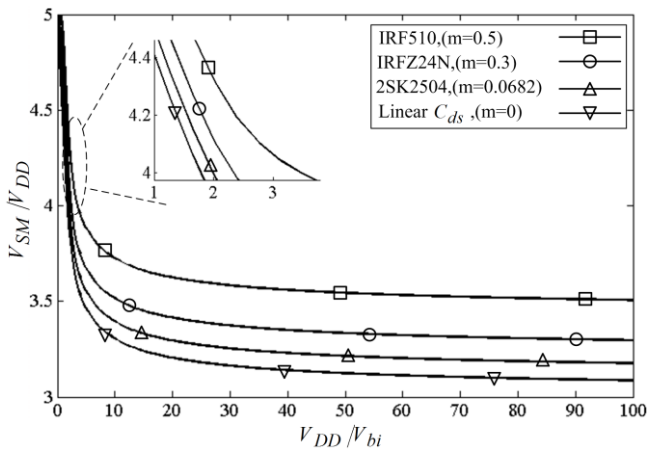


**FIGURE 5.** $V_{SM}/V_{DD}$ **in terms of** $V_{DD}/V_{bi}$ **for different values of the grading coefficient** ***m*** **and linear drain-source capacitance.**

## IV. Switch Stresses Analysis

The peak switch voltage and peak switch current are defined as $V_{SM}$ and $I_{SM}$ , respectively. The normalized of $V_{DD}I_{DD}$ by $V_{SM}I_{SM}$ obtained the output power capability $c_p$ that is defined as

$$c_p = \frac{I_{DD}V_{DD}}{I_{SM}V_{SM}}, \tag{28}$$

The peak switch voltage $V_{SM}$ become manifest at the range of $\pi \le \theta < 2\pi$ , where the current through the nonlinear shunt capacitance is zero. Hence, we can rewrite (13) as

$$\frac{V_{SM}}{V_{DD}} = \frac{V_{bi}}{V_{DD}}\left\langle\left\{1 - \frac{1-m}{\omega C_{j0}V_{bi}}\left[I_{DD}(\theta_{\max} - \pi) - I_m\left(\cos(\theta_{\max} + \varphi) + \cos(\varphi)\right) - \frac{I_n}{n}\left(1 + \cos(n\theta_{\max})\right)\right]\right\}^{1/(1-m)} - 1\right\rangle. \tag{29}$$

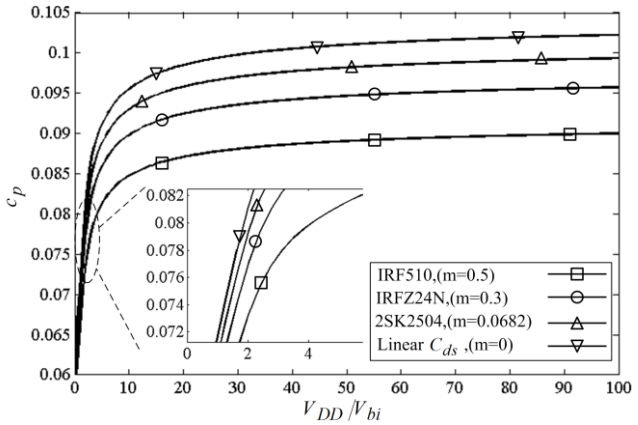


**FIGURE 6. The output power capability $c_p$ in terms of $V_{DD}/V_{bi}$ for different values of the grading coefficient m and linear drain-source capacitance.**

In (29), $\theta_{\max}$ is acquired by applying the differential function for the switch voltage waveform in (13) and equating the result to zero, which is expressed by

$$\left.\frac{dv_s}{d\theta}\right|_{\theta=\theta_{\max}} = \left(-2\omega C_{j0}R^{-1-\frac{m}{1-m}}n^2\pi(-8+n^2\pi^2)^{-2(1+\frac{m}{1-m})}\right)\times \left(V_{DD}\cos(\varphi)\right)$$
$$\left\langle \omega C_{j0}R\left(-8+n^2\pi^2\right)^2+2(-1+m)n^2\pi V_{DD}\cos(\varphi)\times \right.$$
$$\left[-\left(8+n^2\pi(5\pi-4\theta_{\max})+16\cos(n\theta_{\max})\right)\cos(\varphi)+\left(-8+n^2\pi^2\right)\cos(\theta_{\max}+\varphi)\right]\Big\rangle^{m/1-m}\times$$
$$\left[4n\cos(\varphi)\left(n\pi+4\sin(n\theta_{\max})\right)+\left(-8+n^2\pi^2\right)\sin(\theta_{\max}+\varphi)\right]. \quad (30)$$

The obtained analytical equation in (30) has no analytical solution for $m \neq 0$. This expression can be solved using numerically approaches. As can be concluded from (30), the peak switch voltage is expressed in terms of $\varphi$, $V_{DD}$, $V_{bi}$, $m$, and $\omega C_{j0}R$.

Figure 5 depicts plots of the normalized peak switch voltage in terms of $V_{DD}/V_{bi}$ for three types of MOSFETs and a linear drain-source capacitance using numerically solution of (29) with the values of $\theta_{max}$ that are obtained from (3). From Fig. 5, it seems that peak switch voltage is decreased with the decrement of the grading coefficient. This response is happened because the average value of the nonlinear capacitance in one-period of class-E inverter operation decreases with the increase in *m*.

The peak switch current $I_{SM}$ is the sum of dc-supply current $I_{DD}$, output current amplitude $I_m$, and $n^{th}$ harmonic current amplitude $I_n$. Hence, the peak switch current normalized with respect to the dc-supply voltage, i.e., $I_{SM}/I_{DD}$ can be obtained from (16) and (17) as

$$\frac{I_{SM}}{I_{DD}} = 1+\frac{I_m}{I_{DD}}+\frac{I_n}{I_{DD}} = 1+\frac{\pi}{2\cos(\varphi)}\left(1-\frac{8}{n^2\pi^2}\right)+\frac{4}{n\pi}. \quad (31)$$

By substituting (29) and (31) into (28), the output power capability $c_p$ is calculated as

$$c_p = \frac{V_{bi}}{V_{DD}}\left\langle\left\{1-\frac{1-m}{\omega C_{j0}V_{bi}}\left[I_{DD}(\theta_{\max}-\pi)-\right.\right.\right.$$
$$I_m\left(\cos(\theta_{\max}+\varphi)+\cos(\varphi)\right)-$$
$$\left.\left.\left.\frac{I_n}{n}\left(1+\cos(n\theta_{\max})\right)\right]\right\}^{1/(1-m)}-1\Big\rangle^{-1}\times$$
$$\left\langle 1+\frac{I_m}{I_{DD}}+\frac{I_n}{I_{DD}} = 1+\frac{\pi}{2\cos(\varphi)}\left(1-\frac{8}{n^2\pi^2}\right)+\frac{4}{n\pi}\right\rangle^{-1}. \quad (32)$$

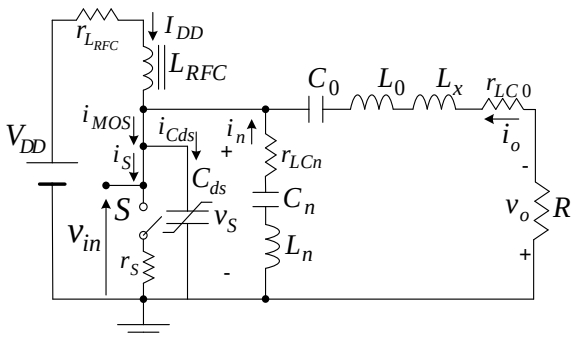


**FIGURE 7. The equivalent circuit model of the class-E/F$_n$ inverter by including ESRs of the switching device and passive elements.**

Figure 6 illustrates plots the output power capability in terms of $V_{DD}/V_{bi}$ for three types of MOSFETs with various grading coefficients and a linear drain-source capacitance. It can be stated from Fig. 6 that the output power capability $c_p$ for a linear capacitance is maximum while it decreased with the increment of the grading coefficient. Therefore, the peak switch voltage reaches to high values for large *m*. The output power capability reaches to zero with the decrement of the dc-supply voltage, which means that the peak switch voltage is infinite.

## V. Power-Conversion Efficiency Analysis

In a really implemented class-E inverter circuit, the major source of power losses is the parasitic resistances of both active and passive elements. Additionally, the parasitic resistances are assumed small enough to prevent from any distribution of the switching and output waveforms. Therefore, we propound the equivalent series resistance (ESR) of load network $r_{LC0}$, switch on-state resistance $r_s$, the dc-feed inductor $r_{L_{RFC}}$, series parallel resonant filter $r_{LC3}$, as depicted in Fig. 7. Moreover, the MOSFET gate-drain and drain-source parasitic capacitances have ESRs that

are much lower than other ESRs.

The power dissipation at $r_{L_{RFC}}$ is calculated as

$$P_{r_{L_{RFC}}} = \frac{1}{2\pi}\int_0^{2\pi} r_{L_{RFC}} I_{DD}^2 d\theta = r_{L_{RFC}} I_{DD}^2. \quad (33)$$

The power losses in the output load network is

$$P_{r_{LC}} = \frac{1}{2\pi}\int_0^{2\pi} r_{LC} i_o^2 d\theta = \frac{r_{LC} I_m^2}{2}. \quad (34)$$

Similarly, the power losses at the series parallel resonant filter $r_{LC3}$ is obtained as

$$P_{r_{LCn}} = \frac{1}{2\pi}\int_0^{2\pi} r_{LCn} i_n^2 d\theta = \frac{r_{LCn} I_n^2}{2}. \quad (35)$$

The ESR of the MOSFET in the switch on-state leads to power losses that can be calculated by

$$P_{rs} = \frac{1}{2\pi}\int_0^{2\pi} r_s i_s^2 d\theta = \frac{1}{2\pi}\int_0^{\pi} r_s (I_{DD} + i_o + i_n)^2 d\theta, \quad (36)$$

From (33)-(36), the power conversion efficiency $\eta$ is calculated as

$$\eta = \frac{P_o}{P_o + P_{r_{L_{RFC}}} + P_{r_{LC}} + P_{rs}}. \quad (37)$$

The analytical expression for power losses and power conversion efficiency are shown in Appendix, where the power conversion efficiency is specified with an accurate analytical expression in terms of the ratio of ESRs for the series load network, the dc-feed inductor and the MOSFET on-state resistance to the load resistance.

## VI. Circuit Design Examples and Results Confirmations

### A. Design Specifications

In this section, a design example of the class-E/$F_3$ inverter is given. The shunt capacitance with the MOSFET device is only the nonlinear drain-source parasitic capacitance. The required shunt capacitance can be adjusted only using the grading coefficient *m* of the MOSFET body junction diode without any external auxiliary circuit. The satisfaction of both the peak switch voltage and the dc-supply voltage for the class-E/$F_3$ inverter can be done easily by tuning of the grading coefficient *m* as an adjustment parameter.

The given design specifications are dc-supply voltage $V_{DD}$=20 V, peak switch voltage $V_{SM}$ =80 V, operating frequency *f*=4 MHz, output power $P_o$= 7.2 W, load resistance *R*=13.2 Ω, and loaded-quality factor *Q*=10. From these design specifications, we have $V_{SM}/V_{DD} = 4$ and $P_o R/V_{DD}^2 = 0.2376$.

Figure 8 depicts plots $V_{SM}/V_{DD}$ in terms of $P_o R/V_{DD}^2$ for three types of the MOSFETs with different grading coefficient *m* and the linear shunt capacitance *m*=0. It can be reported

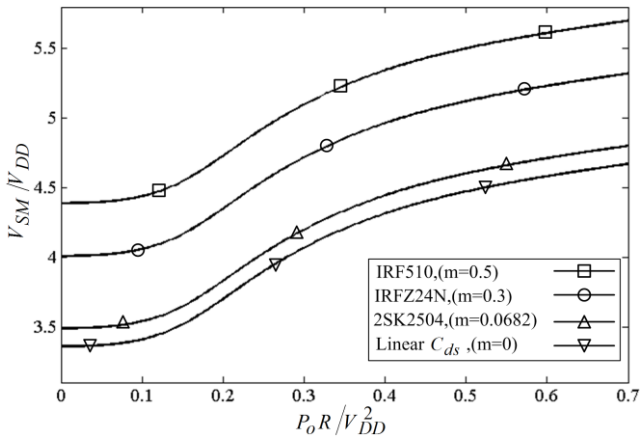


**FIGURE 8. The normalized peaks switch voltage in terms of $P_o R/V_{DD}^2$ for different values of the grading coefficient m and linear drain- source capacitance.**

from Fig. 8 that the grading coefficient *m* can be effectively used as a modification variable to tune in the given output power according to the permissible peak switch voltage simultaneously. Therefore, this main restriction area for implementing of class-E/$F_3$ inverter is solved without any external auxiliary circuit.

Based on the design specifications, there are exist three possible values for $V_{SM}/V_{DD}$ with three different grading coefficient *m*, as it can be concluded from Fig. 8. The obtained peak switch voltage for three types of MOSFETs such as IRF510, IRFZ24N, and 2SK2504 are 97.52 V, 89.92 V and 79.52 V, respectively. On the other hand, the breakdown drain-source voltage of the IRF510, IRFZ24N and 2SK2504 are 100 V, 55 V and 100 V, respectively. Therefore, only the 2SK2504 MOSFET with the grading coefficient *m*=0.0682 satisfied the given output power and the peak switch voltage of the MOSFET simultaneously.

The peak switch voltage for the design specification is 20 % lower than the breakdown drain-source voltage of 2SK2504 MOSFET. Therefore, it is approved that the 2SK2504 MOSFET can operate safely for the given design specifications from the MOSFET breakdown voltage point of view that is satisfied the obtained grading coefficient *m*.

### B. Circuit Implementation Results Discussions

From (4), *L* is obtained as

$$L = \frac{QR}{\omega} = 5.25\,\mu\text{H}. \quad (38)$$

From (27) and (38), $L_0$ is

$$L_0 = L - L_x = \frac{R}{\omega}\left[Q - \tan(\varphi_1 - \varphi)\right] = 5.12\,\mu\text{H}. \quad (39)$$

From the resonant condition of $L_0$-$C_0$ in figure 2 and (39), the resonant capacitance $C_0$ is obtained as

$$C_0 = \frac{1}{\omega^2 L_0} = 309.2\,\text{pF}. \quad (40)$$

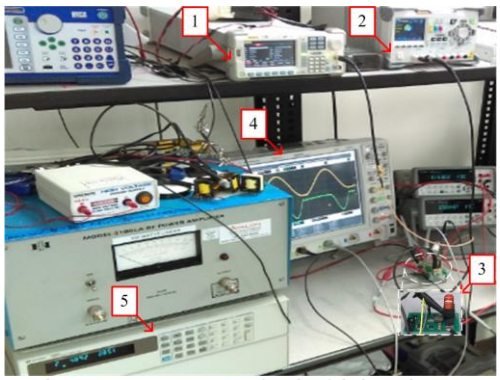


**FIGURE 9. The measurement setup for the fabricated proposed class-E/F3 inverter. (1) Signal generator. (2) dc-supply voltage. (3) Implemented circuit under test. (4) Oscilloscope. (5) Electronic-load.**

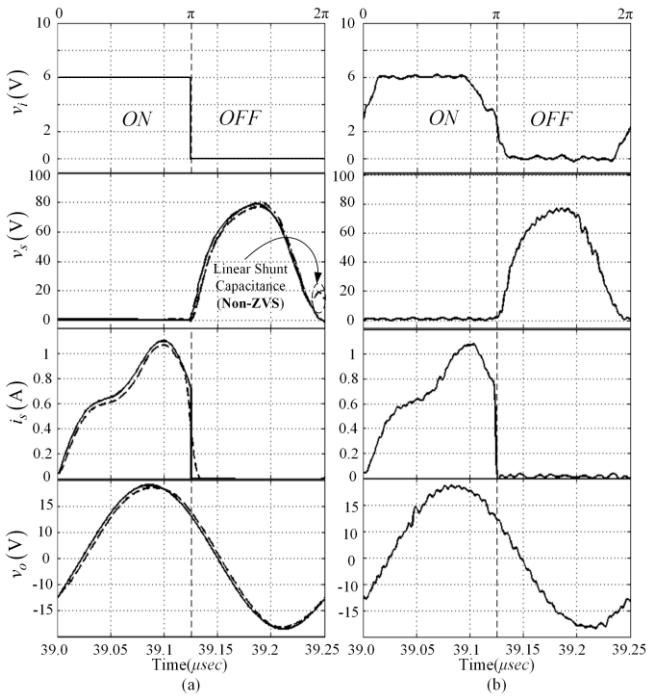


**FIGURE 10. The input, switching voltage, switching current and output waveforms for the proposed class-E/F3 inverter. (a) Theoretical expressions (solid-line), PSpice simulations (dash-line), Theoretical for only Linear Shunt Capacitance (dot –dash-line). (b) Circuit experiment.**

The dc-feed inductance $L_{RFC}$ when the current ripple ratio is less than 0.1 is given as [33]

$$L_{RFC} = 2\left(\frac{\pi^2}{4}+1\right)\frac{R}{f} \approx \frac{7R}{f} = 22.88\,\mu\text{H}. \tag{41}$$

The validation of obtained analytical expressions for the design of the class-E/$F_3$ inverter using 2SK2504 MOSFET as switching device and extracted elements values are done by performing PSpice simulations and experimental measurements. The experimental setup for the fabricated circuit prototype of the proposed class-E/$F_3$ inverter is illustrated in Fig. 9. The extracted design elements values of the proposed inverter are presented in Table II.

TABLE II
THEORETICAL, SIMULATIONS, AND EXPERIMENTAL MEASUREMENTS FOR THE CLASS-E/$F_3$ INVERTER EXAMPLE

| | *Theoretical* | *Simulated* | *Measured* | *Difference* |
|---|---|---|---|---|
| $R$ (Ω) | 13.2 | 13.2 | 13.1 | 0.75 % |
| $D$ | 0.5 | 0.5 | 0.5 | 0.00 % |
| $V_{DD}$ (V) | 20 | 20 | 20.0 | 0.00 % |
| $f$ (MHz) | 4.0 | 4.0 | 4.0 | 0.00 % |
| $V_{SM}$ (V) | 80 | 80 | 79.1 | 1.12 % |
| $I_{DD}$ (A) | 0.36 | 0.36 | 0.35 | 2.77 % |
| $L$ (μH) | 5.25 | 5.1 | 5.0 | 1.96 % |
| $C_0$ (pF) | 309.2 | 308.1 | 306.3 | 0.58 % |
| $L_{RFC}$ (μH) | 22.88 | 22.88 | 22.6 | 0.87 % |
| $L_n$ (μH) | 11.2 | 11.2 | 11.1 | 0.89 % |
| $C_n$ (pF) | 620 | 620 | 610 | 1.61 % |
| $r_s$ (Ω) | 0.1 | 0.1 | 0.1 | -0.00 % |
| $r_{LRFC}$ (Ω) | 0.16 | 0.16 | 0.1 | – |
| $r_{LC0}$ (Ω) | 0.12 | 0.12 | – | – |
| $r_{LC3}$ (Ω) | 0.22 | 0.22 | | |
| $P_{rLRFC}$ (mW) | 77.5 | 78.4 | – | – |
| $P_{rLC}$ (W) | 0.12 | 0.1 | – | – |
| $P_{rLC3}$ (W) | 0.14 | 0.1 | | |
| $P_o$ (W) | 7.2 | 7.3 | 7. 1 | 2.7 % |
| $P_{in}$ (mW) | – | – | 28.3 | – |
| $G$ (dB) | – | – | 55.2 | – |
| *THD* | 0.00 % | 7.3 % | 10.3 % | – |
| $\eta$ | 93.1 % | 92.8 % | 91.6 % | 1.29 % |

Figure 10 shows the extracted waveforms from theoretical analysis, PSpice simulations, and laboratory measurements for the proposed class-E/$F_3$ inverter circuit example, which proved the effectiveness of the analytical design expressions. The measurements of parasitic resistances for all passive elements are performed using an LCR meter of HP4284A. Furthermore, the ESR of the dc-feed inductor is measured at dc by following the experimental measurement procedure in [34]. Moreover, the switch-on state resistance $r_s = 0.1\Omega$ is obtained from the 2SK2504 PSpice model [32]. The PSpice-simulation and the theoretical predictions along with the measurement outcomes for the circuit design example are summarized in Table II. It is seen from figure 10 that the peak switch voltage is 76.6 V. The measured output power is 7.1 W. A 4 MHz input square waveform using the function generator Stanford Research DS345 is generated with the amplitude of 6 V and 0 V offset. A 34401A Digital Multimeter is applied to do the measurement of the voltage and current for the designed class-E/$F_3$ inverter. The Textronix TDS3014B and the TCP202 current probes are employed to acquire the waveform data of the output voltage and the current, respectively.

The output power $P_o$ of all harmonics is extracted from the sum of powers at all harmonics in both simulations and experiments activities. The power gain is defined as

$$G = 10\log_{10}\left(\frac{P_o}{P_{in}}\right), \tag{42}$$

where $P_{in}$ and $P_{out}$ are the input and output power, respectively. Moreover, the total harmonic distortion (THD) is obtained by

$$\text{THD}=\frac{\sqrt{\sum_{n=2}^{\infty}V_{on}^2}}{V_{o1}}, \tag{43}$$

where $V_{on}$ is a root-mean-square value of the $n^{\text{th}}$ harmonic in the output voltage $v_o$.

It is seen from Fig. 10 that the ZVS/ZDVS conditions are obtained at 4 MHz. On the other hand, theoretical result of the class-E/$F_3$ inverter with only linear shunt capacitance shows that ZVS cannot be archived. This important effect proved the vital role of the accurate tuning of the MOSFET nonlinear drain-source capacitance. As a result, for the inverter design example, the measured power conversion efficiency $\eta$ is 91.6 % with the output power 7.1-W. It can be concluded from these results that it is important and effective approach to consider the nonlinearity of the MOSFET drain-source capacitance along with the grading coefficient $m$ as an adjustment parameter for designing of a class-E/$F_3$ inverter with a given output power and peak switch voltage.

## VII. CONCLUSION

The analytical expressions for satisfying of the class-E ZVS/ZDVS conditions in the class-E/$F_3$ inverter with the MOSFET nonlinear drain-source parasitic capacitance at any grading coefficient $m$ and 50% duty ratio is presented. The effective impacts of the grading coefficient $m$ with a proper selection procedure are proved on both switching waveforms and element designs equations. These degrees of the nonlinearity shunt capacitance used as an adjustment parameter to satisfy the peak switch voltage and output power simultaneously. An accurate model is proposed to predict the output power capability and power conversion efficiency based on the grading coefficient $m$. A prototype class-E/$F_3$ inverter circuit example using a MOSFET with $m$=0.0682is presented with the output power 7.1-W and obtained power conversion efficiency 91.6 %.

## APPENDIX

In this section, the derivation of analytically expression for power losses and power conversion efficiency are shown.

$$P_{r_{L_{RFC}}}=\frac{1}{2\pi}\int_0^{2\pi}r_{L_{RFC}}I_{DD}^2\,d\theta=r_{L_{RFC}}I_{DD}^2$$
$$=\left(\frac{V_{DD}}{R}\right)^2\frac{4r_{L_{RFC}}}{\left[\frac{\pi}{2\cos(\varphi)}\left(1-\frac{8}{n^2\pi^2}\right)\right]^4}. \tag{44}$$

$$P_{r_{LC}}=\frac{1}{2\pi}\int_0^{2\pi}r_{LC}\,i_o^2\,d\theta=\frac{r_{LC}I_m^2}{2}=\left(\frac{V_{DD}}{R}\right)^2\frac{2r_{LC}\cos^2(\varphi)}{\pi^2\left(1-\frac{8}{n^2\pi^2}\right)^2}. \tag{45}$$

$$P_{r_{LCn}}=\frac{1}{2\pi}\int_0^{2\pi}r_{LCn}\,i_n^2\,d\theta=\frac{r_{LCn}I_n^2}{2}$$
$$=\left(\frac{4}{n\pi}\right)^2\left(\frac{V_{DD}}{R}\right)^2\frac{2r_{LCn}}{\left[\frac{\pi}{2\cos(\varphi)}\left(1-\frac{8}{n^2\pi^2}\right)\right]^4}. \tag{46}$$

$$P_{rs}=\frac{1}{2\pi}\int_0^{2\pi}r_s\,i_s^2\,d\theta=\frac{1}{2\pi}\int_0^{\pi}r_s\,(I_{DD}+i_o+i_n)^2\,d\theta$$
$$=\left(\frac{V_{DD}}{R}\right)^2\frac{r_s}{2\pi\left(-1+n^2\right)\left[\frac{\pi}{2\cos(\varphi)}\left(1-\frac{8}{n^2\pi^2}\right)\right]^4}\times$$
$$\left\langle -4n\pi\left(1-\frac{8}{n^2\pi^2}\right)\left(2-2n^2+\frac{4}{n\pi}\sin(n\pi)\right)+\right.$$
$$(-1+n^2)\left[\frac{32}{n\pi}+2\left(2+\frac{\pi^2}{4\cos^2(\varphi)}\left(1-\frac{8}{n^2\pi^2}\right)^2+\left(\frac{4}{n\pi}\right)^2\right)n\pi\right.$$
$$\left.\left.-\frac{8}{n\pi}\cos(n\pi)\left(4+\frac{4}{n\pi}\sin(n\pi)\right)\right]+\right.$$
$$\left.\left(\frac{8\pi}{\cos(\varphi)}\left(1-\frac{8}{n^2\pi^2}\right)\right)\left(\frac{4}{n\pi}\right)n^2\cos^2\left(\frac{n\pi}{2}\right)\sin(\varphi)\right\rangle. \tag{47}$$

$$\eta=\frac{P_o}{P_o+P_{r_{L_{RFC}}}+P_{r_{LC}}+P_{rs}}$$

$$= \left\{ 1 + \frac{2r_{L_{RFC}}}{R}\sin^2(\varphi) + \frac{r_{LC}}{R} + \frac{r_{LCn}}{R}\frac{16}{n^2\pi^2\sin^2(\varphi)} + \frac{r_s}{R}\frac{1}{2\pi\left(-1+n^2\right)\left[\frac{\pi}{2\cos(\varphi)}\left(1-\frac{8}{n^2\pi^2}\right)\right]^2} \times \left\langle -4n\pi\left(1-\frac{8}{n^2\pi^2}\right) \times \left(2-2n^2+\frac{4}{n\pi}\sin(n\pi)\right) + (-1+n^2) \times \left[\frac{32}{n\pi} + 2\left(2+\frac{\pi^2}{4\cos^2(\varphi)}\left(1-\frac{8}{n^2\pi^2}\right)^2 + \left(\frac{4}{n\pi}\right)^2\right)n\pi - \frac{8}{n\pi}\cos(n\pi)\left(4+\frac{4}{n\pi}\sin(n\pi)\right)\right] + \left(\frac{8\pi}{\cos(\varphi)}\left(1-\frac{8}{n^2\pi^2}\right)\right)\left(\frac{4}{n\pi}\right)n^2\cos^2\left(\frac{n\pi}{2}\right)\sin(\varphi)\right\rangle \right\}^{-1}. \quad (48)$$

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