Development of a Prototype Solid-State Fault-Current Limiting and Interrupting Device for Low-Voltage Distribution Networks

M. M. R. Ahmed, *Member, IEEE*, Ghanim Putrus, Li Ran, *Member, IEEE*, and Roger Penlington

***Abstract*—This paper describes the development of a solid-state fault current limiting and interrupting device (FCLID) suitable for low-voltage distribution networks. The main components of the FCLID are a bidirectional semiconductor switch that can disrupt the short-circuit current, and a voltage clamping element that helps to control the current and absorb the inductive energy stored in the network during current interruption. Using a hysteresis-type control algorithm, the short-circuit current can be constrained according to a predefined profile. Insulated-gate bipolar transistors and diodes are used to construct the semiconductor switch. Varistors are used as the voltage clamping element. An effective method is adopted to improve the current sharing between parallel varistors in order to provide the required capability of energy absorption. An overall protection scheme for the FCLID is described. A prototype FCLID for 230-V single-phase, or 400-V three-phase, applications is developed and tested. Analyses and experiments are carried out to define the stresses that the main components in the FCLID are subject to. The results show that the developed prototype is capable of limiting a 3-kA prospective short-circuit current to 120 A for a period of 0.8 s, without exceeding the thermal limits of the chosen switches and varistors.**

***Index Terms*—Current limiter, electrical power distribution, fault current, semiconductor switch, varistor.**

I. Introduction

THERE is a growing interest in the development and utilization of fault-current limiters in electrical distribution networks. This arises from the need to deal with the ever-increasing short-circuit level in power systems and to constrain the stresses on the transformers, circuit breakers, feeder cables, and embedded generators during short-circuit faults. This can also be attributed to the concern over power quality as fault current limiters can be used to mitigate voltage sags caused by faults [1]. Fault-current limiters are needed to provide a limited, but sustained short-circuit current through the fault for a sufficient time (for example, 1 s) to enable proper coordination of protective relays. In some cases, they may also be used to maintain sustained short-circuit current through a cable that has developed an intermittent fault to enable fault location.

Several devices to limit the fault current have been developed including electronically controlled fuses, tuned LC circuits, thyristor-controlled series reactors, solid-state fault-current limiters based on resistors/inductors switched by gate turn-off thyristors (GTOs), and superconducting fault-current limiters [1]–[6]. Some of these devices, such as the electronically controlled fuses, are of a single shot design. Following an operation, the supply to the load is lost until the device is replaced. Other devices such as tuned LC circuits and those which limit the fault current by inserting a fixed impedance in the circuit are usually sensitive to the network condition (e.g., the short-circuit level) and fault location [2]–[6]. Fast current interrupting devices, such as fuses or solid-state circuit breakers, are only useful for certain applications, such as the bus-tie location or for the protection of single loads. These devices can interrupt the current almost instantaneously, but are not able to sustain its flow for a sufficient time [7] which is required for protection coordination with relays in the overall protection scheme [8]. Superconducting fault-current limiters often have a slow recovery time, which makes them difficult to use if the protected power circuit requires autoreclosure [9].

Despite the successes of previous devices in many targeted applications, there is still the need for new devices of better usability and controllability while remaining affordable. A single device that integrates the two functions of fault-current limiting and interrupting would be desirable in order to reduce the overall switchgear cost [6].

The practical success of a fault-current limiter relies on its design with respect to the intended application. In general, a fault-current limiter is desired to have the following performance characteristics:

- low or zero impedance during normal operation;
- high and controllable impedance during faults;
- fast transition from normal conducting to current-limiting modes without causing excessive voltage spikes;
- fast recovery after fault interruption (necessary for applications that require autoreclosure);
- no adverse effects on the selectivity of the overall protection scheme (allow protection coordination);
- high reliability and fail-safe operation;
- low cost with minimum maintenance requirements;
- capability to tolerate and ride through currents associated with normal overload, transformer inrush current, motor starting and energizing a capacitor bank.

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This paper presents the development of a new device which combines the two functions of limiting and interrupting the short-circuit current. This device is thus called a fault-current limiting and interrupting device (FCLID). The device is expected to limit the short-circuit current and maintain it for a considerable period of time which is necessary for protection coordination. The current may be eventually interrupted by the device itself if other protective relays in the system fail to clear the fault. For the reasons to become clearer later in this paper, this presents serious challenges, particularly on the energy handling capability of the main components used and the protection of the FCLID itself. Such issues are analyzed in this study and solutions are suggested to satisfy the requirements. A prototype FCLID is developed using the knowledge obtained. The study serves as a stepping stone for developing FCLIDs of higher voltage and current ratings.

In the project, the authors have generically investigated several aspects including the switch topologies [10], the energy handling capability of the varistors used [11], as well as the transient harmonic requirements of the distribution network [12]. This paper aims to describe the overall design of the FCLID prototype including the component selection, control parameters, and the protection of its devices. Section II reviews the operating principles and characteristics of the proposed FCLID. Section III analyzes the factors affecting the thermal stress on the main components of the FCLID. The control parameters and component ratings of the FCLID are then determined in Section IV. Section V presents a protection scheme for the FCLID when used in practical applications where uncertainty of the distribution network is inevitable. Experimental test results of the prototyped FCLID are presented in Section VI.

II. Fault Current Limiting and Interrupting Device

The configuration of the FCLID incorporated in a single-phase distribution network is shown in Fig. 1. It consists of a fast acting, bidirectional switch realized using power semiconductor devices [insulated-gate bipolar transistors (IGBTs) and diodes as shown in the figure], a varistor (nonlinear resistor), and a snubber circuit, all connected in parallel.

There are alternative ways to construct the switch [7], [13]. The topology shown in Fig. 1 was chosen after considering the conduction and switching losses and transients associated with the reverse recovery current of the diodes.

During normal operation of the power network, the IGBTs in the synthesized switch are always gated on. Since the IGBTs conduct permanently during this steady-state period, there will be an associated onstate power loss which accounts for about 1% of the rated load power. In order to reduce this loss, the FCLID may be bypassed using, for example, a vacuum circuit breaker (VCB), as shown in the dashed lines in Fig. 1. The VCB opens on detecting a short-circuit fault in the downstream power network. The VCB controller may be designed such that it ensures that before opening, the fault level is within the FCLID capability. Otherwise, the VCB remains closed and the fault is dealt with by upstream protective devices—for example, a fuse.

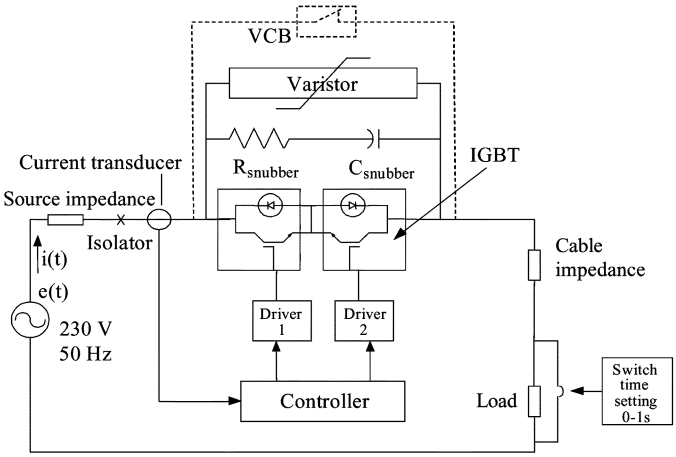

Fig. 1. Schematic diagram of the FCLID.

The semiconductor device (IGBT) initially conducts the fault current until it reaches a preset value $(I_{\max})$ at which instant it is turned off. The fault current is thus diverted to the snubber circuit and varistor. The snubber circuit helps to damp the high *dv/dt* that appears during the initial stage of the IGBT turn-off process. During this stage, the snubber capacitor is charged (and, hence, becomes inactive) and the varistor current starts to build up rapidly. The clamping voltage of the varistor is set higher than the peak supply voltage. Therefore, the current in the circuit will start to decrease when this voltage is reached, following an $R-L$ decay (1) as the source voltage can be considered constant in the relatively short interval within a switching cycle. The semiconductor switch is turned on again to re-establish the current when it reduces to a preset low value $(I_{\min})$. The current will again follow the trajectory of an $R-L$ circuit, as given by (2). The current response in the circuit when the switch is turned on and turned off is shown in Fig. 2. The varistor voltage is almost constant when the varistor is in the clamping state

$$i(t) = I_{\min} + \left[\frac{e(t)}{R} - I_{\min}\right][1 - e^{-(t-t_1)/RL}] \tag{1}$$

$$i(t) = I_{\max} + \left[\frac{e(t) - V_{\text{clamp}}}{R} - I_{\max}\right][1 - e^{-(t-t_2)/RL}]. \tag{2}$$

In the above equations, R and L are the total series resistance and inductance in the circuit, and V_{clamp} is the varistor clamping voltage. Times t_1 and t_2 denote the instants when the controlled switch is gated on or off, respectively.

The switching logic is the same for both the positive and negative half cycles of the limited short-circuit current and the operation is sustained until the fault is cleared by a downstream relay or for a preset period of time that is desired by the application and permitted by the capability of the FCLID. The latter case is considered in this work, where the limited fault current is interrupted when the switch in the FCLID is permanently gated off at $\mathrm{t} = 0.08$ s, as shown in Fig. 2. The fault can then be isolated using an isolator which does not need to have a high breaking duty.

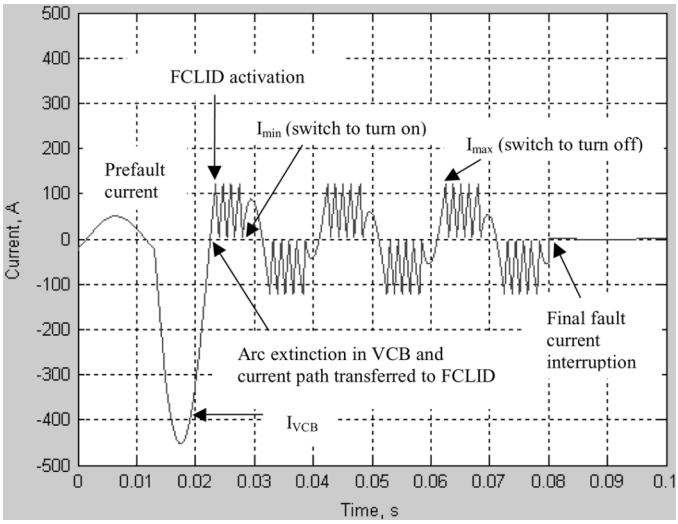

Fig. 2. Current response of the FCLID.

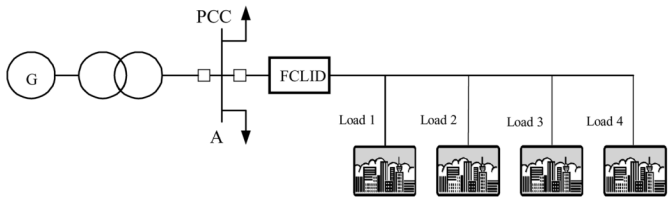

Fig. 3. FCLID installed in a typical distribution network.

Fig. 3 shows a possible way of installing the FCLID in a typical low-voltage (230/400 V) three-phase distribution feeder. Busbar A is the point of common coupling (PCC) with other cable feeders. Without the fault current limiter, the prospective peak short-circuit current at the PCC is typically about 25 kA and the maximum load current is about 400 A in total. The fault current reduces along the feeder length with the lowest value (which depends on the feeder impedance) being at the far end of the feeder. As the purpose of this project is to prove the concept of the FCLID, a single-phase prototype with reduced current ratings was developed. Without the FCLID, the prospective peak short-circuit currents at Load 1, Load 2, Load 3, and Load 4 were assumed as 3, 2.5, 1.7, and 1 kA, respectively. The normal load current is assumed to be less than 50 A. Thus, the value of $I_{\max}$ of the prototype FCLID is set at 120 A which is sufficiently higher than the peak value of the rated load current $\sqrt{2} \times 50$ A. This means that the maximum limited short-circuit current in the feeder is 120 A. The supply X/R ratio is set to 5, $I_{\min} = 0$ A and intended current limiting time $= 0.8$ s.

A feature of the developed FCLID is that, disregarding the location of the fault or supply system condition, the general profile of the limited current is determined by $I_{\max}$ and $I_{\min}$. Furthermore, $I_{\max}$ and $I_{\min}$ can be adjusted in a subcycle time scale to control the harmonic content of the current [14].

In addition to the controllability over the profile of the limited short-circuit current, the following features of the developed FCLID can also be expected based on the above description of its operating principles.

1) The device inherently integrates the two functions of fault-current limiting and interrupting.
2) The current limiting function is achieved via the insertion of a varistor. The varistor needs to absorb the stored energy associated with the inductive current in the circuit. The power dissipation in the varistor needs to be carefully considered so that the FCLID can operate for the targeted period of time.
3) During the operation of the FCLID, the rate of change of current is determined by the total series inductance in the circuit, which depends on the supply system condition and fault location. Therefore, these factors will affect the switching frequency of the FCLID and, hence, switching power losses in the semiconductor devices.
4) The varistor presents its clamping voltage to the rest of the circuit when conducting but the supply source voltage is time variant. Therefore, the switching frequency is not constant even within a half fundamental cycle, which will further affect the power loss profile.

In some damp and/or contaminated environments (such as costal areas), intermittent faults in distribution networks' cables can occur quite frequently [15]. One planned application of the developed FCLID is to provide a sustained current in such cables for a period long enough to "burn" the intermittent fault into a permanent one and, hence, assist in identifying the fault location. It is expected that this will reduce the number of call-outs that the network operator will receive. This highlights the importance of the FCLID in providing a limited but sustained short-circuit current.

III. Effects of Operating Conditions and Control Parameters

Analytical calculations and numerical simulations in the time domain are used to guide the design of the FCLID. Internal variables of the device have been examined under different operating conditions. To simplify the calculations, the analytical method is based on approximations, such as those made in deriving (1) and (2). The results of analytical calculation provide valuable insight to help identify the important factors that affect the design choices. Numerical simulation is based on more detailed representation of the system conditions and component characteristics. The results from the simulation are used to determine the required ratings of the components.

Fig. 4 shows the relationship between the energy to be absorbed by the varistor per 20 ms (based on a constant rate) during current limiting operation and the short-circuit current level of the supply system as measured at the fault location. The results of Fig. 4 show that the energy dissipation rate of the varistor is nearly constant irrespective of the short-circuit level. More details about the mechanism giving rise to the power dissipation in the varistor are given in [11].

The effect of the system short-circuit current level on the average switching frequency of the FCLID is shown in Fig. 5. As the short-circuit level increases, the semiconductor switching frequency and, hence, the switching losses increase proportionally. Therefore, the FCLID controller need to be designed such that it inhibits the FCLID operation whenever the short-circuit level is above its rating.

It can be deduced from the result shown in Fig. 2 that as $I_{\min}$ increases, the shape of the current waveform improves and

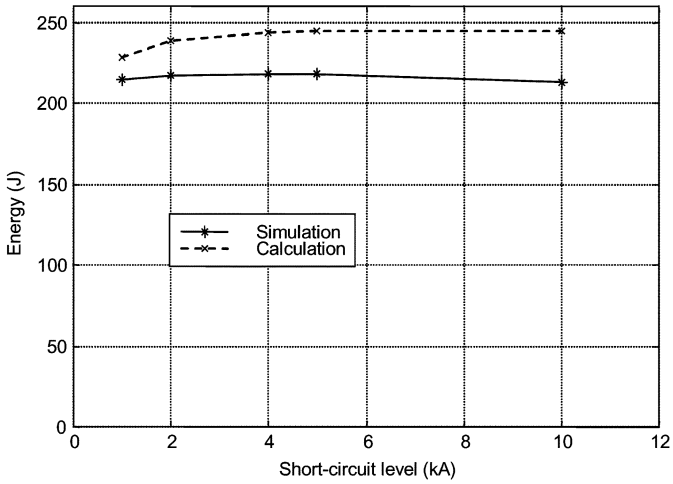

Fig. 4. Varistor energy dissipation as affected by the short-circuit level.

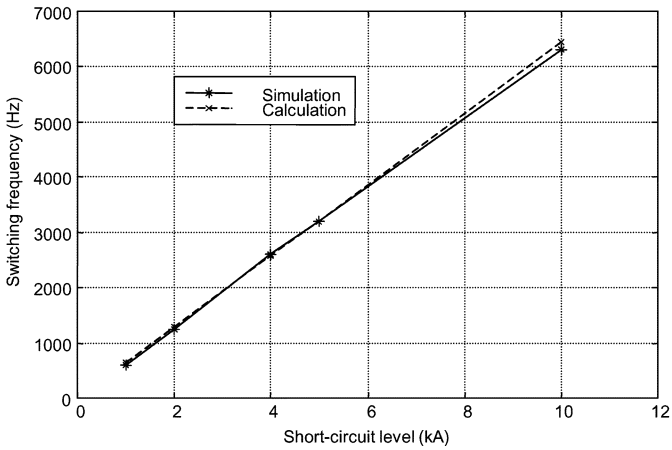

Fig. 5. Relationship between switching frequency and short-circuit level.

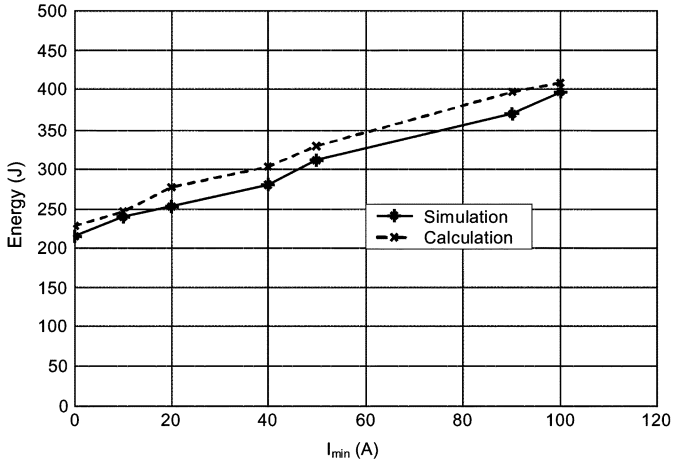

Fig. 6. Relationship between varistor energy dissipation and $I_{\min}$.

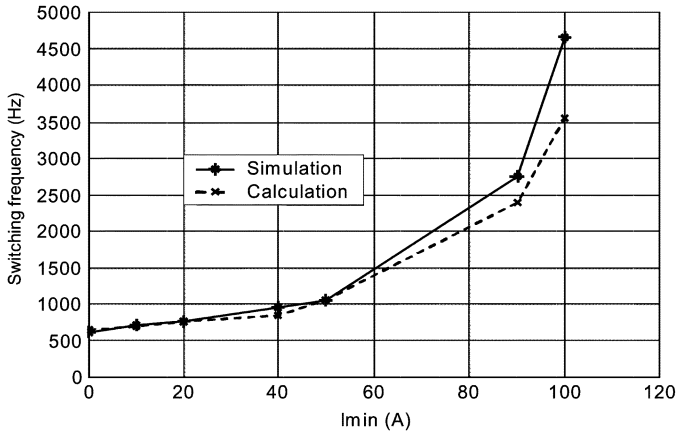

Fig. 7. Relationship between switching frequency and $I_{\min}$.

better resembles a sine wave [12]. This reduces the low-order harmonic content in the system current at the expense of increasing the high-frequency components which are generally easier to deal with. However, both the switching losses and the varistor energy dissipation will increase, as shown in Figs. 6 and 7. Fig. 6 shows the varistor energy dissipation (per 20 ms) as affected by $I_{\min}$ when $I_{\max}$ is fixed at 120 A. As $I_{\min}$ increases to reduce the current tolerance band, the average varistor current increases and so does its energy dissipation. Fig. 7 shows that the average switching frequency of the FCLID also increases dramatically with $I_{\min}$ as implied by (1) and (2). Therefore, in practice, $I_{\min}$ is to be set adequately low (relative to $I_{\max}$) in order to avoid excessive stresses on the semiconductor switch and the varistor.

IV. Design of the Prototype FCLID

The objective of this project is to design and build a single-phase 230-V FCLID prototype with specifications as described in Section II. These specifications have been determined just for this study, as a "proof of concept" to demonstrate the principles of the FCLID. As explained in Section II, the presence of the VCB shown in Fig. 2 is not essential for the operation of the FCLID. The VCB may be added if it becomes necessary to avoid the IGBT onstate power loss during system normal operation. Therefore, to simplify the design of the prototype, it was assumed that the FCLID is not bypassed by a VCB and that the bidirectional switch in the FCLID is constantly gated on before fault occurrence.

In the design of the FCLID prototype, the following major aspects are the main considerations.

A. Interruption Time

The interruption time is the time from the moment when the instantaneous value of the network current exceeds a threshold preset value (after fault occurrence) to the first interruption of the fault current by the semiconductor switch in the FCLID. This time consists of the detection time, switch triggering time, and switch turn-off time. If the interruption time is too long, due to, for instance, a slow response of the measuring and control components, then the actual current (at the moment of interruption) may be more than that which the semiconductor switch can safely interrupt. For the short-circuit levels and dc offset anticipated in practice, it has been determined in this study that the interruption time should be no more than 10 μs to prevent malfunction of or damage to the FCLID [10]. The response time of a Hall effect current transducer is less than 500 ns and the IGBT

turn-on and turn-off times are normally less than 1 μs. Therefore, the total interruption time can be practically kept within 2μs including all controller delays.

If the FCLID is initially bypassed by a VCB, the interruption time is extended correspondingly to include the response time of the VCB. Thus, the FCLID operation starts after the VCB operation and subsequent extinction of the arc.

B. Selection of the Switching Element

The bidirectional semiconductor switch must satisfy a set of requirements and there are several alternative components available which could deliver the desired performance. The technical aspects to be considered are

- rated voltage;
- maximum controllable current (the maximum pulsating current for the switch);
- turn on and turn off times;
- switching frequency and switching losses;
- maximum acceptable junction temperature;
- gate driver circuit.

For high-voltage and current applications, the GTO has been the dominant choice for a fully controllable semiconductor switch due to its large current and offstate voltage capabilities. However, it has a limited switching frequency and high switching losses and requires a complex gate drive circuit. Compared with the GTO, the integrated gate-commutated thyristor (IGCT) has the advantages of lower losses per rated kilovolt-amperes, faster switching, and higher reliability. The IGCT is not used in this work because the developed prototype is designed for low-voltage applications. IGBTs have become popular in low- and medium-voltage applications. With the introduction of the high-voltage IGBT and IGCT, they present a challenge to the dominance of the aging GTO. A 1200-V, 300-A (pulsating current) IGBT has been chosen for developing the FCLID in this study because it better meets the requirements listed above. Voltage and current margins are provided. The varistor inherently prevents any transient overvoltages from developing across the IGBT. Without the varistor, transient overvoltages can appear across the IGBT during current interruption as a result of the energy stored in the network inductance ($v = \mathrm{L}\, di/dt$). It should be noted that during the short-circuit period, the network is normally highly inductive.

In order to define the maximum operation time of the FCLID, the junction temperature of the selected IGBT has been evaluated for the operating conditions anticipated in practice. Fig. 8 shows the junction temperature of the IGBT with different system short-circuit current levels (I_{sc}). It is assumed that the FCLID starts to limit the current from $t = 0$ s and the control strategy is the same as stated before, $I_{\max} = 120$ A and $I_{\min} = 0$ A. The initial junction temperature of the IGBT is assumed to be 40 °C and the rated maximum junction temperature is 125 °C. The transient thermal impedance [16] of the selected IGBT stabilizes after about 0.2 s, after which time, the increase in the junction temperature is not significant. Further calculations confirmed that the IGBT, of appropriate current rating, could work safely for a period of up to 2 s even with I_{sc} =10 kA.

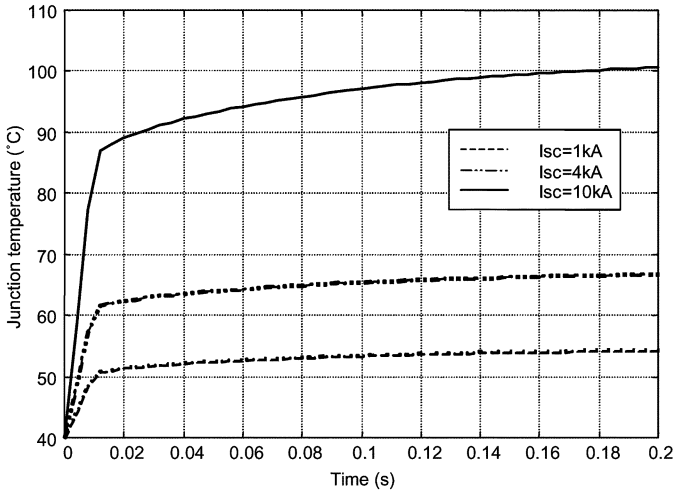

Fig. 8. IGBT junction temperature.

C. Selection of the Varistor

Metal–oxide varistors (MOV) are normally n-type ZnO-based ceramic semiconductor devices. They show a highly nonlinear current-voltage (I–V) characteristic similar to that of a back-to-back Zener diode pair (ignoring the forward conduction). Selection of the varistor for the FCLID is a three step process.

Step 1) defining the necessary steady-state voltage profile during the FCLID operation;
Step 2) selecting a type of varistor to provide the required voltage clamping characteristic;
Step 3) evaluating the energy absorption requirement of the varistor during the FCLID operation.

The most critical aspect required for the correct specification of the varistor in the FCLID is the energy to be absorbed by the device. The energy handling capability of the varistor is defined as the amount of energy that the varistor is required to absorb without any failure or damage. In order for the varistor to operate safely, it should be able to absorb this energy before its temperature rises to a damaging level as this would cause a short circuit through the varistor. The energy rating of a varistor is usually specified in a manufacturer's data sheet for a single shot operation. However, these data do not specify whether the varistor is suitable for repetitive energy absorption, as is the case during the FCLID operation. Therefore, an experimental study on the energy handling capability was performed which revealed that when the varistor is subjected to continuous repetitive pulses, it can handle a total energy about 50% higher than the rating for a single pulse (specified in the manufacturer's data sheet) [11]. The total energy can be calculated from the rate (per 20 ms) shown in Fig. 4 and the time of operation. This gives energy dissipation in each varistor used in the proposed prototype of about 1200 J for a 0.8-s period of the FCLID operation. The energy per pulse rating, as specified in the data sheet of the selected varistor, is 880 J [17].

The energy rating required by the FCLID can be, as in the present case, higher than that provided by a single varistor. In order to achieve the required energy absorption, this study proposes to operate multiple varistors in parallel. However,

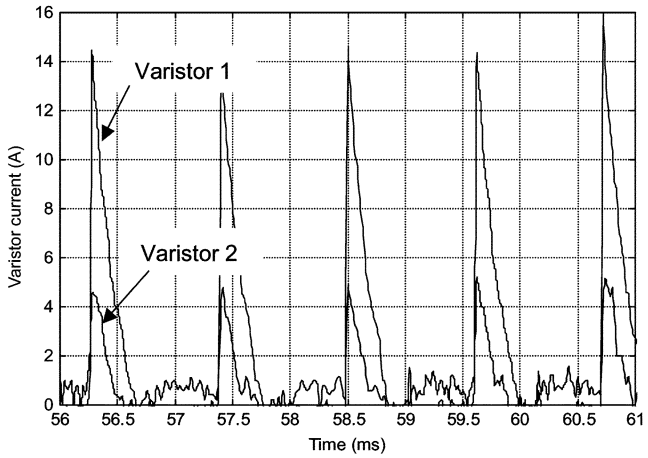

Fig. 9. Varistor unequal current sharing.

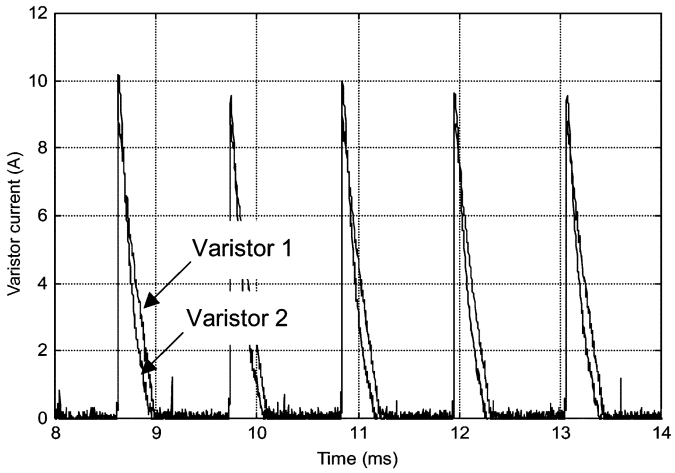

Fig. 10. Varistor equalized current sharing.

the matching of varistor characteristics is extremely difficult due to the nonlinearity of the I–V relationship [17]. One of the paralleled varistors would tend to conduct the majority of the current leading to failure of that device and then cascaded failure of the other MOVs. To prevent the failure, the authors employed a method to equalize the current sharing. In this method, each varistor is connected in series with a small resistor which adds to the onstate dynamic resistance of the varistor, but has little effect on the offstate resistance. Fig. 9 shows the currents measured in two directly paralleled varistors in an experimental setup, featuring unequal sharing. Fig. 10 shows the equalized current sharing with 5-Ω series resistance for each varistor. Tests were carried out to illustrate the effects of the series resistance. Table I shows the effect on the peak current sharing between two varistors, while Table II shows the effect on the peak voltage across the designed FCLID during varistor clamping when the semiconductor switch is turned off. It is clear that the higher the resistance is, the better the current sharing will be. It is also clear that the peak voltage across the FCLID increases with the resistance. When the series resistance is below 5 Ω, the voltage increase is less than 10% of the nominal clamping voltage (600 V). This has little effect on the voltage rating of the semiconductor switch.

TABLE I
EFFECT OF THE SERIES RESISTANCE ON THE CURRENT SHARING

R(Ω)	0	1	2	3	4	5
I_1 (A)	17	14	13	12.5	11	10.2
I_2 (A)	3	6	7	7.5	9	9.8

TABLE II
EFFECT OF THE SERIES RESISTANCE ON THE VOLTAGE ACROSS THE FCLID

R(Ω)	0	1	2	3	4	5
V(V)	595	596	600	605	624	642

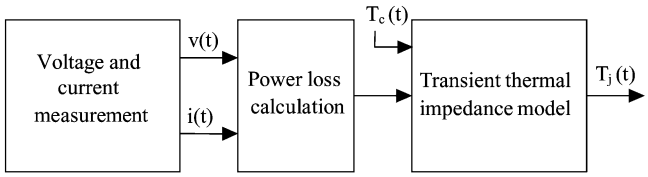

Fig. 11. Temperature prediction of the IGBT.

In the present study, eight standard varistors, each with a series resistor of 5 Ω, have been connected in parallel to achieve the required energy rating for the prototype FCLID. Data of the varistors are given in Section VI. Due to the equalized current sharing, the energy handling capability of the parallel combination could be significantly improved compared to unequal current sharing.

V. PROTECTION OF THE FCLID

As described in Section IV-C, the energy absorption capability of the varistors can be increased with equalized current sharing. Also, as explained in Section IV-B, the FCLID may be designed such that the junction temperature of the controlled IGBT switch is kept within the limits specified by a manufacturer's data sheets. Despite this, the FCLID will no doubt experience uncertain operating conditions in practice, including uncertainties in the system short-circuit level, ambient temperature, and required operating time. This is further complicated by the fact that the characteristics of the components are temperature dependent. For instance, the switching time of an IGBT is significantly increased as the junction temperature rises, increasing the switching losses [18]. It is therefore important to devise a real-time protection scheme for the FCLID. In this work, a method to predict the junction temperature of the IGBT in transient conditions has been developed. The instantaneous values of the device current and voltage were used to calculate the power losses in the semiconductor switching devices. A computer model is employed to predict the instantaneous junction temperature of the component $T_{\mathrm{j}}(\mathrm{t})$ based on the transient thermal impedance model [16] and the measured case temperature $T_{\mathrm{c}}(\mathrm{t})$ as shown in Fig. 11.

Fig. 12 shows the predicted junction temperature, using measured IGBT current i(t) and voltage v(t) of the FCLID prototype in a test that lasted for 1 s. The accuracy of the method is dependent on the accuracy of the voltage, current, and case temperature measurements in addition to the accuracy of the synthesized transient thermal impedance model of the IGBT. Transducers

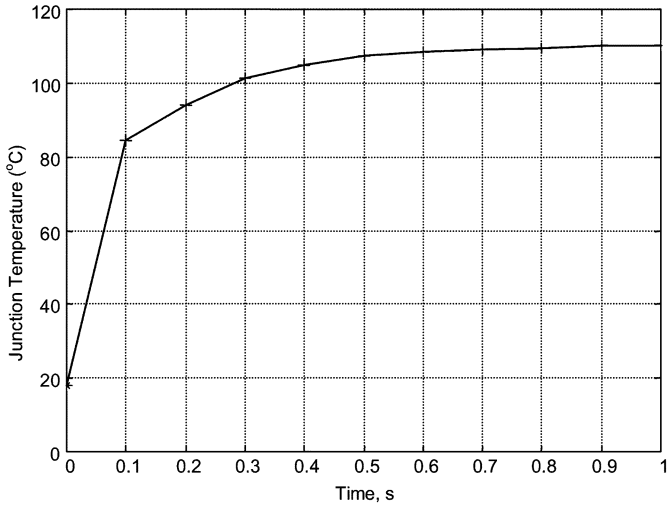

Fig. 12. Prediction of the IGBT junction temperature.

TABLE III
FCLID SPECIFICATIONS AND COMPONENT PARAMETERS

Item		Rating
Power system	rated voltage	230 V, rms
	frequency	50 Hz
Current	normal load current	50 A, rms
	short-circuit	3 kA, rms
Solid-state switch	rated voltage	1200 V
	rated pulsating current	300 A
Snubber circuit	resistance	15 Ω
	capacitor	47 nF
Varistor	rated voltage	250 V
	maximum clamping voltage	650 V
	rated energy	880 J

with wide frequency bandwidth are essential to capture the fast switching edges. The method to predict the junction temperature was verified in a destructive test.

The same concept of temperature prediction may also be applied to the prediction of the varistor temperature since the relationship between the input energy to the varistor and its temperature is linear, within the thermal stability region [11].

VI. EXPERIMENTAL RESULTS AND ANALYSIS

The analytical and simulation results described in the preceding sections were used to develop a single-phase FCLID prototype, based on the specifications presented in Section II. The parameters of the selected components are summarized in Table III. The solid-state switch is comprised of two IGBTs with built in inverse-parallel diodes, which gives it the ability to block high voltage in both directions. In addition, a simple RC snubber circuit was connected across the switch to protect the device from the high *dv/dt* effect during the initial part of the turnoff process. Eight varistors were connected in parallel to share the current when the solid-state switch is turned off and clamp the voltage to a safe limit.

Fig. 13 shows a photograph of the developed FCLID prototype. The VCB was not included in the design in order to

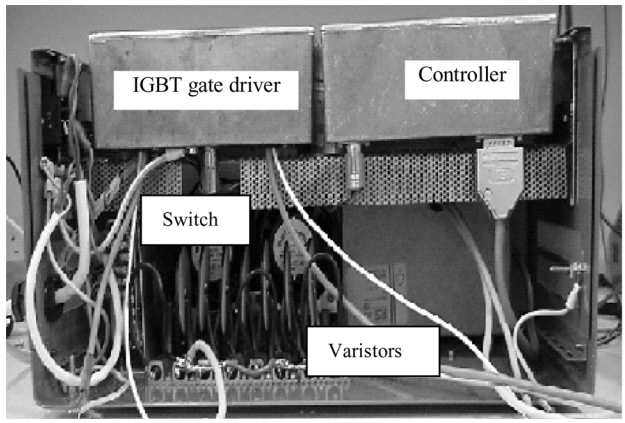

Fig. 13. Photograph of the prototyped FCLID.

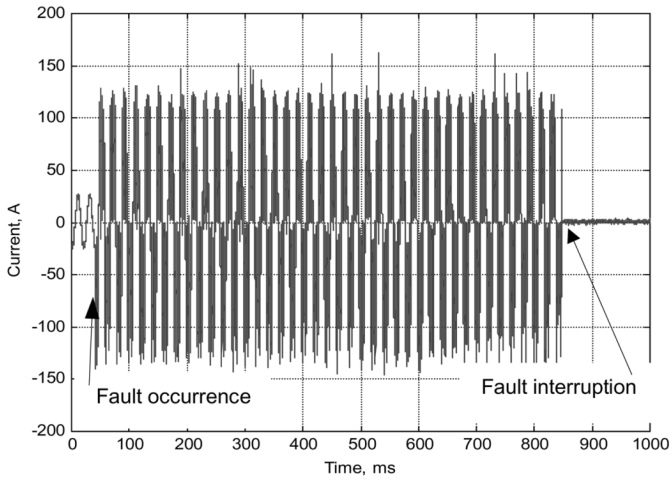

Fig. 14. Current waveform.

simplify the development of the prototype, as explained in Section IV. To test the prototype, it was connected as shown in Fig. 1 and its performance was evaluated for short-circuit faults on the load side (initiated by closing the switch across the load). Fig. 14 shows the waveform of the short-circuit current being limited to approximately 120 A (peak) for a period of 0.8 s. The load current before the fault occurrence was set to 18 A rms and the prospective short-circuit current was measured to be 3 kA rms. The fault was initiated at $t = 40$ ms and the FCLID started to operate immediately afterward where the IGBT began to switch on and off in order to keep the current between $I_{\max}$ and $I_{\min}$. The fault was cleared at a preset time $t = 840$ ms by keeping the IGBTs gated off. The small current that flows after this time is the leakage current through the varistor, which can be completely interrupted by an isolator (Fig. 1) if required.

It can be noted that the first peak of the short-circuit current, shown in Fig. 2 as I_{VCB}, is not present in Fig. 14. This is because the VCB was not implemented in the prototype. Also, $I_{\max}$ was set to approximately 120 A and $I_{\min}$ to nearly 0 A in this test. Note that the current shown in Fig. 14 was externally measured and contained some noise caused by radio-frequency interference (RFI) from fast current switching of the FCLID. A magnified section of the current waveform (for a fundamental cycle when the noise level is low) is shown in Fig. 15, with a redefined time scale.

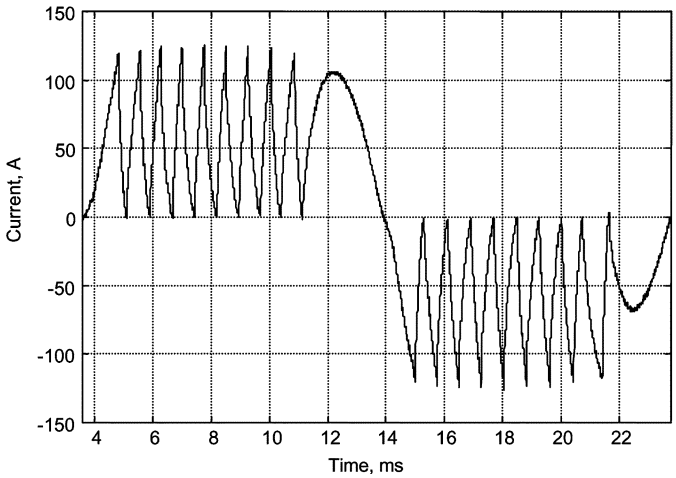

Fig. 15. Magnified section of the current waveform.

The current waveform shown in Fig. 15 is similar to the simulated one shown in Fig. 2; the switching frequency is different due to different system parameters. As the laboratory experiment was carried out without the bypassing VCB, the FCLID in the experiment was activated by a slightly different mechanism to that illustrated in Fig. 2. In the experiment, the IGBTs in the FCLID were initially gated on and were first gated off upon detecting the line current reaching 120 A which activated the FCLID ON/OFF operation. As explained in Section IV-A, the current will further increase during the controller interruption time, but this increase is relatively small (about 2.6 A in 2 μs) when the IGBT would actually turn off. A further increase of the current can be estimated according to $\Delta i = v/L \cdot \Delta t$ where L is the circuit inductance. Obviously the longer the delay is following activation, the higher would be the current increase which the IGBT must be able to safely turn off. Reference [10] reported a study which shows, for typical applications in a 230/400-V distribution network, a maximum delay of up to 10 μs is possible which gives a current rise of about 13.3 A. This current rise is relatively small and may be easily taken care of by careful selecting the IGBT current rating.

In the experimental tests conducted, once the FCLID was activated, it remained in the current limiting mode until it was externally stopped and the fault current was permanently interrupted. In practice, certain indicators may be used to decide how long the FCLID should stay in the current limiting mode. This could be a preset signal determined by the operator (based on system conditions) or a signal from the real-time thermal protection scheme described in Section V. If the fault is cleared by a downstream protective device, the FCLID can automatically return to the full conduction mode since the current will no longer reach $I_{\max}$ and the IGBTs will remain in the on state.

The possibility of scaling up the voltage and current ratings of the FCLID is important when dealing with high-power applications. The proposed architecture of the FCLID assists in connecting series/parallel devices to achieve high-voltage/current ratings.

IGBTs have a positive temperature coefficient and, therefore, it is relatively easy to operate them in parallel to obtain high current ratings [16]. Therefore, the current capability of the FCLID can be increased by increasing the number of varistors and IGBTs connected in parallel.

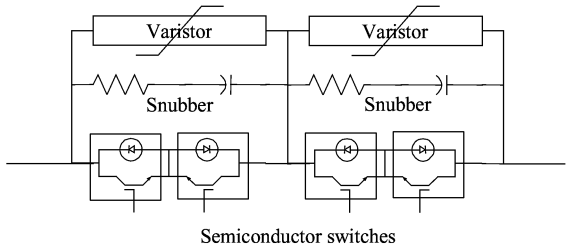

Fig. 16. Series connection of switches.

A known difficulty for the high-voltage applications is to connect IGBTs in series to achieve the required voltage rating. While active gate drive could be utilized to improve voltage sharing among series-connected IGBTs [19], the proposed FCLID implement varistors in its structure which (due to their nonlinear characteristics) can assist in equalizing the voltage sharing. In line with the circuit topology and control scheme of this study, Fig. 16 shows an envisaged scheme in which the varistors used within the FCLID can be used to assist the IGBT voltage sharing.

VII. Conclusion

The development of a 120-A solid-state FCLID is presented in this paper. Based on the analysis, simulation, and experimental tests, the following can be concluded.

1) The FCLID can inherently perform two integrated functions: limiting and interrupting the short-circuit current. A switching strategy is proposed to control the limited current when the network condition and fault location vary.
2) This FCLID is able to limit a prospective short-circuit current of 3 kA (rms) to 120 A (peak). The FCLID can respond quickly after the fault occurrence.
3) Based on the FCLID requirement and characteristics of the available switching devices, IGBTs were chosen for this application.
4) An effective method for improving the current sharing between parallel varistors has been implemented and the required energy rating of the varistors for the FCLID application has been achieved.
5) The developed prototype FCLID is capable of limiting the fault current for up to 0.8 s, which is sufficient to enable several types of practical applications.
6) Prediction of the junction temperature of the IGBT and varistor leads to fully protected and fail-safe operation of the FCLID.

The technology used in this high-speed, multifunction, and multishot system provides useful experience for developing higher-current FCLIDs for 11-kV distribution networks.

Acknowledgment

This paper describes part of a development work which is covered by Patent GB2375902 [14].

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