Energy-band alignment of $HfO_2/SiO_2/SiC$ gate dielectric stack

R. Mahapatra,[1,a)] Amit K. Chakraborty,[2] A. B. Horsfall,[1] N. G. Wright,[1] G. Beamson,[3] and Karl S. Coleman[2]
[1]*School of Electrical, Electronic and Computer Engineering, Newcastle University, Newcastle upon Tyne, Newcastle NE1 7RU, United Kingdom*
[2]*Department of Chemistry, Durham University, South Road, Durham DH1 3LE, United Kingdom*
[3]*National Centre for Electron Spectroscopy and Surface Analysis (NCESS), STFC Daresbury Laboratory, Warrington WA4 4AD, United Kingdom*

(Received 12 November 2007; accepted 9 January 2008; published online 30 January 2008)

The band alignment of $HfO_2/SiO_2/SiC$ gate dielectric stack has been investigated by x-ray photoelectron spectroscopy and electrical characterization. Two types of valence band offsets are observed in the stack layer; the smaller value of 1.5 eV corresponds to the HfO_2/SiC band offset while the larger one of 2.2 eV is due to the interfacial SiO_2/SiC. The barrier height is extracted to be 1.5 eV from the Schottky emission characteristics and is higher than the reported value for HfO_2 on SiC without interfacial SiO_2. Thus, presence of an interfacial SiO_2 layer increases band offsets to reduce the leakage current characteristics. © *2008 American Institute of Physics*.
[DOI: 10.1063/1.2839314]

The integration of high-dielectric constant (κ) gate oxides for silicon carbide (SiC) based metal-oxide-semiconductor (MOS) devices has attracted much attention recently due to its enhanced electrical strength and stability.[1–6] However, several challenges exist in implementing high-κ gate oxides into SiC-based MOS devices. One such challenge is the low band offset at the high-κ/SiC interface due to the wide band gap of 4*H*-SiC (3.26 eV) and the modest band gap of high-κ oxides (typically 5–7 eV). Recently, Tanner *et al.*[7] reported a conduction band offset of 0.7–0.9 eV at the HfO_2/4*H*-SiC interface, which results in insufficient barrier height causing an unacceptably high leakage current. The low band offsets at the high-κ/SiC interface may be overcome by introducing an ultrathin SiO_2 interfacial layer (IL) between SiC and high-κ gate dielectrics.[2] However, no experimental results of band alignment of $HfO_2/SiO_2/SiC$ gate dielectric stack have been reported until now in the literature. Therefore, it is of great importance to investigate the possible band alignment of a $HfO_2/SiO_2/SiC$ stack layer in order to explore its potential as a gate dielectric stack for SiC-based MOS device applications. In this letter, we report, for the first time, the band alignment of $HfO_2/SiO_2/SiC$ gate dielectric stack investigated by x-ray photoelectron spectroscopy (XPS) and electrical measurements.

n-type 4*H*-SiC wafers with 10 μm thick epilayer (doping concentration of 3×10^{15} cm^{-3}) were used as substrates in this study. A conventional Radio Corporation of America cleaning was performed, and then the wafers were dipped in a dilute HF solution to remove native oxides from the SiC surface prior to oxidation. The initial thin (~4–6 nm) SiO_2 layers were grown on 4*H*-SiC substrate at 1150 °C in dry O_2 for 15–30 min. The thickness was measured by capacitance-voltage characteristics. Then HfO_2 films were grown on SiO_2/4*H*-SiC layers by evaporating metallic Hf (~3 and ~25 nm) in an electron beam deposition system at substrate temperature of 200 °C and base pressure of 1×10^{-6} mbar, followed by thermal oxidation in dry O_2 ambient at 650 °C. The thicknesses of HfO_2 films were measured by Tencor P-1 profilometer and were almost unchanged after oxidation of metallic Hf. The XPS was performed to investigate the valence band and core level electronic structure of the dielectric stack layers using a Scienta ESCA 300 photoelectron spectrometer. Electrical characteristics of HfO_2-based gate dielectric stacks were carried out using fabricated Al-metal gate MOS capacitor structures with a HP4155A semiconductor parameter analyzer.

Figure 1(a) shows the valence band (VB) spectrum of 4*H*-SiC. The valence band maximum (VBM) is determined by extrapolating a tangent to the spectrum at the point where the intensity falls rapidly near the Fermi level. The valence band maximum ($E_{\mathrm{VBM}}^{\mathrm{SiC}}$) for 4*H*-SiC is found to be 1.8 eV. The VB spectra of bulk HfO_2 (~25 nm), bulk SiO_2, and thin HfO_2 (~3 nm)/SiO_2 (~4 nm)/SiC stack are shown by the curves I, II, and III in Fig. 1(b), respectively. The VBM for bulk HfO_2 ($E_{\mathrm{VBM}}^{\mathrm{HfO_2}}$) and bulk SiO_2 ($E_{\mathrm{VBM}}^{\mathrm{SiO_2}}$) are observed at 3.3 and 4.5 eV. The valence band offsets for HfO_2/SiC and SiO_2/SiC are found to be 1.5 and 2.7 eV, respectively, using the following relations:

$$\Delta E_V^{\mathrm{HfO_2/SiC}} = E_{\mathrm{VBM}}^{\mathrm{HfO_2}} - E_{\mathrm{VBM}}^{\mathrm{SiC}}, \tag{1a}$$

$$\Delta E_V^{\mathrm{SiO_2/SiC}} = E_{\mathrm{VBM}}^{\mathrm{SiO_2}} - E_{\mathrm{VBM}}^{\mathrm{SiC}}. \tag{1b}$$

These values are similar to previously reported results.[7,8] Conversely, it is interesting to note that two valence band maximum features are observed for $HfO_2/SiO_2/SiC$ layer as shown in the inset of Fig. 1(b). Similar behavior has also been reported in HfO_2/IL/Si system.[9,10] The smaller band offset of 1.5 eV corresponds to the HfO_2/SiC band offset while the larger band offset of 2.2 eV is due to the interfacial SiO_2/SiC band offset. It should be mentioned here that the interfacial SiO_2/SiC band offset of 2.2 eV in $HfO_2/SiO_2/SiC$ structure is smaller than the bulk SiO_2/SiC band offset of 2.7 eV. This discrepancy is due to intermixing of HfO_2 and interfacial SiO_2 making a silicatelike complex interfacial oxide which is confirmed by XPS core level spectra, as discussed below.

[a)]Author to whom correspondence should be addressed. Electronic mail: rajat.mahapatra@ncl.ac.uk and k2raj@yahoo.com.

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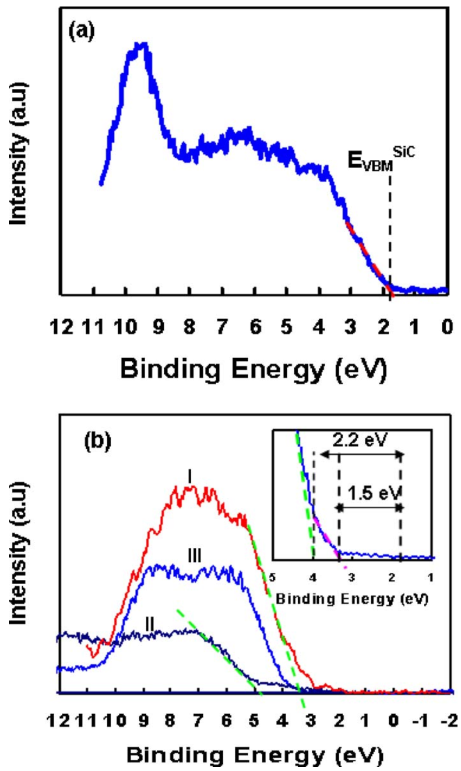

FIG. 1. (Color online) (a) the valence band (VB) spectrum of 4*H*-SiC substrate. (b) The VB spectra of (I) bulk HfO_2 (~25 nm), (II) bulk SiO_2, and (III) HfO_2 (~3 nm)/SiO_2 (~4 nm)/SiC, respectively. Two valence band offsets of 1.5 and 2.2 eV are observed for $HfO_2/SiO_2/SiC$ layer, as shown in the inset.

Figures 2(a) and 2(b) show Hf 4*f* and Si 2*p* core-level spectra of HfO_2 (~3 nm)/SiO_2 (~4 nm)/SiC gate dielectric stack at the surface as well as in the interfacial layer (between 3 and 8 nm depth), respectively. The spectra show strong signatures of HfO_2 at the surface, indicated by the position of the Hf 4*f* doublet at ~17.65 and 19.30 eV [Fig. 2(a)]. The peak position is further shifted to higher binding energies in the interfacial layer, indicating the formation of a Hf-silicate-like complex oxide.[11] In the Si 2*p* core level spectrum of the interfacial layer [Fig. 2(b)], a peak at 100.2 eV corresponding to the SiC substrate is observed and the additional high energy features contain the information of interfacial oxide layer. It is known that the binding energy difference between the stoichiometric SiO_2 and SiC is about 3.5 eV.[12] However, in Fig. 2(b), the high energy peak is gradually shifted toward the SiC substrate peak across the interfacial layer. The lower Si 2*p* binding energy shifts (2.0–2.6 eV) from the SiC peak is due to the result of the silicatelike compound in the interfacial layer rather than a pure SiO_2. As the substrate temperature during Hf deposition is low, the silicate may be formed during the oxidation of Hf at 650 °C.

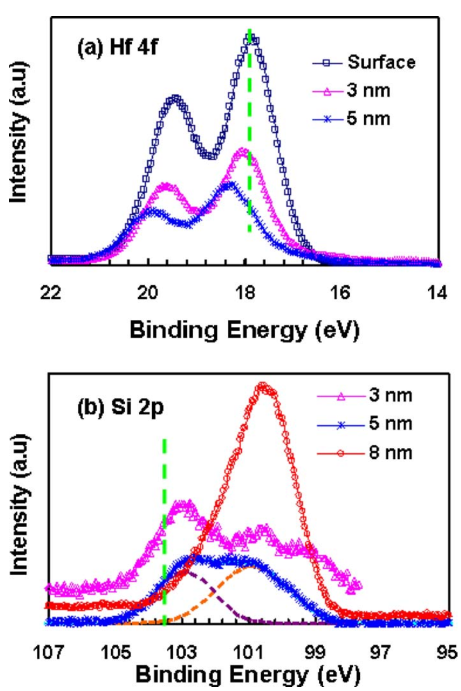

FIG. 2. (Color online) Photoelectron spectra showing (a) Hf 4*f*, and (b) Si 2*p* of HfO_2 (~3 nm)/SiO_2 (~4 nm)/SiC gate dielectric stack at the surface as well as in the interfacial layer (at 3–8 nm depth), respectively.

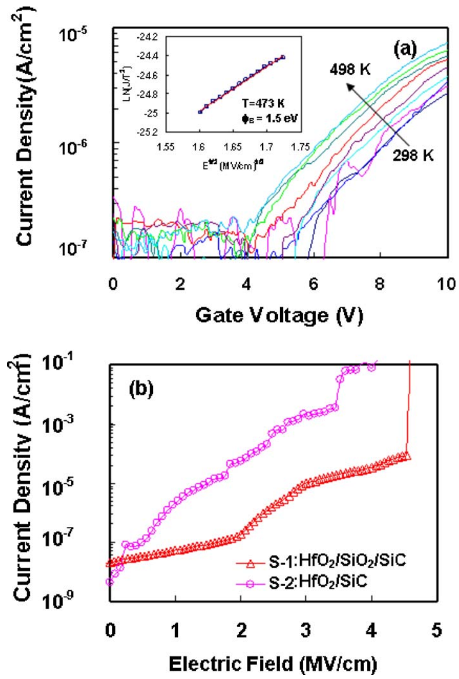

FIG. 3. (Color online) The current vs gate voltage characteristics of the Al/HfO_2 (~25 nm)/SiO_2 (~6 nm)/SiC MOS capacitor at various temperatures with substrate electron injection. The experimental results at higher temperatures fit the Schottky emission theory very well, as shown in the inset. (b) Leakage current density of HfO_2(~25 nm)/SiO_2(~6 nm)/SiC and HfO_2(~25 nm)/SiC gate dielectrics.

Figure 3(a) shows the current versus gate voltage characteristics of the Al/HfO_2/SiO_2/SiC MOS capacitor at various temperatures under substrate electron injection. The experimental results at higher temperatures fit the Schottky emission theory very well, as shown in the inset of Fig. 3. The standard Schottky emission can be expressed as

$$J = A^* T^2 \exp\left[\frac{-q(\phi_B - \sqrt{qE/4\pi\varepsilon_r\varepsilon_0})}{kT}\right], \qquad (2)$$

where A^* is the effective Richardson constant given by $A^* = 4\pi q(m_{\mathrm{ox}}^*)k^2/h^3$. The dynamic dielectric constant estimated from the slope of the Schottky plot [inset in Fig. 3(a)] is quite close to the reported value of 3.69 for HfO_2,[13] which is the square of the measured refractive index ($n=\varepsilon_r^{1/2}=1.92$). The barrier height ($\phi_B$) is calculated to be ~1.5 eV from the intercept of the curve (inset in Fig. 3), and is higher than the

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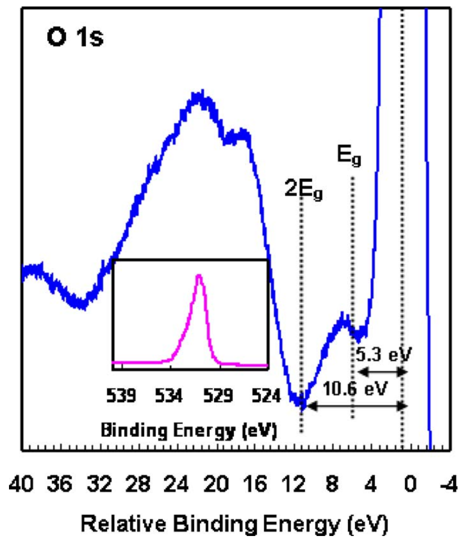

FIG. 4. (Color online) O 1*s* spectra (inset) and its energy loss for HfO_2 (~3 nm)/SiO_2 (~4 nm)/SiC gate dielectric stack.

previously reported value (~0.7 eV) for HfO_2 on SiC without interfacial SiO_2.[7] We also note that the introduction of the ultrathin interfacial oxide layer between HfO_2 and SiC lowers the leakage current density compared to that for HfO_2 directly deposited on SiC, as shown in Fig. 3(b). The dielectric breakdown fields are found to be 3.4 and 4.5 MV/cm for HfO_2/SiC and HfO_2/SiO_2/SiC, respectively.

The complete band alignment follows once the band gap (E_g) of HfO_2 is known. Figure 4 shows the O 1*s* core level energy loss spectrum of HfO_2/SiO_2/SiC system containing features due to photoelectrons which have lost energies of E_g and $2E_g$. The band gap of HfO_2 is found to be 5.3 eV from the O 1*s* loss spectroscopy which is consistent with the reported results.[10,14] Based on the results presented in this letter, the diagrams for the energy-band alignment for HfO_2/SiC and HfO_2/SiO_2/SiC systems are drawn schematically in Fig. 5. Assuming a value of 3.26 eV for the band gap of 4*H*-SiC and using the value of extracted barrier

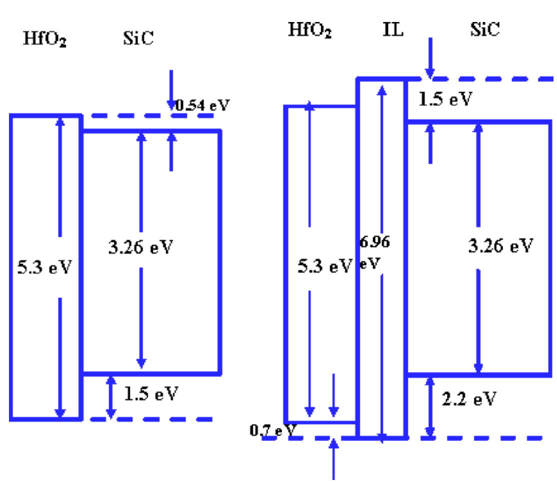

FIG. 5. (Color online) The schematic band alignments for HfO_2/SiC and HfO_2/SiO_2/SiC systems.

height, the band gap of the interfacial oxide layer is extracted to be 6.96 eV. It is interesting to note that the band gap of interfacial oxide layer is reduced from the actual value (~8.9 eV) of SiO_2. This is due to the intermixing of HfO_2 and SiO_2 layers in the interface which is elucidated by XPS core level spectra as discussed earlier and this extracted band gap value is comparable to the reported value of Hf silicate.[15]

In conclusion, the band alignment of HfO_2/SiO_2/SiC gate dielectric stack has been investigated using x-ray photoelectron spectroscopy and electrical characteristics. Two valence band maxima features are observed in the stack layer. The smaller band offset of 1.5 eV corresponds to the HfO_2/SiC band offset while the larger one of 2.2 eV is due to the interfacial SiO_2/SiC. The barrier height or conduction band offset is extracted to be 1.5 eV. Thus the growth of an initial SiO_2 layer increases band offsets to reduce the leakage current characteristics which suggests that the HfO_2/SiO_2/SiC stack layer will be a potential gate dielectric for SiC-based MOS device applications. A further optimization to grow the dielectric stack with an abrupt interface is believed to improve the interface morphology and also the electrical properties. In particular, a strong attention should be given to minimization of the formation of the intermixing layer at the interface.

This work was funded by the U.K. Engineering and Physical Sciences Research Council (EPSRC) (Grant No. EP/0068827/1). The EPSRC is also thanked for financial support of the NCESS facility under Grant No. EP/E025722/1.

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