Multi-level 3 bit-per-cell Magnetic Random Access Memory concepts and their associated control circuit architectures

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Abstract—Designs for two novel multi-level Magnetic Random Access Memory (MRAM) concepts are presented in this paper along with their associated control circuit architectures. Both the ChiralMEM and 3D-MRAM concepts contain 8 states with distinct electrical resistances, giving a 3 bit-per-cell capacity. Operation of the two memory concepts are presented along with designs for the circuitry in particular focusing on the conversion of three conventional binary bits to octal encoded data and the required sequence for writing 8 states per cell using current driven magnetic fields. Discrimination and subsequent conversion of the 8 read-out resistance levels back to 3 conventional binary bits is discussed along with the write sequence for controlling arrays of multi-bit memory cells.

***Index Terms*— 2D- and 3D-MRAM, multi-bit memory, MTJ stacking, control architecture, binary-octal conversion**

I. Introduction

The demand for random access memory has significantly increased over recent years due to the introduction of multi-processor computing. A data-centric rather than compute-centric movement within applications means that memory technology has had to rapidly advance to keep up with the requirements for modern computing.

To date, the primary method of increasing memory capacity has been to increase the density of the memory on a chip by making individual memory cells smaller. However, the scalability of conventional memory (DRAM) is reaching a fundamental limit with the 2007 ITRS roadmap stating that "manufacturable solutions are not known" for DRAM below the 40 nm fabrication process due to the cell bit-line capacitance ratio of the transistors [1]. Also of great concern in an energy conscious market is the high power consumption of DRAM due to its volatile nature [2].

To avoid the problems presented by DRAM, memory developers are looking to alternative technologies. The three main technologies aiming to compete with DRAM are flash, phase change memory and magnetic RAM (MRAM) [3-6]. All three have the advantage of being non-volatile, leading to low power consumption and are scalable below the 35 nm fabrication process. However, out of the three memory technologies, MRAM is the only one with unlimited read and write endurance with phase change and flash memory cells currently affected by degradation after approximately 10^5 cycles.

A single bit per cell MRAM [7, 8] has been commercially available since 2006 and has already found a market in data critical systems [9-11]. Unfortunately, problems have been encountered in increasing the density of existing MRAM. This is due to accidental writing ('half-selection') of neighboring cells as the bits become more densely packed.

One method which is increasingly being investigated as a method for increasing memory density without the need to pack cells closer together is multi-level memory. In multi-level memory, the conventional two states (1 bit) within a single memory cell are replaced by structures capable of storing data in 4, 6 or even 8 states, potentially tripling the density of the memory [12-20].

In this paper we present two MRAM concepts which are capable of increasing the density of MRAM through the use of multiple magnetic states within a single memory cell and by utilizing the third dimension to stack multiple magnetic memory modules around a single vertical current line [19-22]. The concepts also have the added advantage of being fundamentally less susceptible to half selection of bits than conventional MRAM devices.

II. Conventional MRAM

The central component of an MRAM cell (Figure 1a) is a spintronic device structure called a Magnetic Tunnel Junction (MTJ). At the most basic level, an MTJ consists of two ferromagnetic layers separated by a thin insulating spacer layer (Figure 1b).

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The digital 1 and 0 memory states are set by the relative parallel or antiparallel alignment of the two magnetic layers. The magnetization direction of the bottom layer is pinned in one direction by a synthetic antiferromagnet [23, 24] whilst the magnetization of the top layer is free to rotate under the influence of an applied magnetic field or spin-polarized current.

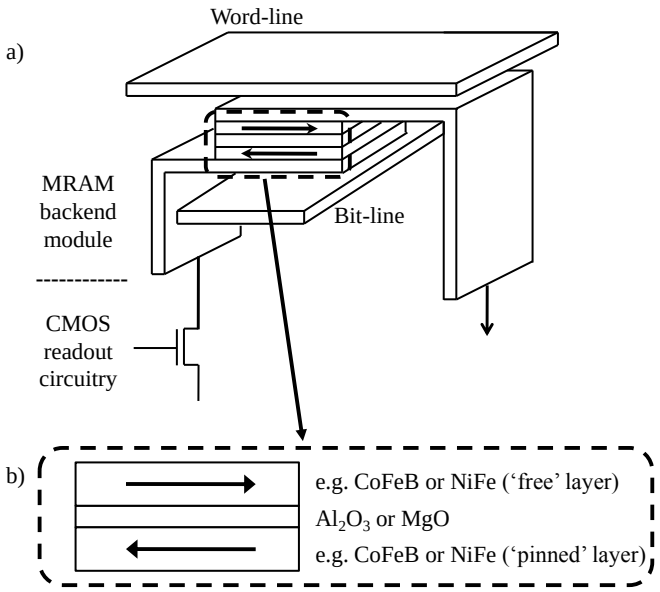


Figure 1. a) Schematic diagram of conventional field switched Magnetic Random Access Memory (MRAM) b) Simplified view of the magnetic tunnel junction (MTJ). The magnetization direction of the top magnetic layer ('free' layer) can be switched from alignment parallel to the bottom layer ('pinned' layer) to an alignment anti-parallel using the magnetic fields generated by application of current to the word- and bit-lines.

The change in relative orientation between the two magnetic layers changes the electrical resistance through the cell, which is read out via contacts on the top and bottom of the MTJ. If the magnetization of the layers are parallel, the resistance is low and the cell is classed as being in state 0. Conversely, the resistance is high when the two layers are antiparallel and the bit has a value of 1. The ratio of the resistances in the parallel and antiparallel alignments is termed the Tunneling Magnetoresistance (TMR) ratio and is stated as a percentage change, $\Delta R/R_{parallel} = (R_{antiparallel} - R_{parallel})/R_{parallel}$.

Writing the data state to MRAM is carried out by one of two methods: field driven or spin torque transfer (STT). In field driven MRAM the free layer magnetization is switched by the magnetic field generated from a pair of crossed strip lines close to the MTJ. A limiting feature of this design is the distance between neighboring cells which can lead to accidental writing or 'half-selection' of the MTJ by adjacent word and bit lines if the distance is reduced too far.

Spin Torque Transfer (STT) MRAM uses a spin polarized current passing through the MTJ to reverse the magnetization state [25]. STT-MRAM requires a high current density to switch the magnetization state of the MTJ, limiting reductions in the size of the access transistor beneath the MTJ (since the transistor minimum feature size is proportional to the current it can drive [26]). This high current density also leads to degradation and breakdown of the tunneling barrier, limiting write endurance of the STT-MRAM cell. Furthermore, the currents used in read and write operations are similar, which may cause accidental writing of the cell during a read attempt.

Increasing MRAM density through the reduction of MTJ cell size creates severe challenges which have the potential to hamper the commercial competitiveness of MRAM. An alternative approach for enhancing memory density is to increase the number of bits in a single memory cell. Discrimination of multiple intermediate resistance levels in an single MRAM cell was not possible in the first generation of MRAM due to the small resistance ratios of the MRAM cells which used a metallic spacer layer to produce resistance ratios of the order of a few tens of percent by Giant Magnetoresistance (GMR) [8, 27].

In the latest generation of MRAM, TMR is exploited rather than GMR through the use of a dielectric rather than metallic material as the spacer layer. The properties of the dielectric spacer layer and quality of the interfaces between the spacer layer and magnetic layers are crucial in determining the resistance ratio of the structure [28]. TMR ratios of up 70% are possible for Al_2O_3 (alumina) and up to 600% for crystalline MgO dielectric barriers [4, 7, 8, 29, 30]. These materials therefore open up the possibility of the accurate discrimination of intermediate resistance states making multi-level MRAM an exciting workable possibility for increasing memory density.

III. MULTI-LEVEL MRAM

In this paper two multi-bit per cell designs are presented which have the potential to eliminate the 'half-select' and thermal stability problems of conventional field driven MRAM. The first solution has been termed ChiralMEM [19-21]. For this memory concept a single MTJ structure is fabricated from an elongated nanostructure containing asymmetrical structural pinning features along its length. The pinning features have the ability to prevent complete magnetization reversal within the free layer of the MTJ and hence allow the controllable formation of multiple stable magnetization states (Figure 2a). The elongation of the nanostructure also inherently improves bit stability.

The second novel design contains three stacked MTJ structures (Figure 2b). The design uses a vertical current strip to generate a circumferential field that acts along the long axis of the three curved MTJs in each stack [20, 22].

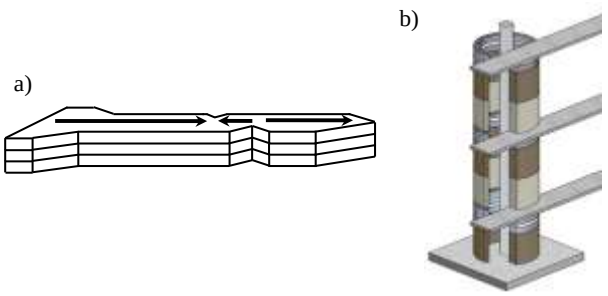


Figure 2. a) Schematic diagram of the cross section of a ChiralMEM multi-bit field switched Magnetic Random Access Memory (MRAM) cell. The top layer of the MTJ contains up to three separate magnetic domains which are controlled via the application of word-line and bit-line fields b) A 3D-MRAM cell which uses a single vertical word-line and 3 horizontal bit-lines to independently control the magnetization direction of each of the MTJs.

Both systems contain eight states with distinct resistances, giving three bit-per-cell capacity. Each of the concepts have different advantages; ChiralMEM has the benefit of being based upon a single MTJ structure, but requires more complex magnetic behavior, whereas, 3D-MRAM is more challenging to fabricate but each MTJ has simpler magnetic behavior requiring a less complex write sequence.

A. Operation of ChiralMEM multi-bit magnetic memory

The principle of operation of ChiralMEM is similar to that of conventional MRAM. In conventional MRAM, the digital states, 1 and 0 are represented by the whole of the free layer being aligned in a single uniform magnetization state (either parallel or antiparallel to the pinned layer). By comparison, ChiralMEM is able to support multiple regions of oppositely directed magnetizations within a single free layer. This is achieved by controlled pinning of magnetic domain walls at structural features in the free layer, allowing a range of metastable remanent magnetization states to be generated which represent different digital states. Each of the resulting remanent magnetization states has a different resistance which depends upon the proportion of parallel and antiparallel regions of magnetization in the MTJ.

A magnetic domain wall is the boundary between two regions of opposing magnetization. Within the domain wall the magnetic moments of neighboring atoms rotate to gradually reverse the magnetization direction. The direction of rotation of the moments determines the chirality of the domain wall (i.e. clockwise or counter clockwise) and can initially be set by the application of a transverse magnetic field.

A domain wall can be propagated along the length of a magnetic nanostructure by the application of an axial magnetic field. As the axial field is increased a domain wall is nucleated at one end of the structure, and moves along the length of the nanostructure without hindrance unless a magnetic pinning feature is introduced, such as a geometrical notch. In this case the domain wall is ‘pinned’ at the feature, creating two regions of opposing magnetization within the nanostructure.

It is important to note that strong pinning of a domain wall at a structural feature will occur only if the chirality of the domain wall opposes the sense of rotation of the magnetic moments at the pinning feature. The chirality dependent pinning brings the benefit that the number of different field levels required to write multiple magnetic states is reduced compared to a multi-bit cell relying simply on different field amplitudes. Detailed information on the magnetic functionality of ChiralMEM and 3D-MRAM can be found in references [22, 31-33].

The distance between pinning features in the free layer can be used to tune the resistance levels representing each of the memory states. The present design for ChiralMEM has a total of 8 states formed from the pinning of either 0, 1 or 2 domain walls along the length of the free layer. The unique resistance of each of the 8 states means that a single ChiralMEM cell is equivalent to 3 conventional binary bits.

The write process for ChiralMEM operates by the application of magnetic fields of varying magnitudes generated from the crossed current lines to propagate and pin domain walls within the free layer of the nanostructure. As discussed above, two magnetic field components are required to set the chirality of the injected domain wall and to propagate it along the free layer of the MTJ. In order to maintain the use of conventional MRAM terminology, the transverse field current line has been termed the bit-line and the axial field current line the word-line. The bit-line current is set at a single magnitude with positive or negative polarity and the word-line current has one of two magnitudes with positive or negative polarity. As mentioned earlier, if chirality dependent pinning was not used, more than two magnitudes would be required, increasing the complexity of the write sequence.

The write sequence for the eight magnetization configurations of ChiralMEM has three stages (Figure 3). In the first stage, the free layer is set with uniform magnetization in a direction either parallel or antiparallel to the magnetization of the pinned layer. The second stage creates two regions of opposing magnetization by creating, propagating and pinning a single domain wall. Finally, for the third stage, three regions of magnetization are created by a second domain wall that is propagated and pinned at the remaining structural feature. Each stage is subdivided into two sub-stages with the word-line current alternating between positive and negative polarity. The magnetization of the free layer is written only if the bit-line current is applied coincidentally with the word-line current. If the bit-line is off when the word-line is on, the magnetization remains unaffected as a domain wall is not created.

Figure 3 contains examples of the write sequence for two of the eight possible magnetization states in the ChiralMEM free layer (with the final magnetization alignment shown schematically below the write sequence).

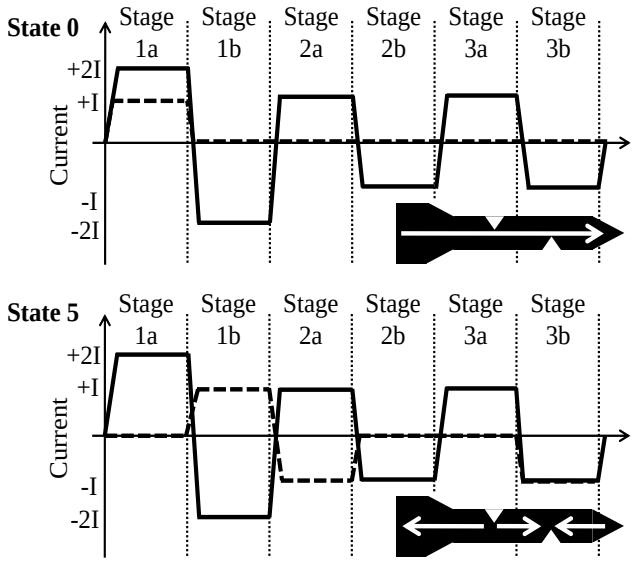


Figure 3. The timing diagram for the write sequence of a ChiralMEM MRAM cell. The graphs show the current applied to set the bit-line (dashed) and word-line (solid) fields. Three write stages are required to write a three domain state to memory, each stage contains two sub-stages where the word-line current alternates between positive and negative polarity. The bit-line is activated only at the required stages of the word-line sequence. The examples shown in the figure represent the write sequence for state 0 (no pinned domain walls) and state 5 (two pinned domain walls).

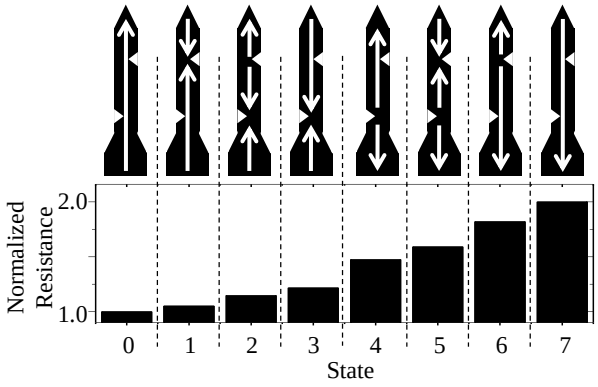


Figure 4. Schematic diagram of the free layer magnetization states and associated normalized calculated resistances of the magnetic tunnel junction for each of the eight magnetization states in a ChiralMEM MTJ cell. Resistances are calculated for 100% TMR ratio.

All eight magnetization states are shown in Figure 4. In state 0 the magnetization of the ChiralMEM free layer is saturated parallel to the pinned layer. Figure 3 demonstrates that in order to write such a configuration, the magnetization of the free layer is changed only in stage 1a and remains unchanged in all later stages of the write sequence i.e. the bit-line field remains off during all stages of the write sequence apart from stage 1a.

State 5 requires two pinned domain walls so all stages of the write sequence are needed. The free layer is first saturated in the antiparallel direction in stage 1b with the first domain wall pinned in stage 2a and the second domain wall pinned in stage 3b. In stages 1a, 2b and 3a the bit-line current is off.

Reading from the memory cell is carried out using electrical contacts placed on the top and bottom surfaces of the MTJ which are connected to a transistor in the CMOS front-end module. The memory state is established using circuitry capable of discriminating between the different voltage levels from the resistance measurement. A large tunneling magnetoresistance ratio is needed to accurately discriminate between the intermediate states [34].

Figure 4 shows an example of the calculated TMR ratios for each of the 8 states. States 0 to 7 are numbered in order of the increasing resistance of the MTJ. The resistance of the MTJ has been modeled using the criteria given by Camblong et al. for the case where spin flip is allowed in the material and the spin flip length is significantly smaller than the domain size [35]. This criteria holds for the ChiralMEM structures, where the ratio of the lengths of the three sections shown in Figure 4 are 0.6 : 0.28 : 0.12 for the region before the first notch, between the first and second notch and after the second notch, respectively. Each section is considered to be an individual domain and the length of the shortest domain is greater than one micron. This is significantly greater than the spin flip length in conventional TMR materials [36].

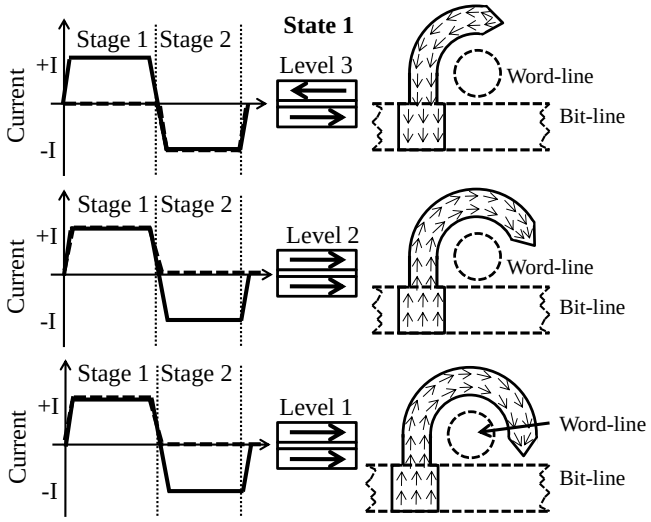


Figure 5. The timing diagram for the write sequence of an eight level 3D-MRAM structure showing the current applied to set the bit-line (dashed) and word-line (solid) fields for the three levels. A schematic of the magnetization of the top level of the multilayer stacks is shown for each of the three MTJs.

The total resistance of the MTJ structure has been calculated by considering the structure as a network of resistors comprised of three parallel sections connected in series [35]. The resistance of the three parallel sections represents the relative local orientation of the magnetization of the ChiralMEM free layer and the pinned layer. A TMR ratio of 100% has been used in the calculation of resistance in Figure 4, which is similar to the ratios currently used in commercial MRAM [37]. Such a treatment for the calculation of the resistance of magnetic tunnel junctions has been shown to compare well to experimental data in ring shaped MTJs and MTJs using artificial ferrimagnets [38,39]. Theoretical calculation of the resistance of GMR structures with multiple states was also shown in the work by Zhang and Levy [34].

B. *Operation of 3D stacked multi-bit magnetic memory*

The proposed 3D-MRAM is similar to ChiralMEM and conventional MRAM but introduces the concept of vertical stacking of MTJs. In conventional MRAM the word- and bit-lines are both horizontal current strips. In 3D-MRAM a novel vertical current rod or 'via' runs up the centre of the curved MTJ structures acting as the word-line for each cell. In the first embodiment of the design, three MTJs are stacked above one another around a word-line, with an individual bit-line to write each MTJ. This vertical word-line has benefits for reducing cross-talk between cells and the half-select problem experienced by conventional MRAM.

Each MTJ in a single 3D-MRAM cell can be in one of two digital states with the magnetization of the free layer aligned wholly parallel or antiparallel to the pinned layer. The MTJ is switched between the two magnetization states through the application of coincident currents through the word- and bit-lines which combine to create a local magnetic field large enough to switch the selected MTJ free layer.

The two magnetization states within each MTJ correspond to two resistance levels and, as before, the TMR ratio giving the resistance of the parallel and antiparallel magnetization states is determined by the materials and structure of the MTJ. The resistance of each of the three MTJs in the stack is unique and determined by the design of the structure. For the memory presented here, the shortest MTJ is at the top of the stack (Level 1) and the longest at the bottom (Level 3) (Figure 5).

Selection of appropriate resistances and TMR ratios can give an approximately linear relationship between the 8 resistance states for the stack when summed in series. Multiple magnetization states within each MTJ are not required in this design, however, a ChiralMEM type free layer would increase the number of states within in each MTJ structure [22].

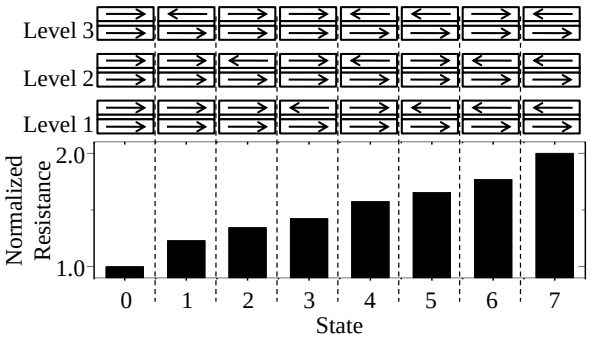


Figure 6. Schematic diagram of the free layer magnetization states and associated normalized calculated resistances of the three magnetic tunnel junctions (assuming 100% TMR ratio) connected in series for each of the eight combinations of magnetization states in the 3D-MRAM structure for a ratio of resistance levels of the magnetic tunnel junctions of 1 : 1.5 : 1.85.

The write sequence for the eight states in this embodiment of the 3D-MRAM takes place in two stages (Figure 5). The word-line current alternates between a positive and negative polarity of the same magnitude in write stage 1 and 2 respectively. A bit-line current with the same polarity is then activated for each MTJ in one of the two stages, depending upon the magnetization direction required. If no bit-line current is applied, the magnetization of the free layer does not switch. Figure 5 shows the sequence to write state 1 to memory. The word and bit-lines are activated together in stage 1 for Levels 2 and 3 and in stage 2 for Level 1. This places Level 1 into an antiparallel state and levels 2 and 3 into parallel alignments.

The resistance of the 3D-MRAM cell is read using contacts placed on the top and bottom of the cell containing the three MTJ structures. As with ChiralMEM, maximizing the resistance ratios for the MTJs is desirable in order to reduce the uncertainty in the discrimination between individual states. Figure 6 shows the calculated resistances for the eight levels of the 3D-MRAM. The calculations presented here assume a TMR ratio of 100% from the MTJs and the resistances of the three MTJs are summed in series to calculate the overall resistance of the cell. The states are labeled in order of increasing resistance. The ratio of the resistances of the MTJs are controlled by geometry and here have been set at 1 : 1.5 : 1.85 for Level 1, Level 2 and Level 3 respectively.

IV. MULTI-BIT MEMORY ARCHITECTURE

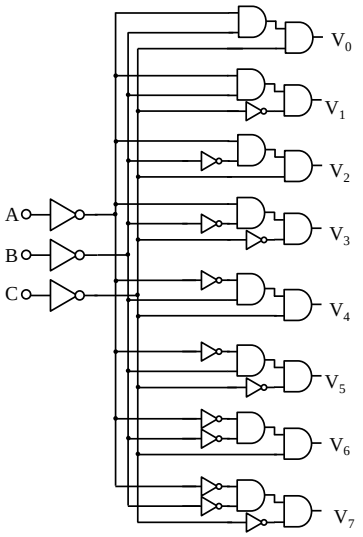
This section details the control architecture for writing to and reading from the eight states of ChiralMEM and 3D-MRAM. The circuitry can be broken down into four sections (Figure 7). The first two stages are involved in the writing of the data to memory and the final two stages with reading the data. In order to write data to the multi-bit memory cell, the incoming data is converted from three binary bits to a single octal encoded level. The octal encoded data is then written to memory using a sequence of crossed word- and bit-line currents of varying magnitudes. To read data from the memory, the resistance across the MTJ is read and the voltage level discriminated before being converted back to binary data.

A. *Data writing: Binary to octal conversion and write sequence*

Figure 8 shows a schematic diagram of a logic circuit for the conversion of three binary inputs to one of eight outputs. The binary input at gates A, B and C is converted into a single voltage output at the correct terminal between V_0 to V_7. The logic circuitry is such that only one of the eight outputs can be active at any given time as shown in the truth table in Figure 8. Figure 9 is a schematic diagram of the circuitry for the application of the three stage write sequence for ChiralMEM.

The first stage in the ChiralMEM write sequence is the selection of one of the eight outputs from the binary to octal convertor. Once the required state is selected, a series of six inputs are activated which connect to the time synch logic circuit. The six inputs supply the bit-line with the required current levels for the write sequence i.e. stages 1a, 1b, 2a, 2b, 3a and 3b (see Figure 3). The bit-line can be set with a positive, negative or zero current at each of the stages.

The time synch logic component of the circuit ensures synchronization of the 6 bit-line current inputs with the corresponding six stages of the word-line current sequence.



A	B	C	Output
0	0	0	V_0
0	0	1	V_1
0	1	0	V_2
0	1	1	V_3
1	0	0	V_4
1	0	1	V_5
1	1	0	V_6
1	1	1	V_7

Figure 8. Schematic diagram of the control architecture for the conversion of three binary inputs (A, B and C) into a single voltage output at terminals V_0 to V_7. Only one of the eight outputs can be active at any given time as shown in the truth table.

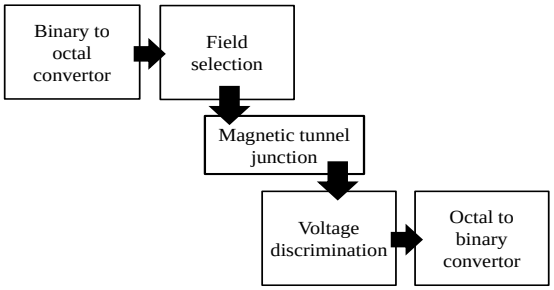


Figure 7. Schematic diagram illustrating the integration of a multi-level field driven MRAM cell with CMOS read and write circuitry for binary input and output.

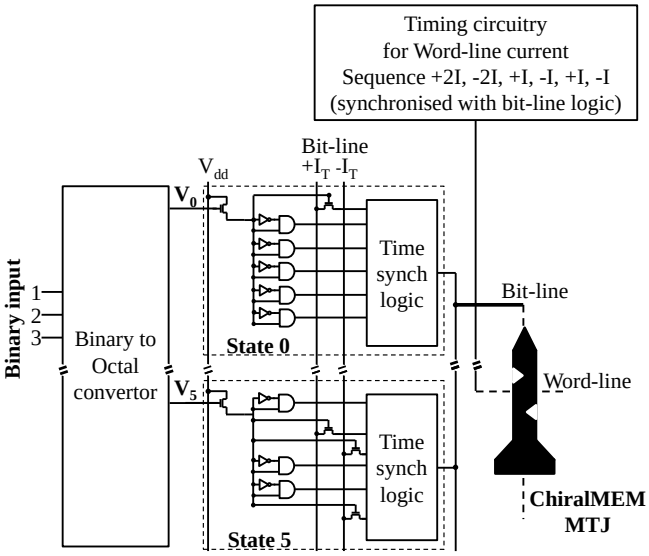


Figure 9. The structure of the control circuitry for the application of selected word- and bit-line currents to write the magnetization states of the ChiralMEM free layer.

The examples shown in Figure 9 are for state 0 and state 5 of ChiralMEM. In the case of state 0, the bit-line is active with a current of +I during the first stage of the write sequence and 0 for the remaining stages. For stage 5, the bit-line current applies a sequence of 0, +I, -I, 0, 0, -I synchronized to the +2I, -2I, +I, -I, +I, -I stages of the word-line write sequence.

Figure 10 shows the schematic diagram of the write circuitry for 3D-MRAM with examples for memory states 0, 1 and 7. A set of three transistors is connected to each of the eight outputs of the binary to octal convertor. Only one of the sets of transistors is activated depending upon which output is triggered.

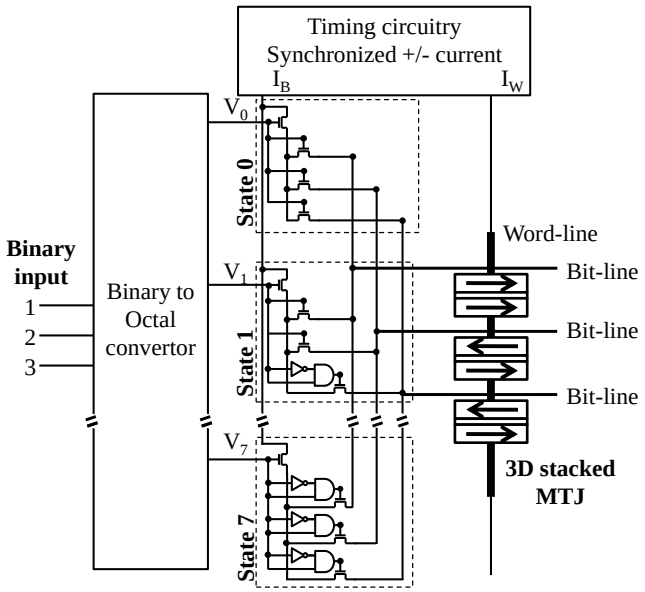


Figure 10. The structure of the control circuitry for the application of selected word- and bit-line currents to write the magnetization states of the individual layers of the 3D-MRAM structure. The word-line current is switched between positive and negative polarity in stages 1 and 2 of the write sequence, respectively. The bit-line current is activated during only one of the two write stages, depending upon the direction of magnetization required.

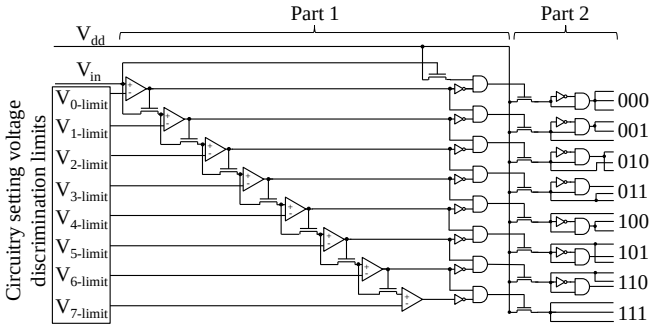


Figure 11. Logic circuitry for the discrimination (part 1) and conversion (part 2) to three binary outputs for the 8 levels of magnetic tunnel junction resistance from a single ChiralMEM or 3D-MRAM cell.

The three transistors pass current in one of the two stages of the write sequence, applying a positive current to the bit-line in stage 1 or a negative current in stage 2. The bit-line current is synchronized with the positive and negative stages of the word-line current sequence so that either two positive currents are simultaneously applied to both the word and bit-line or two negative currents. In the case of state 0 the transistors pass a

positive current to the bit-line of all three MTJs during stage 1 of the word-line cycle. No current is applied to the three bit-lines in stage 2 of the write cycle. To write state 1, the transistors are set to pass a positive current in stage 1 of the write cycle to the bit-lines of Level 1 and 2 and a negative current during stage 2 to the bit-line of Level 3. For state 7, a negative current is applied in stage 2 to all three of bit-lines with no currents applied during stage 1.

B. Data readout: Resistance discrimination and octal to binary conversion

Figure 11 is a schematic diagram of the circuitry for the conversion of one of 8 resistance levels of the memory cell back to 3 binary bits and is considered in two parts. First, the resistance of the cell is read and voltage discrimination determines which of the 8 memory states has been stored. The input voltage, V_{in}, from the readout across the cell is compared with the eight preselected voltage levels shown as $V_{x\text{-}limit}$, where *x* is 0 to 7. If V_{in} is greater than V_0 the signal is passed to the next level and continues to do so until V_{in} is less than the last compared $V_{x\text{-}limit}$ voltage. Once these criteria have been met, the zero output from the comparator triggers the second stage of the conversion and the logic gate sequence converts from the octal level to the corresponding three binary outputs.

V. CONTROL SEQUENCE FOR AN ARRAY OF MULTI-BIT MEMORY CELLS

So far, the discussion of the control architecture has focused on writing to a single cell of memory. However, for implementation into a memory chip, the control architecture must be capable of writing and reading to a large array of cells. This section looks at the considerations and sequences for writing to an array of ChiralMEM and 3D-MRAM elements.

The ChiralMEM cells are arranged in a grid pattern where the word- and bit-lines cross, as shown schematically in figure 12. The simplest method of implementing the write sequence to the whole array is to activate only a single word-line at a time. The word-line current sequence is executed for only the cells on the first word-line along with the synchronized bit-line current sequence for each cell. This exposes every cell in the array to a bit-line current. However, because a current is only applied to the first word-line, the magnetization states are only written to cells along this line and the magnetization states of the remaining cells in the array are unaffected. Once the write sequence is completed for the first word-line, the process is repeated for subsequent word-lines.

Figure 13 shows the write sequence for an array of 3D-MRAM cells. The vertical word-lines in each column of the grid are connected by a single horizontal current strip running beneath the columns. A similar approach to that used for ChiralMEM is implemented to write to the array of 3D-MRAM cells. However, current sequences are applied to each of the bit-lines for the three stacked MTJ structures as opposed to the single bit-line per cell in ChiralMEM.

VI. CONCLUSIONS

The physical arrangements and control circuitry for two novel multi-bit per cell magnetic random access memory (MRAM) concepts have been presented in this paper. In ChiralMEM, eight magnetic states representing 3 bits are stored by pinning magnetic domain walls within an elongated nanostructure which forms the free layer of the magnetic tunnel junction (MTJ) of the memory cell. In 3D-MRAM the additional states are created through the vertical stacking of 3 MTJs each of which have a unique resistance due to differences in their structures. Both concepts offer the ability to triple the density of MRAM per cell.

The designs also offer solutions to two of the common problems associated with conventional field driven MRAM:

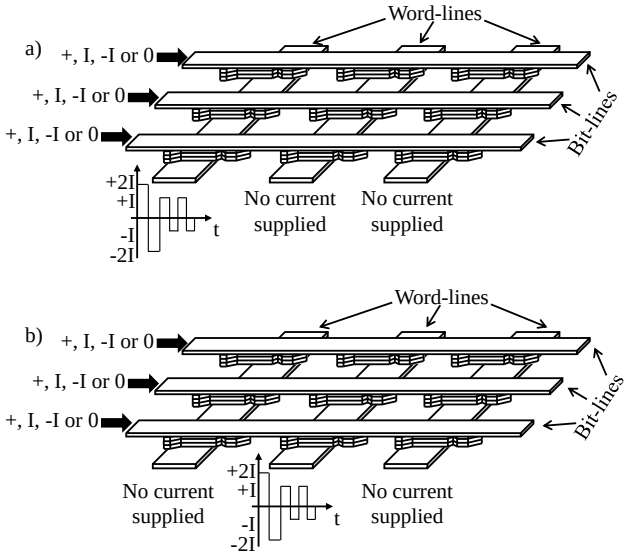


Figure 12. Schematic diagram illustrating the sequence for electronically writing to ChiralMEM cells in an array. In part a) The left hand word-line has the current applied in sequence (+2I, -2I, +I, -I, +I, -I) with the remainder of the word-lines inactive. The required bit-line current sequences are applied to all bit-lines but only the cells with both fields present are written. In part b) the process is then repeated with only the second word-line active.

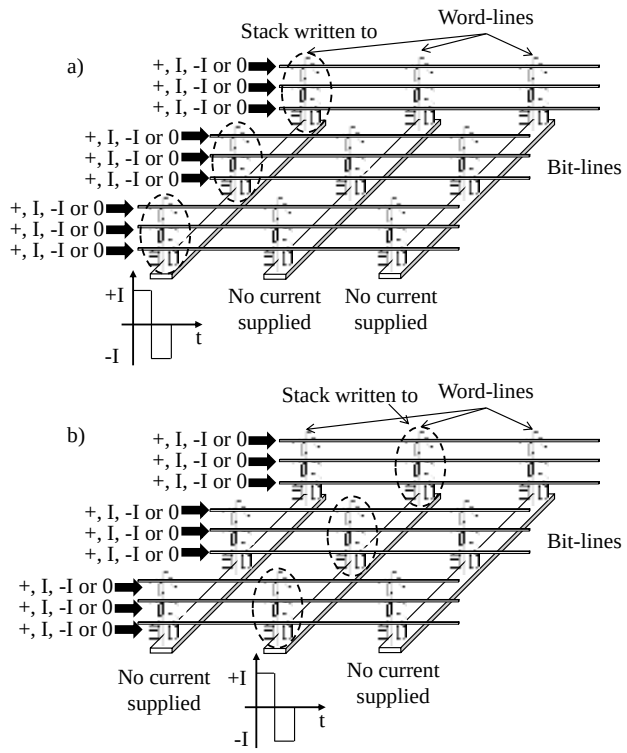


Figure 13. Schematic diagram illustrating the sequence for electronically writing to 3D-MRAM cells in an array. In part a) the left hand word-line has the current sequence (+I, -I) applied with the remainder of the word-lines inactive. The current sequence is simultaneously applied to the bit-lines with only the cells with the active crossed fields being written. In part b) the process is then repeated with only the second word-line active.

half selection of bits and switching due to thermal instabilities. ChiralMEM inherently offers improved stability of the magnetization states due to its elongated structure. In addition, the requirement for the application of directional crossed fields means that half selection of cells is significantly reduced. The control architecture for binary to octal conversion, data writing, output discrimination and octal to binary conversion is given as an example for prototyping these novel concepts.

Finally, a simple method has been suggested for writing to an array of ChiralMEM and 3D-MRAM cells which reduces the risk of accidental writing of neighboring memory cells.

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