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Improving metal-oxide-metal (MOM) diode performance via the optimization of the oxide layer

Linzi E. Dodd · Samantha A. Shenton · Andrew J. Gallant · David Wood

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Abstract Small area metal-oxide-metal (MOM) diodes are being investigated in many research groups for the detection of THz frequency radiation. In order to create a high speed rectifying device, the central oxide layer of the MOM structure must be thin and have known physical characteristics. The thickness, structure and uniformity of the oxide can be controlled during the fabrication process. In the work presented here, the effects of both oxygen plasma concentration and annealing temperature during fabrication of Ti/TiO_x/Pt MOM diodes have been explored. It has been found that by reducing the oxygen gas concentration from previous work, the TiO_x layer can be more repeatable and uniform. Furthermore, for an anneal temperature up to a threshold temperature in the 200 °C to 250 °C range, the performance of the diodes is excellent, with a value of zero-bias curvature coefficient (CC_{ZB}) that can be up to 4.6 V^{-1}. For higher temperature treatments, the value of CC_{ZB} decreases to a maximum of 2.0 V^{-1}. Similar trends in AC tests can be seen for voltage and current responsivity values.

Keywords high speed · MOM · metal-oxide-metal · diode · diodes · terahertz · rectification · THz · plasma oxidation · annealing · ToFSIMS · responsivity · AFM · curvature coefficient

Linzi E. Dodd

School of Engineering and Computing Sciences, Durham University, South Road, Durham, DH1 3LE

Tel.: +44 191 3342537

E-mail: l.e.dodd@durham.ac.uk

1 Introduction

Metal-oxide-metal (MOM) diodes have potential applications in the rectification of THz radiation because of

their high switching speed of operation [1–4]. The use of dissimilar metals produces an asymmetric, non-linear I-V characteristic, resulting in a net current when rectifying. In this work, platinum and titanium have been used in order to maximize the difference in work function between the metals, although there are other alternative combinations[5].

In order for the diodes to work at high speed, the capacitance associated with the oxide layer must be minimized. In practice, this means diode active areas with dimensions <100 nm square [6]. The oxide dielectric constant should be small, and the oxide thickness is a trade-off between thick for low capacitance and thin for high speed electron tunneling as the current carrying mechanism. The importance of the latter dominates, and so oxide thicknesses are <5 nm [7].

Much work has been presented on diode performance, but with very little on repeatability, particularly with respect to device fabrication conditions. The present work investigates the effect of changing the temperature of an annealing step, which takes places after plasma oxidation of the titanium, on the DC and AC performance of the diodes using curvature and responsivity as a indicative measures. The motivation for this is in the potential application in energy recovery from heat sources, which radiate in the THz range. There is substantial interest in using MOM devices for this purpose, and heat exposure could have a major effect on both diode performance and repeatability.

This work investigates the effect of reducing oxygen concentration from previous work [8] resulting in an oxide whose thickness is a function of plasma power [9] which is more repeatable. Others have looked at a similar concept using a $Al/AlO_x/Pt$ system [10]. The oxidation of the titanium base layer takes place after a cleaning etch step in-situ in an Oxford Instruments combined reactive ion etch/plasma oxidation machine. The resultant oxides were then analyzed both electrical and physically.

This work also follows an investigation of the effect of annealing temperature on diode performance [11] using nickel/chromium diodes with a nickel oxide layer. Using atomic force microscopy, it was shown that the oxide roughness and crystallinity depended on the annealing temperature. The ideal structure was found to be polycrystalline at 250 °C, where the optimum electrical results were also obtained.

2 Experimental Details

2.1 Diode Fabrication

Details of the full fabrication method can be found in [8,12,13]. Briefly, fabrication was as follows: a bi-layer lift-off process using the photoresist PMGI SF9 followed

by Microposit SPR-350 was performed in order to deposit layers of 25 nm of titanium and 100 nm of gold as the base of each diode. The photoresist SPR-350 was then used to define areas of gold to be removed, via a wet etching step using (4:1:8 KI:I_2:H_2O), until visual inspection determined that the exposed gold had been removed (<1 minute), thus exposing areas of titanium to be oxidized. This oxidation was achieved using reactive ion etching, a process that removes a small layer of titanium (100 W, 100 mT, 20 sccm CF_4 and 2 sccm O_2 for 15 s - RIE mode), followed by plasma regrowth (150 W to 350 W, 500 mT and 50 sccm O_2 and 50 sccm Ar for 5 min - PE mode), which oxidizes the clean surface to a known thickness, typically in the 4 nm to 5 nm region, as confirmed by TEM studies [8]. By altering the plasma power, the thickness of the oxide can be varied.

Once the chosen oxide thickness was produced using the plasma oxidation method, the structure of this oxide can be controlled via an anneal step. Prior to the work presented here, the annealing step in the fabrication process was performed at 100 °C for 30 minutes on a hot plate. This step was introduced in order to bake the oxide layer and ensure no further oxidation took place in atmosphere, during testing. For the present work, the temperature was varied from 50 °C to 300 °C over 6 wafers in a nitrogen environment using a furnace. For simplicity, wafers identification is given

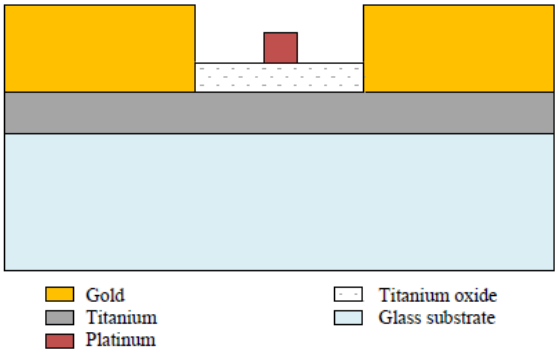


Fig. 1: The bi-layer lift-off fabrication process used in the production of MOM diodes

by these temperature values, although the peak temperatures obtained were a little higher (this is reflected in the actual temperature values used in the data of Figure 6). The fabrication process was identical for all wafers apart from this annealing step. A secondary bi-layer lift-off process was then undertaken to deposit the platinum to a thickness of 30 nm. Figure 1 shows the final diode structure after this fabrication process.

2.2 Device Layout and Testing

The configuration and dimensions of the diodes varied across the wafer. Figure 2 shows SEM images of a typical diode layout. The diode area itself is defined by the crossover region of the metalizations, with typical values in the 1 µm^2 to 10 µm^2 region: these are larger than ideal for high speed operation, but the areas chosen would prove any effect of annealing temperature, and give a better indication of uniformity, as large area

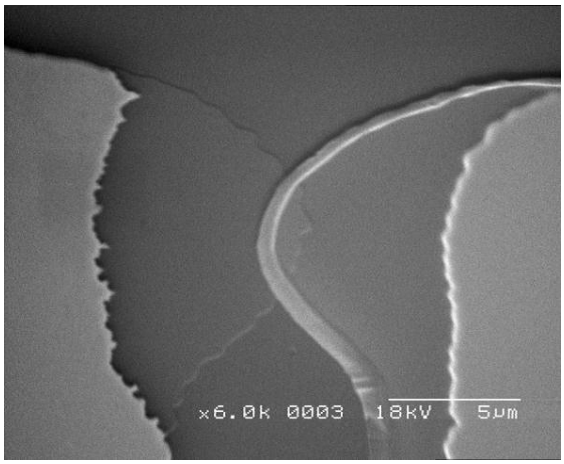


Fig. 2: SEM image of typical diode layout. The oxidised titanium is the left crossover material, and the platinum is on the right

diodes are more likely to have defects in the structure for a given defect density. The edge of the platinum layer can be seen to be raised in Figure 2, this is due to the lift-off process used to pattern the platinum. Because of the high melting point of platinum and the fact that e-beam deposition is used, the bi-layer lift-off procedure results in a rough edge profile, which does not affect the diode structure, as the platinum is the top layer. There were two groups of diodes: one with a single crossover region and one with multiple crossover regions, and both with different arm widths. Each group contained nine diodes, three sets of three repeats, with each set having a different separation between the contact pads.

In order to perform DC analysis on the diodes, a ninth order best fit was required for the I-V characteristic. From this, the first and second order derivatives could be calculated, with both the resistance and curvature coefficient for a given voltage V_b determined using Equation 1. The curvature coefficient (CC) is commonly used as a measure of diode performance and is a measure of how non-linear the diode is: for energy recovery applications, curvature is particularly important at zero volts applied bias (CC_{ZB}).

$$CC = \left(\frac{\frac{d^2I}{dV^2}}{\frac{dI}{dV}} \right) \Bigg|_{V=V_b} = \frac{d^2I}{dV^2} R \tag{1}$$

3 Results and Discussion

3.1 Physical Analysis of Reduced Oxygen Concentration Oxide

Time of Flight Mass Spectrometry (ToFSIMS) has been used to confirm the thickness of the oxide layers discussed here, with Atomic Force Microscopy (AFM), crater depth analysis and Transmission Electron Microscopy (TEM) used to calibrate the time measurement obtained from ToFSIMS, which can be seen in Figure 3. It can be seen here that the oxide thickness reaches a maximum with plasma power, and then the thickness decreases with additional power increases. It is believed that this is due to the interaction of two simultaneous processes taking place during the plasma oxidation; the oxide growth and surface etching from the plasma bombardment, as discussed in [8]. At low

powers the oxidation is dominant, with power range causing variations in thickness. However, beyond a certain threshold power, etching begins to dominate causing a sudden decrease in oxide thickness with any further power increase.

Previous results [8] showing a very sudden change in oxide thickness for small changes in power can be seen in green, with the reduced gas concentration results seen in blue. The power range over which an oxide thickness variation occurs is much larger, resulting in a more repeatable process for a given power. For the requirements of the project this thickness and power range is suitable, however if necessary it is believed that the gas concentration could be further altered to make even thinner oxides.

Note all electrical tests were performed on diodes fabricated using a 300 W plasma oxidation, which has been confirmed as being 4.2 nm thick using both AFM and TEM analysis.

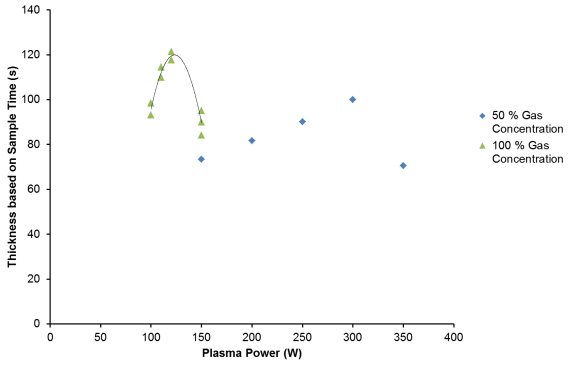


Fig. 3: ToFSIMS comparison between 100 % oxygen plasma diodes (green) and 50 % oxygen plasma diodes (blue) (line is for visual guidance)

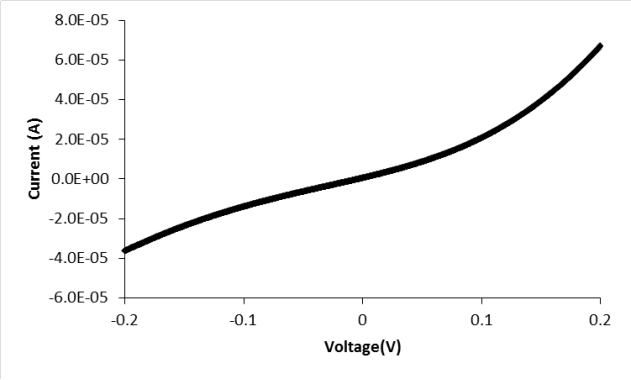
3.2 DC Testing

All diodes that passed visual inspection were DC tested using a Cascade RF/DC manual probe station with two triaxial probes. A voltage sweep between ±0.2 V with 1001 points was conducted. From this, typical results (shown in Figure 4) could be obtained.

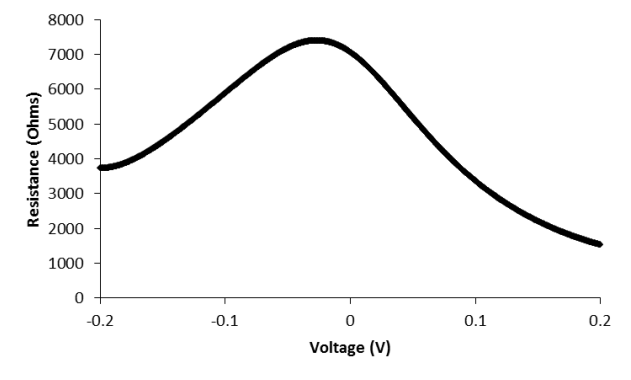
Device layouts were produced for all wafers and were populated with values of zero-bias resistance, zero-bias curvature, peak curvature and current ratio for each diode. It was anticipated that a trend would become apparent between some of these characteristics and the annealing temperature of the wafer. Table 1 shows that the average curvature for wafers 250 and 300 was less than half that of other wafers. Although these devices still show diode characteristics, the values achieved for curvature indicate that a threshold annealing temperature has been passed which reduces their performance dramatically. These results are comparable with those reported in [11], where the threshold annealing temperature is between 350 °C to 400 °C with a peak around 250 °C. The use of titanium and platinum in this project, in comparison with nickel and

Table 1: Mean zero-bias curvature, standard deviation and number of diodes tested for different annealing temperatures

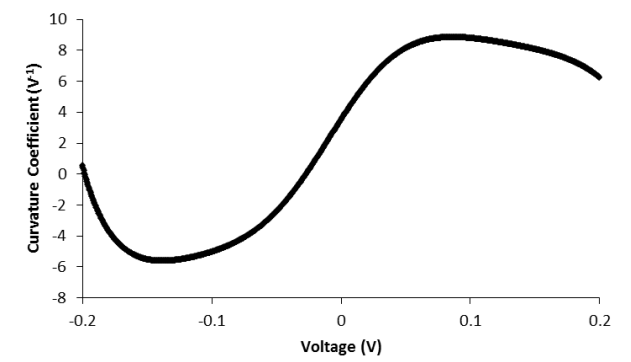
Wafer	Mean CC_{ZB} (V^{-1})	Standard Deviation (V^{-1})	Number of Devices
50	3.1	0.9	52
100	3.1	1.8	64
150	2.3	0.7	58
200	3.1	1.1	52
250	1.4	0.8	50
300	1.4	1.0	39



(a) I-V characteristics for a typical MOM diode



(b) R-V characteristics for a typical MOM diode



(c) CC-V characteristics for a typical MOM diode

Fig. 4: Typical Characteristics of a MOM Diode

chromium, is likely to explain the difference in this threshold temperature.

During analysis, it was noted that there was a linear relationship between the zero-bias resistance and the peak curvature reached by a diode. This relationship is present across the different diode sizes and layouts and also on every wafer. Figure 4b shows a typical plot of resistance with voltage and it can be seen that the peak of this plot is close to zero ($-0.028\,\mathrm{V}$). Equation 1 shows that resistance is a factor in curvature coefficient: for the largest value of resistance, the largest value for curvature will be achieved provided no other parameters change. In this case, other parameters do change and so the change in resistance is part of the reason for, but cannot fully explain, the values for peak curvature.

3.3 AC Testing

AC testing took place using an HP8753C Vector Network Analyser(VNA). An AC signal was sent to the diodes via a coplanar probe, and the resulting DC output monitored using an Agilent B2902A Source and Measurement unit via the Bias T connection on the VNA. AC testing was performed using power and frequency sweeps in order to gain values for both current and voltage responsivities of the diodes and also with the intention of performing lifetime testing. Power sweeps in the range −27 dBm to −22 dBm at set frequencies (300 kHz, 1 MHz, 10 MHz, 100 MHz, 1 GHz and 3 GHz) were conducted and typical plots are shown in Figure 5. For each frequency, a line of best fit was added to both the current and voltage data, with the gradient of this line being the current and voltage responsivity respectively. In some cases, at low power, the noise floor of the equipment was reached. These points were omitted from the line of best fit and not included in the analysis.

This data was then collated and the average responsivities over the frequency sweeps were calculated. In most cases, the responsivity dropped significantly at higher frequencies and, again, these results have been omitted from analysis. Table 2 shows responsivity results for the same diode as used in Figure 5.

Table 2: Responsivity data for a typical diode at different frequencies

Frequency (Hz)	Voltage Responsivity (V/W)	Current Responsivity (A/W)
3×10^5	5013	5.21
1×10^6	4979	5.07
1×10^7	5123	5.01
1×10^8	4928	4.00
1×10^9	1612	0.40
3×10^9	801	0.05

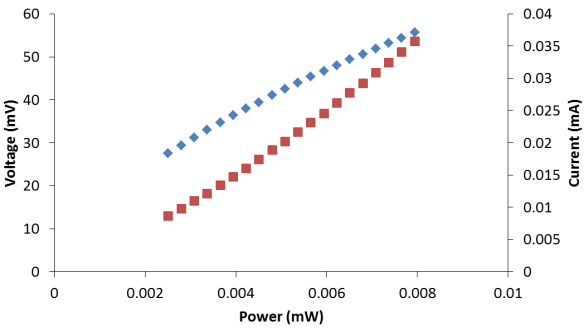


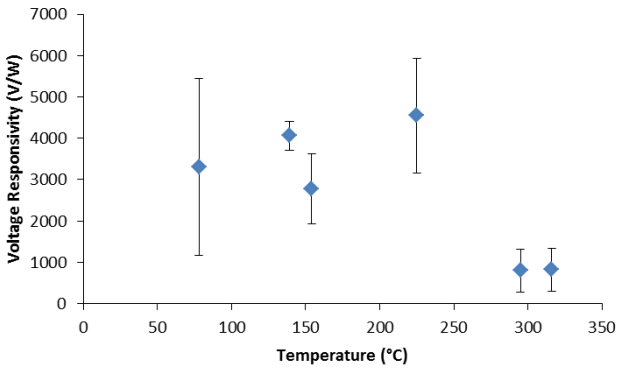
Fig. 5: Voltage (blue) and current (red) responsivity vs power for a 200 °C annealed diode tested at 10 MHz

It can be seen that, in this case, the voltage responsivity of the diode dropped by around 69 % and the current responsivity by 92 % at 1 GHz in comparison to 10 MHz. However, this decrease in performance is not due to a frequency limit in the devices themselves, but

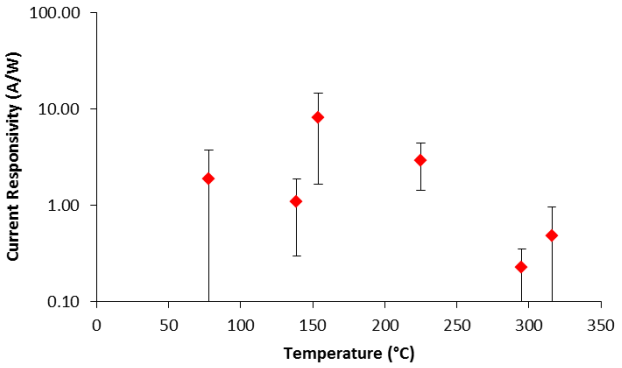
is due to the parasitic capacitance of the crossover region located in the gap between the coplanar waveguide signal and ground lines, which are in parallel with the intrinsic diode capacitance and coupled to the series resistance, which was measured to be in the range 30 Ω to 50 Ω, depending on the sample. The voltage responsivity can be seen to increase for wafer 200, with values lower than this for wafers annealed at other temperatures. This corresponds to what was anticipated from the DC results, as there is a clear threshold temperature between 200 °C and 250 °C, after which the performance of the diodes drops significantly.

The current responsivity shows a plot that agrees with results shown by other groups more closely than the voltage responsivity, with the highest current responsivity results occurring at approximately 150 °C. Previous results [11] show that the curvature of the diode peaks at an annealing temperature of 250 °C, decreasing at 350 °C and with values close to zero at 400 °C. By combining the results of both the voltage and current responsivity graphs, it can be seen that the optimum annealing temperature for a good response in both of these areas is approximately 150 °C to 200 °C.

After electrical testing was complete, AFM images were taken of the annealed TiO_x surface, on exposed regions either side of the covered Pt region. The annealing step, during the fabrication process, was found



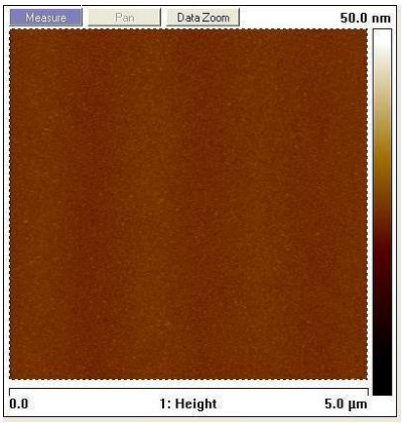
(a) Average voltage responsivity as a function of annealing temperatures



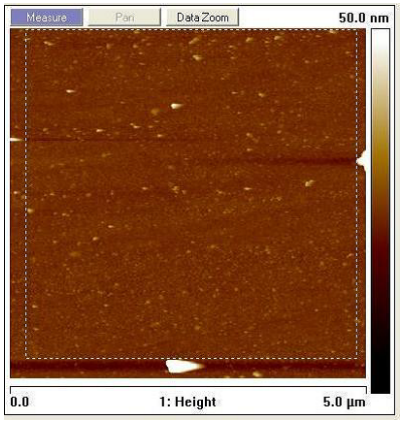
(b) Average current responsivity as a function of annealing temperatures

Fig. 6: Graphs showing responsivity as a function of annealing temperature

to have affected the structure of the oxide layer. These AFM images were used in order to study the effect on the oxide layer more closely. It was found that wafers 50, 100 and 150 had a lower roughness (R_a) than wafers 200, 250 and 300. Typical AFM pictures are shown in Figure 7 where the high temperature induced features can be seen clearly - the R_a values are 0.567 nm and 0.862 nm for wafers 100 and 250 respectively.



(a) AFM image of surface roughness for TiO_x annealed at 100 °C



(b) AFM image of surface roughness for TiO_x annealed at 250 °C

Fig. 7: Surface features of the exposed oxide region after annealing at two different temperatures

4 Conclusion

The effect of gas concentration and plasma power during the oxidation step, as well as annealing temperature on MOM diode performance has been investigated. The diodes show excellent DC performance as measured by the zero-bias curvature coefficient (CC_{ZB}), with values up to $4.6\,V^{-1}$ being achieved, up to an annealing temperature between 200 °C and 250 °C. Beyond this temperature range, the diode performance decreased until a maximum CC_{ZB} of only $2.0\,V^{-1}$ could be achieved. This has important ramifications for both diode fabrication and operation, particularly if long-term exposure to heat sources is likely. Trends in AC results, obtained via both voltage and current responsivity, show a similar threshold temperature effect. Furthermore, oxide thickness can be varied in a repeatable way as a function of plasma power, allowing greater control of diode characteristics.

Further work is looking at the failure mechanisms of the diodes, primarily current stressing and lifetime testing. As part of the current stressing, the diodes are being subjected to a continuous signal, at constant frequency and power, with DC readings taken periodically. For lifetime testing, the diodes are DC tested regularly in order to observe any decay in performance over an extended period.

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