Fabrication of micron scale metallic structures on photo paper substrates by low temperature photolithography for device applications

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Using commercial standard paper as a substrate has a significant cost reduction implication over other more expensive substrate materials by approximately a factor of 100 [1-2]. Discussed here is a novel process which allows photolithography and etching of simple metal films deposited on paper substrates, but requires no additional facilities to achieve it. This allows a significant reduction in feature size down to the micron scale over devices made using more conventional printing solutions which are of the order of tens of microns. The technique has great potential for making cheap disposable devices with additional functionality, which could include flexibility and foldability, simple disposability, porosity and low weight requirements. The potential for commercial applications and scale up is also discussed.

Keywords: *Paper, Flexible, Photolithography, Microelectronics*

Introduction

Silicon has long been the industrial standard substrate for devices made using photolithographic processing. It is only in recent years that more flexible substrates have become commercially interesting [3-4]. This is partially due to their potential to be used within the printing industry, as well as the possibility of developing flexible devices. Typical flexible films tend to be polymer based and have specialist coatings on the surface to allow the material to remain stable when being subjected to temperature and humidity changes [5-6].

To date, electronics work on paper substrates has tended to be limited to using a variety of printing techniques [7-8]. While these are ideal for roll to roll processes [9], there is a limitation on feature size which is achievable using printing; this limit is 20-40 microns [10]. Similarly a significant amount of device fabrication on paper tends to use a barrier layer on the surface to ensure the printed inks do not permeate into the cellulose matrix of the material [11].

There are many different types of papers available, each with their own unique properties [1, 2, 12]. Some of these can be found to be more suited to metal deposition than others. To date though, most electronics applications on paper use printing [13-14], with a few using a shadow mask technique or stencil [15-16].

Electrical measurements show that the conductivity of a feature on paper, when compared to the same feature on silicon, can vary depending on paper type as well as by the deposition technique, for both thin film and ink-jet printed devices

can vary depending on paper type as well as by the deposition technique. For example surface roughness can be found to change with surface finish, but depending on the deposition technique a rough or smooth surface can produce higher or lower resistance [17-18].

A large variety of applications have been demonstrated using printing on paper-based substrates, which have included RFID Antennas [19], transistors [20], displays [21], energy storage devices [22], PV cells [23] and sensors [24] and Cantilevers [25-26].

We present here a novel technique which allows a photolithographic process, similar to that used for patterning on silicon substrates, to be used on standard Epson photo paper when we introduce a modified bake process window. This is the first demonstration of such a process on standard photo-paper. Obviously there are many different types of paper as shown in [1-2]. Epson photo-paper is believed to have an alumina or silica coating, but this is proprietary to the manufacturer. No evidence was found of any specific chemical interactions with this layer, nor with the reverse side of the paper which we believe was uncoated. The ability to use photolithographic processes has a significant advantage in that it will allow an improvement in device performance by shrinking the minimum feature size. This is expected to be seen by giving an increased device density and faster operational frequency for devices. Furthermore, we show that it is feasible to etch simple gold structures with significant accuracy to give almost as good a resolution as found on silicon. We demonstrate how our process can produce functional electrodes on the paper and discuss how this process could be developed further. We also look at the robustness of the devices in terms of flexure and adhesive properties, providing some discussion as to how this might give limitations on device applications. Finally, the potential route to market for the technique is discussed, with comparison provided to more common place printing.

Experimental Details

Standard glossy Epson photo paper was taken as our base substrate [27]. This is known to have an optimal side for printing, which was the side used for device fabrication. Metallic thin films were e-beam evaporated onto the paper substrate – in this case a chromium (5 nm) / gold (60 nm) film was deposited. These were then coated using commercial Rohm and Haas S1813 resist using a Laurell spin coater and a custom membrane chuck to improve spin uniformity on flexible substrates. The bake times / temperatures were varied for optimisation (as will be discussed in the results section). The samples were exposed using an EVG 620 mask aligner using vacuum hard contact to ensure good pattern transfer. The mask chosen included a variety of test samples. Here we show the circular ring structures as a typical example of the features possible. The exposure dose was similarly investigated as an optimisation feature. The sample was then developed in MF319 developed for 1 minute, with mild agitation. The sample was etched using a specifically diluted gold etch solution (water:potassium iodide:iodine [600:4:1]) to allow control of the etch time to optimise the features, while the chromium was etched using a standard dilution etch solution (ammonium ceric nitrate:nitric acid:water [10 g:1 ml:70 ml]). Finally the resist was removed either using an exposure / develop process or acetone / isopropanol rinsing. The novelty in the process is in the exact process window and chemistries required to pattern on the paper substrates, which is significantly different to that seen on more usual microelectronic substrates.

Surface roughness measurements were performed using a Veeco Multimode AFM and Micromeasure STiL, which allowed us to determine the RMS roughness over 50 micron square areas

(in the case of the AFM) and up to 1 mm square regions in the case of the STiL. Structural characterisation was performed using a Hitachi S-2400 SEM. Electrical characterisation was made using a Cascade probe station and an interfaced HP 2092A source meter. Long term flexure trials were performed using a custom designed motorised stage and clamp system to give deformation of the sample from one end, giving the possibility of a large number of repeat cycles with a control flexure.

Results and Discussion

As is well known the effect of substrate roughness affects the quality of a device [28]. Measurements of the surface showed that the paper had a roughness of 15–20 nm in comparison to that found on silicon of 1-2 nm or glass of 5 nm.

For optimisation of the lithographic process, initially a standard 5 minute 95 °C bake with varying exposure doses from 50 to 300 mJ/cm^2 was trialled; it should be noted that a 75 mJ/cm^2 exposure gives optimum lithographic patterning on silicon substrates. This showed that in using the paper substrates the effect of increasing the dose gave some improvement, but it was apparent that the resist was not clearing in the exposed regions even with significant over-exposure and had become permanently bonded to the paper in the exposed areas. For example, a 70 mJ/cm^2 exposure dose showed no evidence of etching or patterning. Increasing the dose to 300 mJ/cm^2 showed what appears to be good patterning, but subsequently it was found that etching was not possible, demonstrating poor clearing of the resist layer at the bottom of the features, perhaps suggesting an interfacial effect between the paper and resist (as might well be expected).

Due to the fact that paper tends to soak up solvent and it is expected that the resist might penetrate deep into the paper (which was a possible cause of the issues in clearing the resist as discussed above), it was decided to examine the effect of bake temperature on resist patterning. The results are shown in Figure 1. Both 95°C and 65°C bake temperatures for 5 minutes showed no clearing of the gold when immersed in gold etch (even though it appeared the resist had developed fully when viewed optically). It was determined that the best possible processing conditions were to simply allow the resist to dry for at least 15 minutes at room temperature. Clearly the higher the temperature the less clearing of resist was achievable, and so no etching was possible.

Examination of this more quantitatively allowed us to determine the operating window to use with this type of paper-based substrate. Figure 2 shows the result of experimentation using a range of bake temperatures and exposure doses for a minimum bake time to eliminate tackiness to the paper (if the paper was tacky it would still pattern but became significantly damaged due to unfavourable adhesion during the contact alignment lithographic process). It is apparent that above 70°C, it is not possible to pattern the resist. Below this temperature, patterning is possible, but the exposure dose tends to have to be increased over that seen on silicon substrates. Also it is noted that even in this operating window, an increase in temperature means an increase in required dose. The samples showed better definition of smaller features when allowed to dry under ambient conditions. Figures 3a/b shows the importance of the bake choice as the sample goes from tacky to stable. It is also worth noting that the air-dried samples were stable for long periods of time with little degradation, even over periods of many days (as long as the samples were kept in a dark environment). Also, it can be seen that the air-dried samples gave a reduction in feature size over those even with low temperature bakes. This could be compensated for in any mask design process. Even low increases

in bake temperature were found to show that a higher dose was required to clear the resist, and this subsequently lead to an apparent increase in side wall angle.

A more detailed examination of the air-dried samples can be seen in Figure 4. This clearly depicts how the operating window shifts compared to that seen on standard substrates. For comparison, this window is 70–90 mJ/cm^2 on silicon. In the under-exposed region, clearing of the resist is less uniform and the features are less well defined as they have an apparent higher degree of edge roughness and increased variability in uniformity. In the over exposed region the features have increased in size and are clearly no longer a good copy of the original mask set. Grossly over-exposed ultimately means the features are no longer individual but joined together. Also, it shows on paper that it is possible to use standard positive resist to good effect with no adverse bake process, which is an advantage in situations which require low substrate deformation or suffer adverse temperature effects.

Examination of the etching process also required some optimisation. For a 5 nm chromium / 60 nm gold bilayer, the gold etch process was found to be slightly longer than that seen on silicon substrates (approximately 1.5x). Also, due to the nature of the gold etch being iodine based, it was found that, unsurprisingly, the paper absorbed the etchant to give a stained appearance. Chromium etching produced an apparent longer etch time to that seen on standard substrates. The increases in etch time are believed to be down to a more complex interaction between the paper structure and the metallic films. At this stage electrical measurements could verify that there was no conductivity between etched regions and non-etched regions, therefore proving that the devices had been isolated. However, there was still at this stage discolouration of the paper, which may have aesthetic issues depending upon the final application. However, the final step for removal of the resist layer was found to also remove >95% of the discoloration.

Having defined the process windows, the next stage was to demonstrate the possibility for the optimised technique to fabricate microscale features on the paper substrates. Figure 5a shows specific arrays of features defined using the optimum bake procedure. Clearly feature sizes of the order of a micron are possible with very little optimisation of the process. Also, the uniformity across the sample is surprisingly good, and samples were easily produced that showed little variation across a 75 mm wide section of paper.

In Figure 5b, lithographically defined metal structures made following wet etch and resist removal are shown. As can be seen, while there is some reduction in absolute resolution compared to those made on a silicon substrate with more edge and surface roughness, we can achieve a resolution of better than 1 micron with careful process control.

In order to verify the potential for fabrication over large areas, it is important to view the structures over such an area as would be appropriate for real devices, or batches of devices. Typical low magnification images of our samples are presented in Figure 6. These clearly show that while there are a few defects, the method works over a large area to give excellent definition. We found that over a 75 x 75 mm sample with a number of 15 mm x 15 mm defined squares of lithographic features, we were able to obtain good resolution. This is important for the potential application of the technique for making large scalable devices.

The samples were further examined using an SEM. Typical images can be seen in Figure 7. Of note, it can be seen that there is good contrast between the substrate and metal structures, suggesting that good selective etching has been achieved. There are some bright items in the channels in places, but there is no evidence from electrical testing that these were not isolated electrically and there was no evidence of leakage at voltages in excess of 5V. However, we do note that for eventual fabrication of transistors, such features could adversely affect device performance, and this is under further investigation. Also, there appears to be excellent edge definition showing that the patterning process is good, even on a rough substrate such as paper, and therefore offers huge potential for device fabrication. Furthermore, there is little defect or damage evidence, suggesting a scalable technique which is robust prior to any flexure of the samples. The central region of the ring features is less pronounced in the SEM, possibly suggesting some over-etching. However, profilometry measurements showed no specific evidence of this, although they did show some swelling of the substrate producing a slight out of plane deformation of the order of a few 100's of nm.

Examination of the electrical properties of the thin films showed that there was little difference in bulk resistance measurements between paper, glass, PEN and silicon, with the resistance being 2-3 ohms. This variation is understandable when considering the different surface roughness. However, roughness effects are expected to dominate once devices are made smaller [29]. We also demonstrate that individual structures are electrically isolated and that our patterned features are still conductive. A series of samples were fabricated to look at feature size and electric properties. We found no evidence of conduction leakage down to our minimum fabricated line separation of 2 microns.

Electrical testing showed that there was no change in the electrical properties of the gold surface, but that where the samples were etched there was no evidence of current leakage suggesting the process worked well. A four point probe measurement gave a sheet resistance of 1.57 ohm / square. This then gives a resistivity of 1.02×10^{-7} ohm-cm, which compares well to the bulk gold value of 2.5×10^{-8} ohm-cm.

Determination of reproducibility on paper substrates for a given device architecture was made. As expected there was more variation than seen in common microelectronic grade substrates, as well as the values being higher. This we believe is attributed to the domination of interfacial effects between the devices and the substrate on the thickness scale used. The results showed that there was a 7% standard deviation variation in results for a given sample set of 20 devices. Clearly, before scale up more in-depth examination is required. Furthermore, a check for anisotropic effects due to the paper fabrication process was made. We designed a simple structure with a central electrode which then fanned out as a number of individual conductive tracks at 30 degree varying angles (similar to the spokes from a bicycle wheel). Each spoke should give the same electrical resistance presuming no anisotropy effects. The resistance measurements showed that there are no noticeable variations outside those seen in measuring a number of different wires. This means we can have confidence that there are no induced effects caused by processing the paper during its fabrication or roll processing. More detailed analysis of this will be part of a future publication.

We then looked at the effect of track width and length for our process. A simple theoretical model would expect a linear relationship between length and resistance, with an inverse relationship between resistance and width for devices. As shown in Figure 8, the measured experimental data

does follow the trend but it appears that there is some deviation for longer track lengths or thinner wires. This can be explained by the fact that interfacial effects will become more dominant at these dimensions. The longer the wire the greater chance for defects caused by the rough surfaces acting on the sample. Similarly as the wires are decreased in width a defect may be found to dominate the full track width. Further examination will be investigated in future work which will look at the true scalability of the process for circuit applications.

Also demonstrated is the possibility to develop individual circuits on both sides of the paper. We looked at the effect of bulk circuit leakage by patterning a series of capacitive structures with an electrode on both sides of the paper. In this case we used photolithography to define the overlap region on the front side of the paper and more coarse features on the rear. It should be noted that we did not attempt to optimise the process on the rear but wanted to simply show the promise of dual side device fabrication. The capacitance measurements showed that we had a dielectric constant of 5.2, which is of the order of the expected value. There was no evidence of leakage and the devices scaled linearly with overlap area as expected.

Finally, the reliability and robustness of the devices on paper were examined. Initial measurements were made by cycling the devices around a radius of curvature of 10 mm and repeat measurements were made to see any variation in electrical conductivity. An initial SEM image of the wires is shown in Figure 9a, with the electrical test results in Figure 9b. This clearly shows that there are some small changes in the resistance of the measured sample. SEM imaging (Figure 9c – specifically down the central region of the image) showed that some cracks in what appears to be the coating on the sample surface occurred from tight bending, suggesting different paper types may offer further improvement. However, what it does show is that it is possible to bend the devices to a fixed shape and that electrically there was a less than 1% change in performance, which is within the error of the measurements made.

Figure 10 shows more flex testing using an automated clamping stage system. This was set to give a radius of curvature of approximately 5 mm at the centre of wire tracks. This work was repeated on 3 separate devices. A couple of main factors were observed. Firstly, if the radius of curvature was decreased to less than 5 mm, there was an increased risk of damage to the devices, which is important to consider when thinking of applications. Secondly, at the radius of curvature of 5mm there was fatigue in the sample followed by total failure when making the sample undergo repeat flexures. Initial changes were found after 1000 – 2000 flexes, with failure around 4000 flexes. Further examination would suggest that this failure was due to the cracking of the paper coating. This would suggest that for cyclic applications it may be essential to either coat a top layer on the paper or to look at alternative papers, as discussed in [1].

A further robustness test was done in order to look at the adhesion properties of the films. This was examined firstly in terms of any effect by manhandling of the substrates, and then secondly by using an industrial quantitative technique. It was found that by simple manhandling of the samples, there was no obvious effect on the quality of the films in terms of either electrical or physical appearance. However, a tape-test showed delamination of a number of devices (Figure 11). It is possible that this delamination is only an issue for certain applications, and certainly there appeared to be no evidence of delamination during normal device operation. Also, the damage does appear to show delamination of the paper interlayers rather than simply being down to the adhesion of the metal to

the paper. It is possible that other paper types may offer an improvement in adhesion properties, if they are not be damaged by layers separating, and this is currently under further investigation.

Finally, it is important to discuss how the technique of performing photolithography on paper is useful, scalable and commercially viable. For example scaling electrodes down means devices such as transistors can operate at a higher frequency. In terms of scale up, sputter coaters are now widely available for deposition using a R2R process. Therefore, the deposition of the metal layer is possible on rolls of paper, which offers a potentially vast range of material choices than is available by printing.

Similarly, highly uniform resist coating has been demonstrated by R2R compatible techniques, for example techniques such as blade coating have been demonstrated. The fact that baking is not required may well simplify the process, although timings may have to be considered. Etching is also feasible by using R2R with either spray etching or dip tanks. More information in R2R processing can be found for example in refs [30-31]

For the exposure process, it would be expected in the short term that samples may have to be sectioned from a roll and a batch process used. However, significant work and progress is being made in the plastic electronics industry to develop direct write technologies, which should be applicable.

While there are still some challenges for achieving a full R2R photolithographic process, these are being examined in the plastic electronics industry. The clear advantage of device feature size reduction for improved performance and density is highly appealing. Similarly, being able to use paper as a substrate has a number of advantages as well as interesting applications over those seen using plastics. Beyond the environmental, recyclability and cost implications, it offers the possibility of devices which are more appealing for certain applications. Initially, such applications are expected to be high volume, low cost, disposable and probably involving commercial packaging or visual based devices.

Conclusion

In conclusion, we have demonstrated for the first time a novel photolithographic technique for selective patterning of metal layers on commercial glossy photo paper substrates. Our process is compatible with standard silicon processing utilising a reduced bake temperature. It shows no degradation of this type of paper and has potential to at least be compatible with all such paper types as well as offering guidance for other paper types. The process has far reaching applications, particularly in the consumable packaging sector. Using lithography will allow the potential improvement of device performance on paper-based materials giving scope for more cheap applications. Similarly, there is the potential to tailor this work to paper types which are again expected to yield performance and resolution enhancement. The application of this technique also offers the potential for production of lift-off based techniques and nanoimprint defined features which will again offer further possible applications. Our devices, when compared to those produced on silicon and glass will show some reduction in performance, but this is not an issue depending on the potential application. Finally, it has been demonstrated how robust paper-based devices can be for general use. This work is of significant importance as it will allow further development of devices on a paper-based substrate. It also demonstrates that although lithography is possible on paper, it

requires a good understanding of lithographic etch processes and process control. This means that developmental work on devices is feasible in standard facilities / laboratories without the need for capital outlay on specific equipment. Also, it will easily allow direct comparison with a multitude of device architectures. This is ultimately expected to open a myriad of applications and new devices. It will bring additional functionality to a high proportion of everyday items. This highlights the fundamental importance of our findings on paper-based photolithography and the potential for future exploitation.

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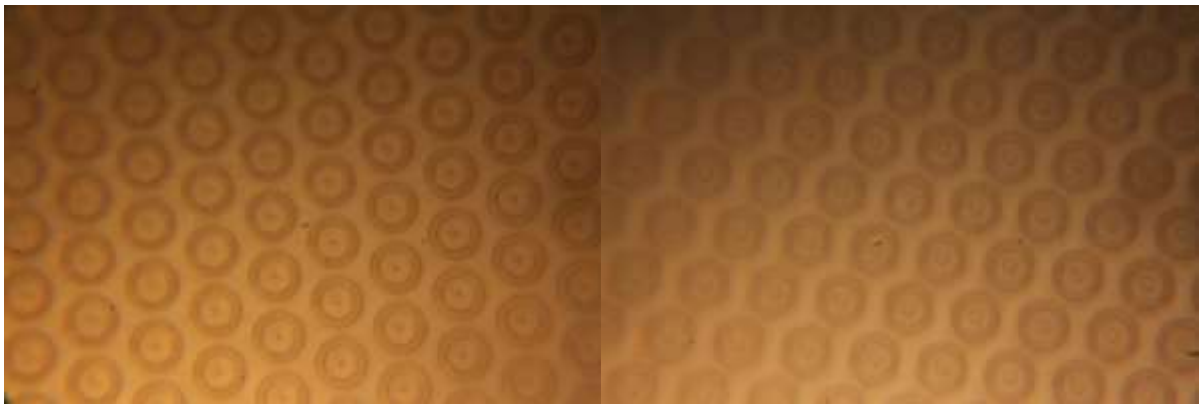


a) *b)*

c)

Figure 1 Comparative photolithographic patterning as a function of pre exposure bake temperature; taken at 50x magnification a) 95°C 5 minutes, b) 65°C 5 minutes , c) room temperature (20°C) 15 minutes [Each ring is of the order of 1-2 microns in width].

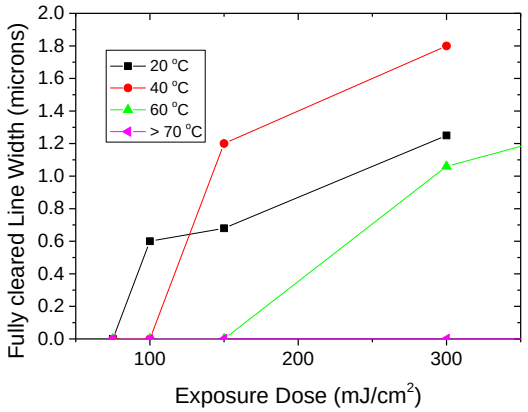
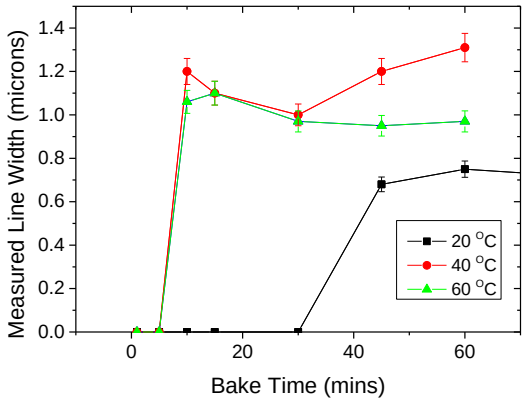
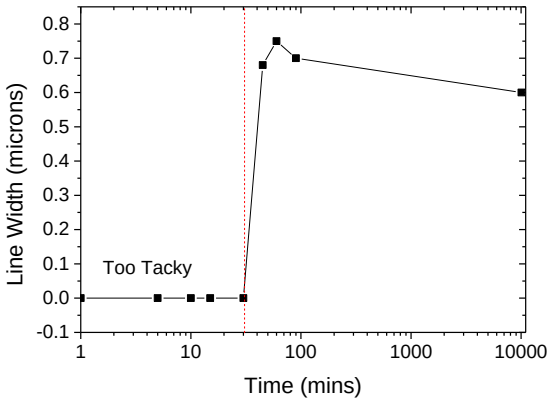


Figure 2 Examination of the patterned line width as a function of exposure dose for a range of bake temperatures.



a)



b)

Figure 3 Examination of bake time effects on line width a) for range of bake temperatures which were found to clear the resist on development b) over longer time period for 20 °C baked samples.

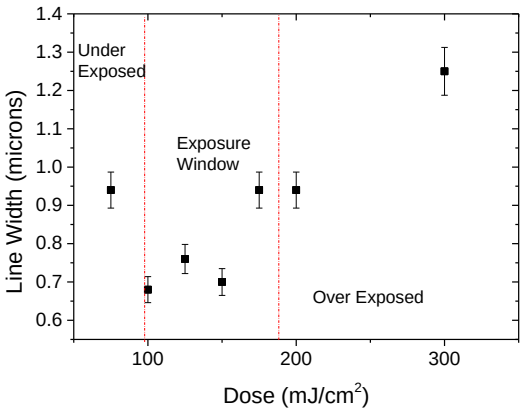
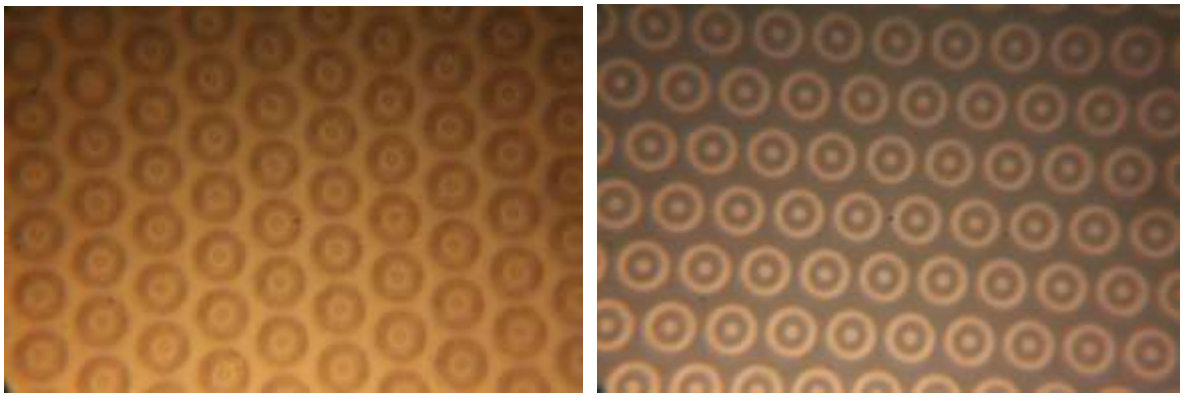


Figure 4 Dose test examination of feature line width on air dried samples.

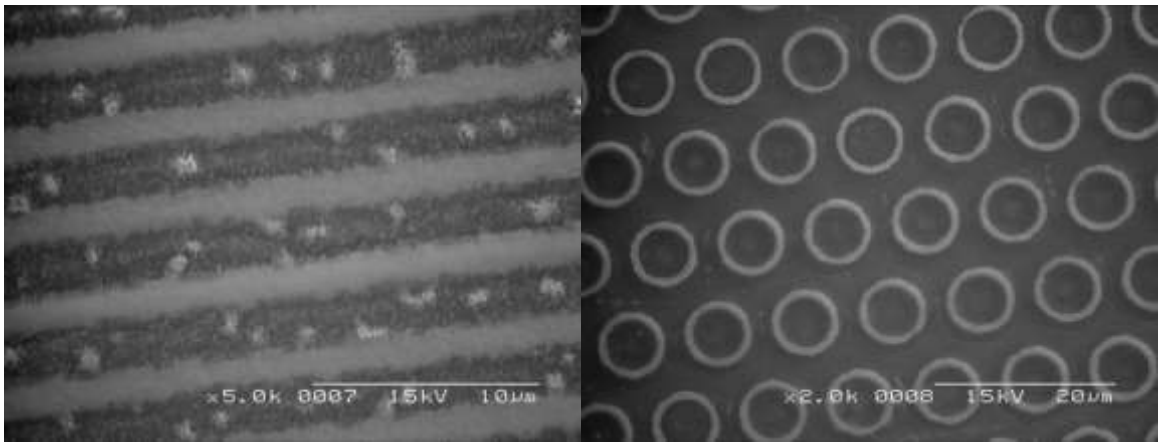


a) b)

Figure 5 Examination of optimised process for typical features – in this case ring structures of 10 micron diameter with a 2 micron line width: a) post development, and b) post etch and resist removal.

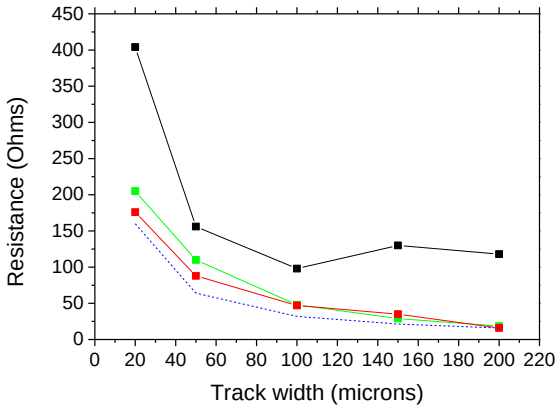
a) *b)*

Figure 6 a) 5x magnification image across 2 mm region on a typically defined array of features patterned on the Epson paper b) photograph of 75 mm sample of multiple arrays of features under flexure.

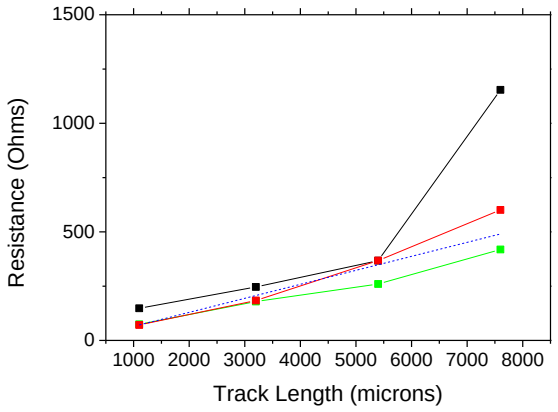


a) b)

Figure 7 Typical SEM images of chromium/gold features fabricated using optimum lithography on paper a) wires b) rings.

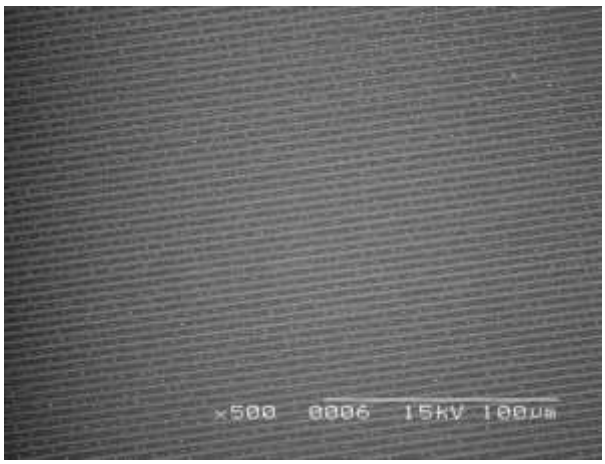


a)

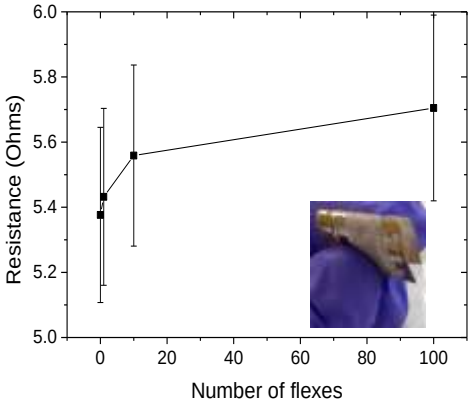


b)

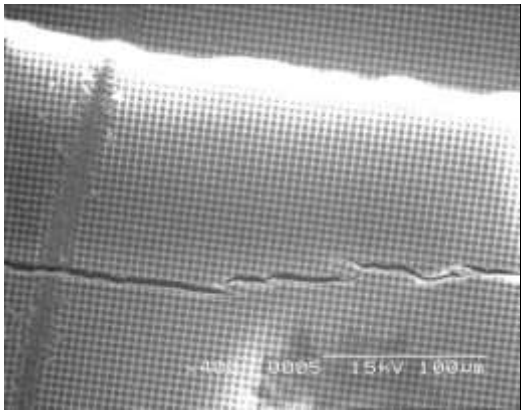
Figure 8 Examination of resistance change as a function of a) track width and b) track length for gold microscale patterned wire. Three sample sets are measured with the blue line a guide for the expected trend in the data from theoretical calculations.



a)



b)



c)

Figure 9 a) SEM image of lithographically patterned wires on paper b) electrical measurements of wire as a function of flexing c) typical damage caused during flexing examined using SEM.

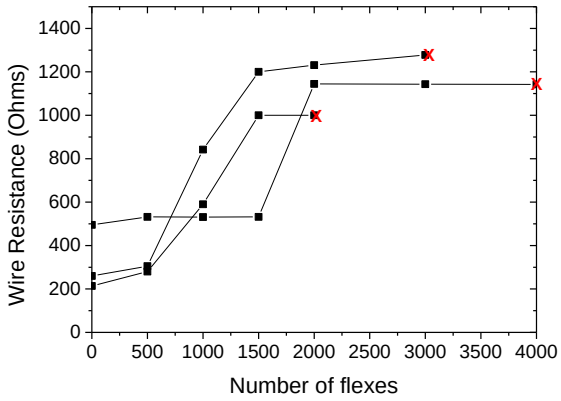


Figure 10 Automated cyclic testing of micro fabricated wires.

a) *b)*

Figure 11 Tape test examination of metal adhesion on paper substrates a) pre-tape test and b) post-tape test.