Fault Tolerant Five-Leg Converter Topology with FPGA-based Reconfigurable Control

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***Abstract*— Fast fault detection and reconfiguration of power converters is necessary in electrical drives to prevent further damage and to make the continuity of service possible. On the other hand, component minimized converters may provide the benefits of higher reliability and less volume and cost. In this paper, a new fault tolerant converter topology is studied. This converter has five legs before the fault occurrence, and after fault detection the converter continues to function with four legs. A very fast fault detection and reconfiguration scheme is presented and studied. Simulations and experimental tests are performed to evaluate the structure requirements, the digital reconfigurable controller and fault detection scheme. For experimental tests, the control and the fault detection and reconfiguration schemes are implemented on a single FPGA chip. Experimental and simulation results show the effectiveness of the proposed fault tolerant topology and its FPGA-based control.**

***Index Terms*— Five-leg converter, Open-switch fault, Fault tolerant control, Fault detection, Field Programmable Gate Array.**

I. Introduction

Electrical machines employed in AC motor drive systems are usually fed by Voltage-Source Inverters (VSI), fed in many applications by controlled rectifiers. This type of drive system is sensitive to faults occurring in the rectifier or the inverter. Any failure in one of the power switches decreases the system performance and its effect can lead to hard failure. Therefore, when the fault occurs, the drive operation has to be stopped for an unforeseen maintenance. This is not acceptable in safety-critical cases where the continuous operation of system is a must. Examples of such systems are some processes in the military, aerospace and automotive industries like steering, fuel pumps and brake-by-wire systems [1-3]. To prevent unscheduled shutdown, real-time fault detection and converter reconfiguration schemes for power converters must be implemented.

In order to have a suitable response to a fault in one of the semiconductor devices, the first step is fast detection of the fault and its location. This is the subject of many earlier researches. Fault detection in a multilevel converter is studied in [4, 5]. A detection method for faults in IGBT switches based on gate signal monitoring is presented in [6]. Average values of three-phase currents are processed in [7] to detect an open-switch fault in a doubly-fed wind power converter. Open-circuit faults in matrix converters are studied in [8]. Nonlinear observers are used in [9] to detect open-switch faults in induction motor drives. Another method for detection of open-switch faults in voltage source inverters feeding AC drives based on analyzing the load currents is presented in [10]. In our earlier contribution [11, 12], a very fast detection scheme is proposed, using a "time and voltage criterion" which can detect and locate a fault in a few microseconds.

Once the fault and its location are detected, appropriate changes must take place in the converter topology. Several schemes are proposed as fault tolerant topologies for power converters. A survey of different fault tolerant structures is provided in [13]. In [14] an additional inverter leg replaces the faulty leg by using bidirectional switches. In [1] a hardware reconfiguration is presented which is realized by connecting the neutral point of the machine to the middle point of the DC-link capacitor. The proposed hardware reconfiguration presented in [15] is based on the connection of the DC-bus middle point to the phase which was linked to the faulty leg before its isolation. A fault tolerant three phase ac/ac converter is proposed for machine-supply application that uses three additional bidirectional switches [16]. In this topology after a fault, the 6-leg back to back converter becomes a 5-leg converter.

On the other hand, component minimized converters have been studied in a large number of papers in recent years [17, 18, 19]. These converters may provide the benefits of higher reliability and less volume and cost. One of these structures is the so-called five-leg converter [17]. This converter has been proposed in applications like independent control of two three-phase electrical machines [17, 18], component minimized AC/DC/AC converter [19] and 6-leg fault-tolerant converter [16]. It is also mentioned in [19] that in cases where input and output frequencies are the same, the five-leg converter is an

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interesting replacement for the six-leg converter. Some examples of such applications are some uninterruptable power supplies and AC/DC distributed power applications. Therefore, the use of this topology might lead to reduction in complexity of the converter while providing the possibility of controlling two sides of the converter with a single controller, therefore reduction in costs. Overall, it is possible to see that this converter can be interesting as a fully controllable bidirectional AC/DC/AC converter.

Another component minimized converter is the four-leg converter which has been studied in few papers. In [20] a form of this converter has been suggested for an AC/AC conversion system. In [21] all the three possible structures of the four-leg converter are studied and the suitability of this converter is approved. It is shown that when the input and output frequencies are the same, reduction of the required DC-link voltage is possible. For a four-leg converter in the two cases out of three, one leg is shared between the two sides of the converter and one input or output phase is connected to the middle point of the DC-link. In the third case, both sides have a connection to the middle point of the DC-link [20].

In this paper, a new fault tolerant converter topology is presented which is tightly related to the five-leg and four-leg converters. In fact, before the fault occurrence, the converter is a five-leg converter. After an open-switch failure, using a corresponding triac, the structure is changed to the four-leg converter. Then an FPGA-based fault detection and reconfigurable control for this proposed topology is presented. Thanks to its parallel architecture, FPGA can run its tasks very quickly. Therefore, this type of digital target appears very suitable for implementation of the fault detection scheme. Besides, the high performance of FPGA for many power electronic and drive applications has been proved [22]. Moreover, by implementing both fault detection and converter control units on a single FPGA chip, the cost will be decreased.

In the following, in section II, a general overview of fault tolerant systems is presented. Then, in section III, for the proposed fault tolerant five-leg converter, all three possible cases of reconfiguration are considered and studied in detail. Fault detection method and reconfiguration control scheme are explained in section IV. For verification, first simulations are carried out using Matlab/Simulink. Then experimental tests are realized. The fault tolerant converter was built in our laboratory and the controller and fault detection scheme are implemented on an FPGA target and tested experimentally.

It is shown that in all cases of open switch faults, the studied detection scheme can detect the fault very quickly; the reconfigurable digital controller operates well before and after a fault occurrence, and the fault tolerant converter continues to supply the load even with an open circuit fault in one of the semiconductor switches.

II. FAULT TOLERANT SYSTEMS

In case of fault occurrence in sensors, actuators or other parts of a complex system, conventional systems may have undesirable performance. In applications where the need for safety, reliability and fault tolerance is high, it is necessary to anticipate the fault tolerance ability against unpredicted faults to increase the reliability and availability of the system while providing an acceptable performance. These types of systems are known as Fault Tolerant Systems (FTS). In other words, a fault tolerant system can maintain its stability and acceptable performance after a fault occurrence whereas the performance of the system in normal and post-fault conditions may be different. In the first case, the emphasis is on the quality of the system performance, whereas in the later case, the most important issue is to achieve a stable and acceptable (probably degraded) performance.

Fault tolerant systems are composed of different blocks. A Fault Detection and Isolation (FDI) unit is the most essential part of any fault tolerant system. Its duty is to detect the fault occurrence, find its location and its magnitude. Once the fault is detected, suitable reaction must be performed in order to have acceptable performance in the system. Fig. 1 shows general fault tolerant system architecture. Upon the fault detection, the Fault Tolerant Control (FTC) block makes the suitable changes in the references, the controller and the system.

An FTS may be based on redundancy or not. In an FTS with redundancy, a redundant part will replace the faulty one, after fault detection and upon reconfiguration. In this case, by correctly designing the FTS, the same operation capability can be achieved after a fault occurrence. However in some cases, some degree of performance degradation is accepted. In these cases, a suitable reconfiguration might be enough to assure the minimum required performance. In Fig. 1, the redundant part and its switching mechanism are shown with dashed bounds, because they might be missing in some FTSs without redundancy.

After fault detection and isolation, a reconfiguration is necessary. Reconfiguration is required in both hardware and software parts of the system. Reconfiguration in the software part is consisted of modifying the references and the controller characteristics, if necessary. All required control signals are generated by the fault tolerant control block.

Fig. 2 shows the studied FTS. The system is composed of a three-phase electrical source and a three-phase load, with a

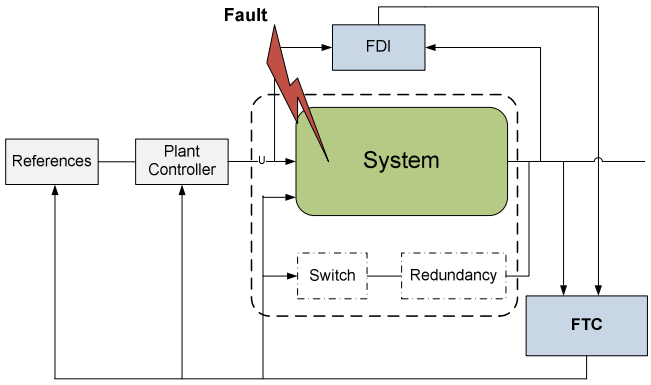

Fig. 1. Fault tolerant system.

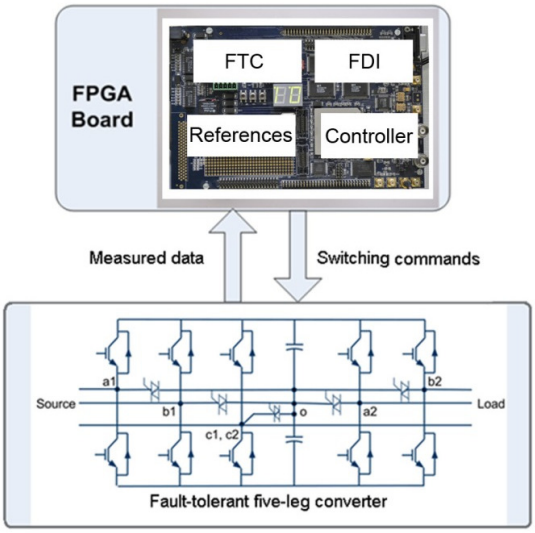

Fig. 2. Studied fault tolerant system.

fault tolerant five-leg converter between them. In this system, no redundant parts are used. Implementation is done on a single FPGA to assure very fast fault detection and reconfiguration. Hardware reconfiguration (converter) is done using additional triacs, which make it possible to change the structure from a five-leg converter to a four-leg one. Software reconfiguration is applied in the PWM generation unit, to generate the suitable switching commands as explained in the following.

III. Fault Tolerant Five-Leg Converter Topology

A. *The proposed fault tolerant structure*

The five-leg converter is studied in a few papers and different control schemes are proposed for it. It is shown that this converter is able to produce two sets of independent voltages to be used in applications like supplying two three-phase motors or loads, or AC/AC conversion systems. This converter has superior characteristics compared to other component-minimized topologies like nine-switch converter and half-bridge-based converters and its use might lead to lower capital cost compared to the conventional back to back converter [17]. However, like other conventional converters, this converter is also sensitive to the faults in its semiconductor devices. Therefore, if a five-leg converter is going to be used in an application that continuity of service or fault tolerance is important, fault compensation ability is mandatory.

To overcome this problem, a fault tolerant five-leg converter is proposed, studied and verified in this paper. This topology is not reported in the literature before. Also in order to have a fast and efficient transition after the fault occurrence, a reconfigurable control is presented for this proposed structure, which is explained later in detail. This proposed topology is shown in Fig. 3. It is consisted of a conventional five-leg converter and five additional bidirectional switches, placed between each leg and the middle point of the DC-link.

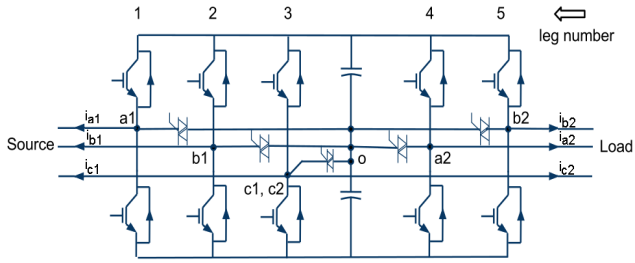

Fig. 3. Proposed fault tolerant five-leg topology.

Triacs are used as bidirectional switches in this study. The triacs should tolerate a voltage at least equal to $V_{dc}/2$ in normal operation of the converter, where V_{dc} is the DC-link voltage. When a triac is switched on, the phase current will pass through it. Five additional voltage sensors are necessary for fault detection. In normal operation, all triacs are switched off and the converter operates like a normal five-leg converter. However after an open-switch failure, the fault detection algorithm finds the location of the faulty switch, stops the faulty leg switching commands and triggers the corresponding triac. The converter is studied in more detail in normal and faulty conditions in the following.

B. *Pre-fault operation (five-leg converter)*

Before the fault occurrence, all triacs are switched off and the converter operates as a normal five-leg converter. Among the several PWM approaches for this topology, it seems that the suggested method in [17, 23] that uses all 32 possible voltage vectors of a five-leg converter, produces less voltage harmonics and is simpler and better suited for practical implementation. In this method a so called "double zero-sequence injection method" is used. Fundamental voltage reference signals v'_{ij} $(i = a, b, c\,; j = 1, 2)$ for both three-phase sides are calculated using methods like field oriented control or voltage oriented control [24, 25]. Then, for each three-phase reference, a zero sequence signal (ZSS) is added to this values to form the modulation signals (1). In fact ZSS does not change the output line-to-line and phase voltages, therefore it is used as a degree of freedom to reduce the current harmonics and improve the DC-bus utilization [17]. Here, the voltage references at the source-side are computed to have a DC-link regulation with unity power factor of the input currents, and the load-side voltage references are set to be balanced sinusoidal ones.

$$v_{ij}(t) = v'_{ij}(t) + v_{zsj}(t) \qquad (1)$$

This is repeated for both sets of three-phase voltage references. Since we have 6 voltage references and only 5 legs, a reduction in the number of voltage references is necessary. Reduction in the number of voltage references is done in [26] using an inverse lookup table. In [17], this is done by adding another ZSS in accordance to the converter configuration in five-leg mode. This method is used here. For the healthy operation of the five-leg converter shown in Fig. 3, the five voltage references are calculated as :

$$\begin{aligned} v_1 &= v_{a1} + v_{c2} \\ v_2 &= v_{b1} + v_{c2} \\ v_3 &= v_{c1} + v_{c2} \\ v_4 &= v_{a2} + v_{c1} \\ v_5 &= v_{b2} + v_{c1} \end{aligned} \quad (2)$$

where $v_1$to v_5 are the corresponding voltage references for legs 1 to 5.

Since the same signal is added to all three reference values of each side, it does not affect the fondumental output voltage on that side. Fig. 4 shows the principle of this method.

In the PWM block, the gating signals are generated by comparing the voltage references with a high frequency triangular carrier. It can be shown that in this case, the pulsewidths τ_i $(i = 1\ to\ 5)$ corresponding to the switching commands of the upper switch of the converter legs are equal to:

$$\tau_i = \left(\frac{1}{2} + \frac{v_i}{V_{dc}}\right) T \quad (3)$$

where T is the switching period.

C. *Post- fault operation (four-leg converter)*

After a fault occurrence, the detection scheme will localize the fault and stop the switching commands of the faulty leg switches and then will trigger the corresponding triac. Therefore after the reconfiguration, the converter will continue to work with only four healthy legs. It should be noted that based on the location of the fault, three different post-fault topologies are possible. For all of them, in a similar manner to PWM for five-leg converter, the control of four-leg converter using proper ZSS injection is possible. However, for each structure of four-leg converter, a different ZSS injection is required.

Case 1: let's consider that the fault occurs in one of the two "input legs" (leg 1 or 2). In this case and after the fault, the reconfiguration will take place by connecting the corresponding input phase to the middle point of the DC-link,

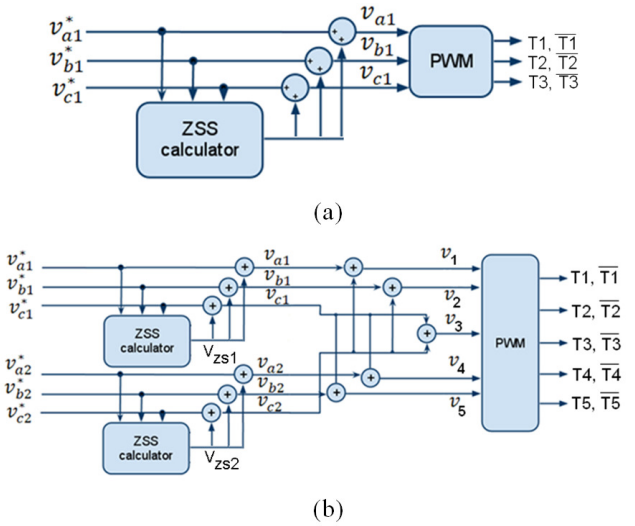

Fig. 4. Principle of PWM module for (a) a three-leg converter, (b) for the 5-leg converter with leg "3" shared between two sides (as shown in Fig. 3).

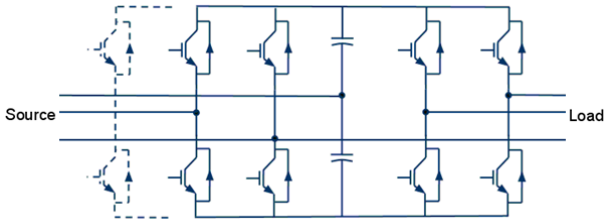

Fig. 5. Reconfigured topology when the leg 1 is faulty.

as is shown in Fig. 5 for a fault in the leg 1. Considering that the voltage references for the source side and the load side are respectively (v_{a1}, v_{b1}, v_{c1}) and (v_{a2}, v_{b2}, v_{c2}), using a ZSS addition method based on the method proposed in [16, 17], new voltage references for legs 2 to 5 are calculated as below, in which the new voltage references are marked by asterisks:

$$\begin{aligned} v_2^* &= v_{b1} - v_{a1} \\ v_3^* &= v_{c1} - v_{a1} \\ v_4^* &= v_{a2} - v_{c2} + v_{c1} - v_{a1} \\ v_5^* &= v_{b2} - v_{c2} + v_{c1} - v_{a1} \end{aligned} \quad (4)$$

These voltages are the inputs of a PWM unit, which will provide the switching commands for the legs 2 to 5. For a fault in the leg 2, similar method will be used to calculate the new voltage references for the legs 1, 3, 4 and 5. Fig. 6 shows the principle of new voltage reference generation for the PWM unit in the case of a fault in leg 1.

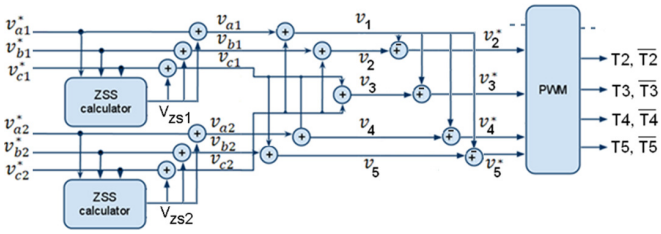

Fig. 6. Principle of PWM and new reference voltage generation for the four healthy legs after a fault in the leg 1.

Case 2: we consider now a fault occurring in the common leg. After triggering the corresponding triac, the structure will be changed to a four-leg converter consisting of two half bridge converters. Fig. 7 shows the converter topology in this case. This converter is well studied in the literature and different control schemes are available for it [20]. In a simple approach, using a ZSS addition, new voltage references are calculated by:

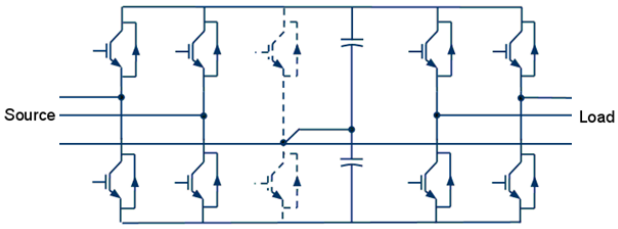

Fig. 7. Reconfigured topology when the common leg is faulty.

$$\begin{aligned} v_1^* &= v_{a1} - v_{c1} \\ v_2^* &= v_{b1} - v_{c1} \\ v_4^* &= v_{a2} - v_{c2} \\ v_5^* &= v_{b2} - v_{c2} \end{aligned} \quad (5)$$

Case 3: let's consider now a fault occurring in one of the two output legs (leg 4 or 5). In this case, by triggering the suitable bidirectional switch, one of the load phases will be connected to the middle point of the DC-link after fault detection. This is shown in Fig. 8 for a fault in the leg 5. New voltage references for legs 1 to 4 are calculated as below:

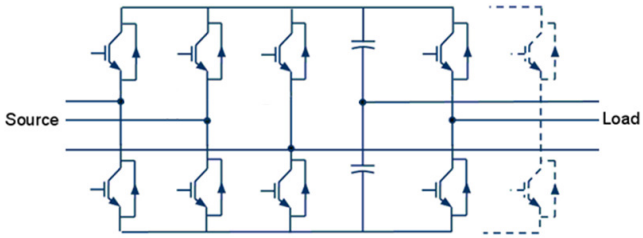

Fig. 8. Reconfigured topology when the leg 5 is faulty.

$$\begin{aligned} v_1^* &= v_{a1} - v_{c1} + v_{c2} - v_{b2} \\ v_2^* &= v_{b1} - v_{c1} + v_{c2} - v_{b2} \\ v_3^* &= v_{c2} - v_{b2} \\ v_4^* &= v_{a2} - v_{b2} \end{aligned} \quad (6)$$

Similar method will be used to calculate the new voltage references in the case of a fault in the leg 4. It should be noticed that this case is somehow similar to case 1.

A general form of the reconfigured voltage reference generation and PWM can be explained as a flowchart as shown in Fig. 9. The required input data are five voltage references for the five legs of the converter and the fault's location.

It is obvious that after the fault detection, not only the structure, but also the control system must be changed. In fact, in healthy or faulty cases, the controls of both converters are not the same and must be changed as quickly as possible to avoid any discontinuity or transient in the currents. FPGAs are good candidates for the fulfillment of this requirement, as they can execute quasi-instantaneously these tasks [11]. Therefore, in this paper, control and fault detection schemes are implemented into a single FPGA, as explained later in part IV.

D. Voltage production capability

It should be noted that in all fault cases, the voltage production capability of the four-leg converter may be lower than that of the five-leg converter. Therefore either the DC-link voltage in the post-fault converter should be initially high enough (or it could be increased) to maintain the same capability of the pre-fault converter, or the post-fault converter can operate with a reduced power level to assure the balanced operation of the drive until the maintenance. Table I presents the maximum producible voltages by the converter in five and four-leg modes. In this table, $V_1$and V_2 represent the amplitudes of the phase voltages at the two AC sides of the converter. The provided results are obtained by considering the inequalities between the DC-link voltage and the voltages

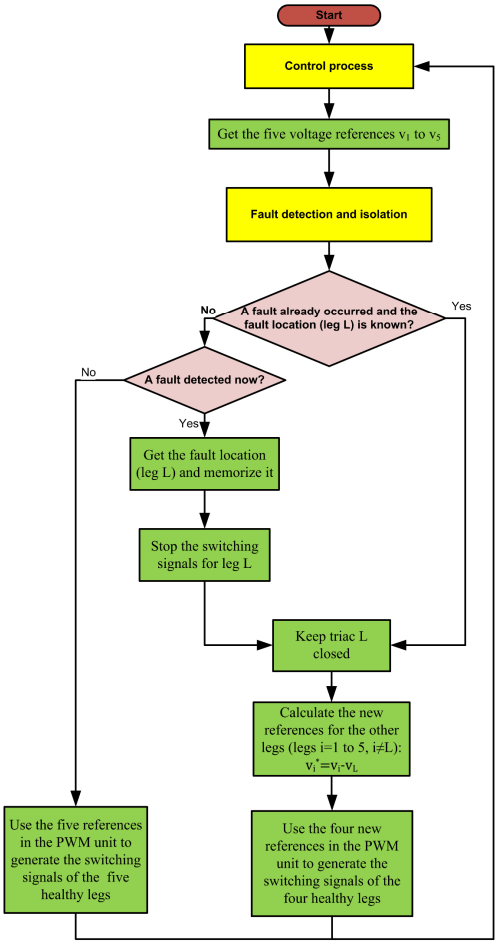

Fig. 9. The generalized reconfigured voltage reference generation and PWM.

at the two sides of the converter, which must be satisfied for converter controllability. As an example for the studied reconfigured converter at case 3 (Fig. 8), it is possible to form the mentioned inequalities and it can be verified that the limiting criteria is as:

$$|v_{a1o}| < V_{dc}/2 \quad (7)$$

$$v_{a1o} = v_{a1} - v_{c1} + v_{c2} - v_o = v_{a1n_1} - v_{c1n_1} + v_{c2n_2} - v_{on_2} \quad (8)$$

where n_1, n_2 are the neutral points at two sides of the converter. From (8) it may be concluded that in this case:

$$\sqrt{3}V_1 + \sqrt{3}V_2 < V_{dc}/2 \quad (9)$$

For the other cases, same calculations can be easily made to obtain the voltage production capabilities, as it is provided in table I [16, 21].

TABLE I
VOLTAGE PRODUCTION CAPABILITIES

Pre-fault (five-leg)	$V_1 + V_2 < V_{dc}/\sqrt{3}$
Post fault (four-leg) case 1	$V_1 + V_2 < V_{dc}/\sqrt{3}/2$
Post fault (four-leg) case 2	$V_1, V_2 < V_{dc}/\sqrt{3}/2$
Post fault (four-leg) case 3	$V_1 + V_2 < V_{dc}/\sqrt{3}/2$

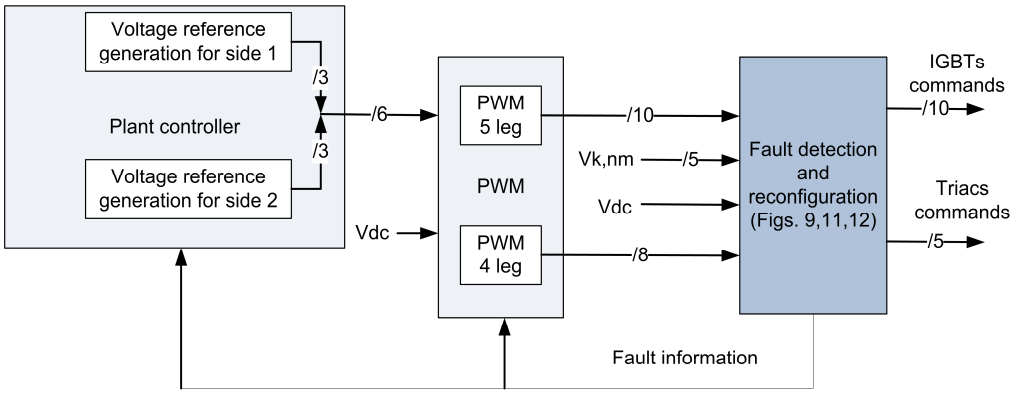

Fig. 10. Proposed reconfigurable control.

After reconfiguration, the switches currents will remain the same, and the current of faulty phase will pass through the capacitors of the DC-link.

IV. Fault Detection and Reconfigurable Control

A reconfigurable control structure is necessary for the proposed fault tolerant converter. The reconfigurable control structure is shown in Fig. 10. It is consisted of two voltage reference generation units, the "fault detection and compensation" unit and two PWM units for five-leg and four-leg modes. The core of this structure is the "fault detection and reconfiguration unit". Its role is to detect the fault and its location, and to send the appropriate switching commands to the switches and the triacs. The four-leg PWM generation unit uses the voltage references and the fault's location to calculate the suitable gate signals for the switches in post-fault converter, as explained in section III.C.

In the "fault detection and compensation unit", fault is detected based on the difference between measured and estimated pole voltages. These voltages are shown in Fig. 11 by V_{ko} where $k \in \{a_1, b_1, c(c_1, c_2), a_2, b_2\}$ are the middle points of the converter legs and "o" is the middle point of DC-link (see Fig. 3). $V_{ko,m}$ indicates the measured pole voltages, while $V_{ko,es}$ shows the estimated values of pole voltages.

Here open circuit faults are studied. The estimated voltages are calculated based on the switch commands and the DC-link voltage. The switching command for the upper switch of the leg k is shown as T_k in Fig. 11. $T_k = 0$ indicates that the switch is commanded to be open, whilst $T_k = 1$ means that the switch is commanded to be closed. The switch commands in each leg are complementary.

Because of the non ideal behavior of drivers and switches, there will be always delays and dead times, which means that the estimated and measured pole voltages are not always equal, even in normal operation of converter. Therefore two adjustments have been used: a comparator is used to determine if the difference between the measured and estimated voltages is large enough to be considered as an error and a time criterion is also used to compensate for delays and dead times in the system. This is shown in Fig. 11 for the leg k. The error signal is observed in a time window, and if it is always greater than a constant value (h) for a long enough time (N period), then one can be sure that there is a fault. This observation time should be longer than the overall delay caused by the sensors, drivers, controller and switches to prevent false fault detection. Fig. 12 shows the state diagram of the fault detection scheme that is implemented on the FPGA.

It is worth mentioning that although only open circuit faults are discussed here, short circuit faults in IGBTs can be detected as well by using fast acting fuses in series with each IGBT. In fact in this protection scheme, a short circuit fault will finally result in an open circuit condition, as it is explained and experimentally approved in [27]. Therefore the fault can be effectively detected. On the other hand, in our detection approach the IGBT's failure is realized for the set of "driver+switch". Therefore once a fault in a driver or in a switch is occurred, the "driver+switch" cannot perform the desired action, and the fault must be detected. Since the effect is the same for fault detection, nothing differentiates the failure in the driver from that in the switch. In another words, it is not important if the fault has occurred in the driver or in the switch itself. Therefore a fault in the driver will be detected as well.

V. Simulation Results

Simulations are carried out using Matlab/Simulink in order to verify the behavior of the proposed fault-tolerant converter. The converter is placed between a three-phase source and a three phase load. The source side voltage references are calculated from a source-voltage oriented control scheme that tends to control the DC-link voltage with a unity power factor at the point of connection to the source [28]. A three-phase RL

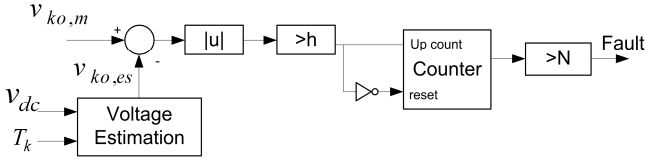

Fig. 11. Fault detection scheme.

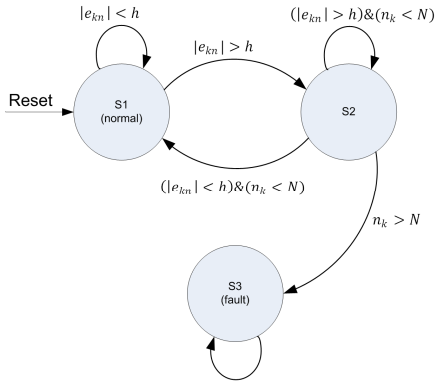

Fig. 12. State diagram of the fault detection scheme.

impedance is placed between the source and the converter. Load side voltage references are sinusoidal balanced three phase voltages. System parameters are provided in Table II. Simulations are done for all three possible cases of fault.

Case 1: in this case, an open switch fault is applied at the leg 1. Fig. 13 shows the output of the counter (Fig. 11) after the fault occurrence. N is considered to be equal to 32, to be large enough to prevent any false fault detection. This value is actually calculated based on the delay times of the real system, which is later introduced in part VI. Also in this figure, the input current $i_{a1}(t)$ of the phase "a1" is provided, to clarify the effect of the fault and converter reconfiguration on this current. Fig. 14 shows the input current of the phase "a1" which was connected to the faulty leg, and also the output current $i_{b2}(t)$of the leg 5 before and after the fault. The moment of fault occurrence is shown with a vertical dashed line. It can be seen that the converter continue to work normally.

TABLE II
SYSTEM PARAMETERS

Source side	Source voltage: 50 Hz, 60 V_{l-l} Input impedance: $R_f = 0.4\Omega$, $L_f = 3mH$
DC-link	Capacitance: 2200 μF
Load side	V_{ref}=50 V_{l-l} 60 Hz, $R_l = 2.75\Omega, L_l = 9mH$
Fault detection parameters	N=32 ; h= 20 V
Switching frequency	8 kHz

One can notice that the THD of source-side (input) current is increased after reconfiguration. One way of explaining this behaviour is by analyzing the applied voltage waveforms on the load and source sides and by observing their harmonic contents. Fig. 15 shows the phase voltages at the two sides of converter for case 1.

$V_{k_i n_i}$ $(k \in \{a,b,c\}, i \in \{1,2\})$, are the phase voltages at the two sides of the converter. As it is visible, after the reconfiguration, the voltage waveforms at the faulty side are changed and have more harmonics, since the phase voltages

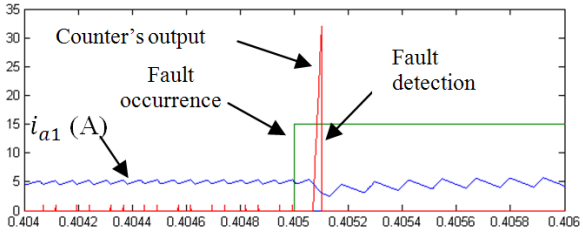

Fig. 13. Zoomed view of the fault detection- case 1.

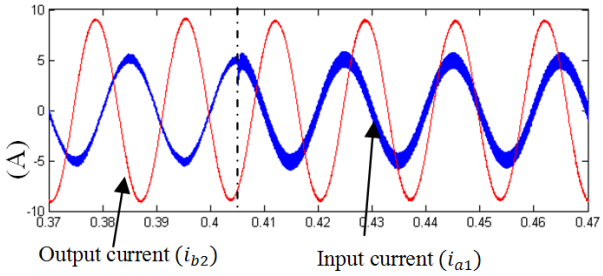

Fig. 14. Faulty-leg current and output current- case 1.

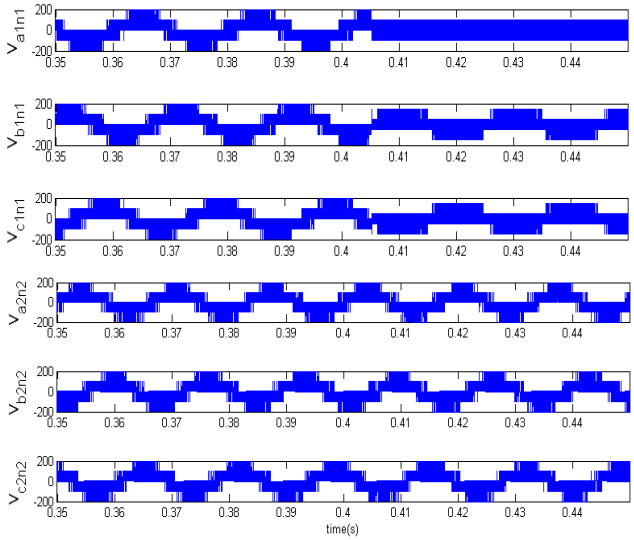

Fig. 15. Phase voltages (V) at the two sides for a fault at t=0.405 s- case 1.

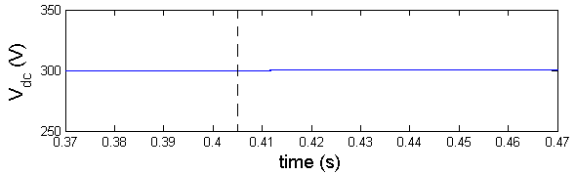

Fig. 16. DC-link voltage- case 1.

have no longer a five-step form, and have only 3 or 4-step forms. Therefore after the reconfiguration, more harmonics will appear in the faulty side phase voltages. This leads directly to more harmonics in the corresponding currents. However, since in our study the priority is continuous service and fault tolerance, the slight increase in THD is not a major concern.

DC-link voltage waveform is shown in Fig. 16, which shows that this voltage is well controlled after the

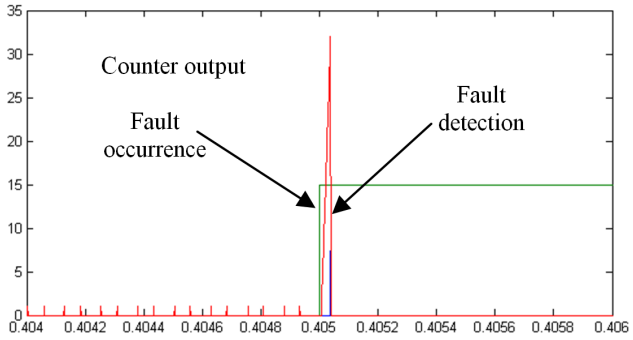

Fig. 17. Zoomed view of the fault detection-case 2.

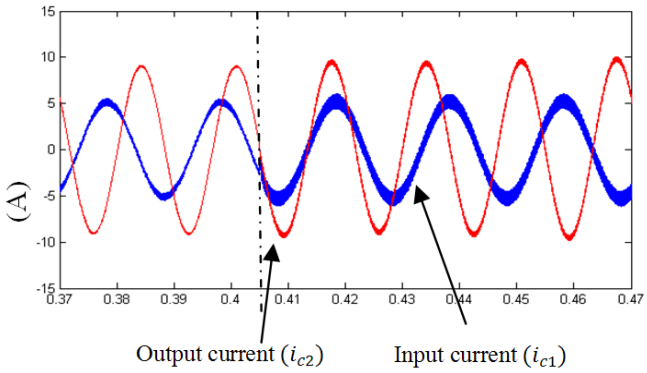

Fig. 18. Current of the input and output phases connected to the faulty leg-case 2.

reconfiguration as well.

Case 2: when a fault happens in the common leg, the reconfiguration of the Fig. 7 takes place upon the fault detection. In this case, the fault detection signal and the counter's output are shown in Fig. 17. In Fig. 18 the currents of the input and output phases which are connected to the common leg before and after the fault are given. DC-link voltage is shown in Fig. 19. Again the converter is not affected by this fault.

Case3: when the fault occurs in one of the output phases, the reconfiguration of the Fig. 8 takes place after the fault detection. Fig. 20 shows the fault detection process. Fig. 21 shows the current of the input current $i_{a1}(t)$ and the current of the output phase which was connected to the faulty leg ($i_{b2}(t)$). DC-link voltage is shown in Fig. 22. Again like two previous cases, in this case the converter is able to continue to supply the load after fault detection and reconfiguration.

Therefore it can be concluded that in all cases, the fault tolerant five-leg converter is able to supply the load after the occurrence of an open switch fault in one of its switches.

VI. Experimental Results

An experimental set-up, given in Fig. 23, is used in order to evaluate the performance of the studied fault tolerant five-leg converter. Fault detection and control schemes for this converter are implemented on a single FPGA. The FPGA implementation procedure is explained briefly here, and the

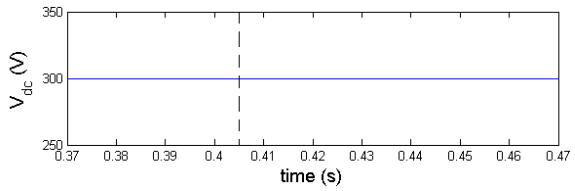

Fig. 19. DC-link voltage- case 2.

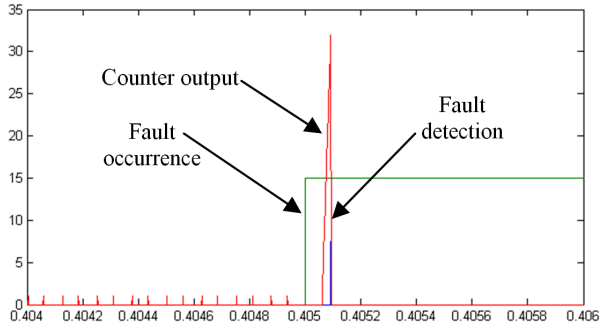

Fig. 20. Zoomed view of fault detection time- case2.

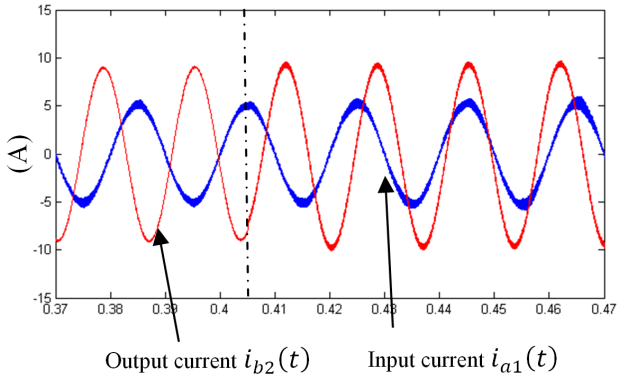

Fig. 21. Input phase current $i_{a1}(t)$ and faulty leg current $i_{b2}(t)$.

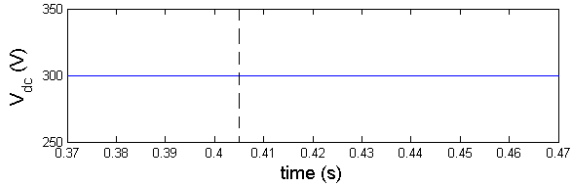

Fig. 22. DC-link voltage- case 3.

details are available in our earlier publications [11, 29, 30]. After the discrete simulations with Simulink, simulation with Altera DSP Builder blocks are performed. Simulink blocks are replaced with proper DSP Builder blocks and for the exchange of data between DSP Builder and Simulink blocks, proper input/output blocks are used. Using DSP Builder allows us to have visual programming and to translate it to HDL form very easily. The VHDL design is later compiled using Quartus software and uploaded on the Altera FPGA board via a Joint Test Action Group (JTAG) interface. Here, a Stratix DSP S80 development board is used, which includes the Stratix EP1S80B956C6 FPGA chip. This chip contains 79,040 programmable logic elements. The development board has an on-board 80-MHz oscillator.

In the experimental set-up, the same component values as in

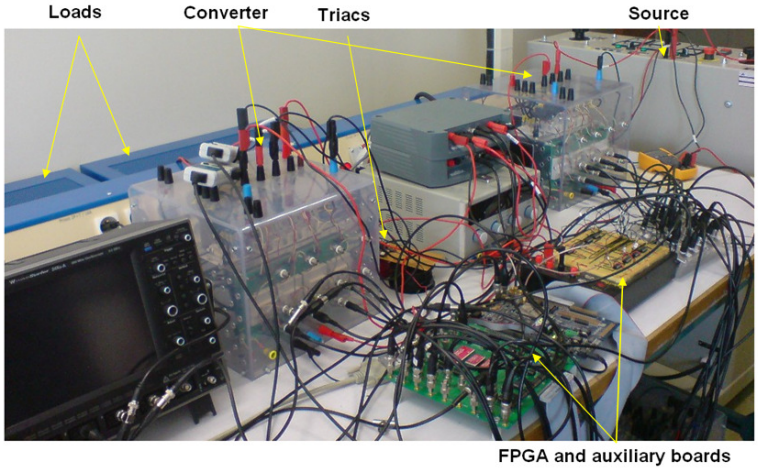

Fig. 23. Experimental setup.

the simulations are used, and the switching frequency is equal to 4 kHz. The IGBTs are SKM50GB123D which are commanded by SKHI22A drivers. A 2200 μF capacitance is placed at the DC-link. Side 1 of the converter is connected to a three-phase sinusoidal source via a three phase inductance of 3 mH and resistance of 0.4 Ω. A three-phase RL load with minimum resistance of 2.75 Ω and inductance of 9 mH is connected to the Load side of the converter. N=30 is chosen for fault detection, so the detection time is equal to 30 μs . This value is chosen to be sufficiently larger than all delays in the control loop, still small enough to make possible fast fault detection. The open switch fault is applied by cutting the diver commands to the switch.

Experiments are performed for all three possible cases of failure. First, a fault in a source side phase is considered (case 1). A fault is applied in the leg 1 of the converter. Fig. 24 shows a zoomed view of the fault occurrence moment and its detection as well as the faulty-phase's current. Fault is detected quickly. Fig. 25 shows the currents of the triggered triac, the leg 1 (input current) and the leg 4 (load current). A zoomed view of the Fig. 25 is provided in Fig. 26. Clearly the converter can continue its operation after fault detection and reconfiguration with minimum affection from the fault.

Harmonic analysis of the converter currents in this case showed that the THD of the faulty phase current (i_{a1}) is increased from 2.91% to 4.29%, while no significant changes in the THD of other legs is registered.

Fig. 27 shows the essentials waveforms for fault detection. The estimated voltage $V_{a_1 o,es}$ can be obtained from the switching command T_1 and the DC-link voltage. The up-counter output which is used for fault detection (see Fig. 11) is shown in this figure as well. This up-counter's output is provided using one of the digital to analog converters of the development board. In faulty operation of the converter when the difference between the measured and estimated pole voltages is large enough, the counter's output starts to increase and when it reaches N=30, a fault is declared. It should be remarked that the low-amplitude peaks in the counter's waveform are correctly not considered as a fault.

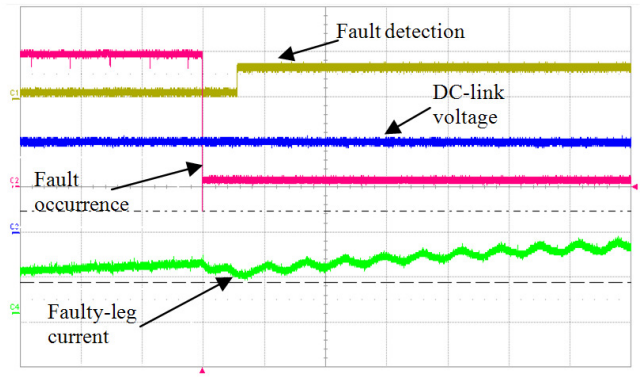

Fig. 24. Fault detection in case 1- from top to bottom: fault- fault detection- DC voltage (100V/div)- faulty phase current (5A/div)-time scale:200 μs/div.

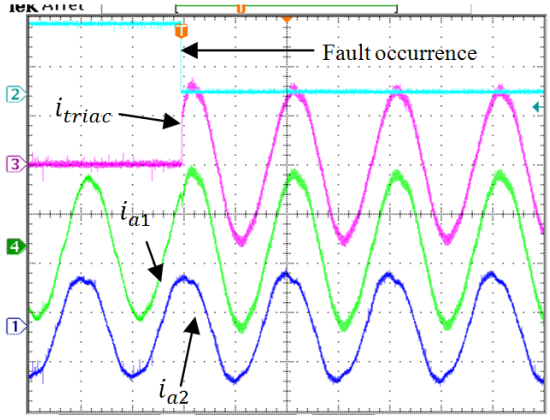

Fig. 25. Fault detection in case 1- from top to bottom: fault- triac current (5A/div)- faulty phase current (5A/div)– load current (5A/div)-time scale: 10ms/div.

For the second case, which is a fault in the common leg, the tests are repeated and the resulted waveforms are shown in Figs. 28 and 29.

Fig. 28 shows the currents of the input and output phases which are connected to the common leg, as well as the current of the corresponding triac. Fig. 29 shows the fault detection signals in case 2. The fault detection and reconfiguration is

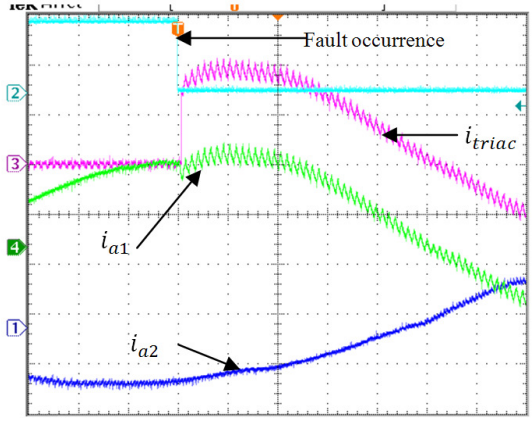

Fig. 26. Fault detection in case 1, zoomed view- from top to bottom: fault- triac current (5A/div)- faulty phase current (5A/div)– load current (5A/div)- time scale:1ms/div.

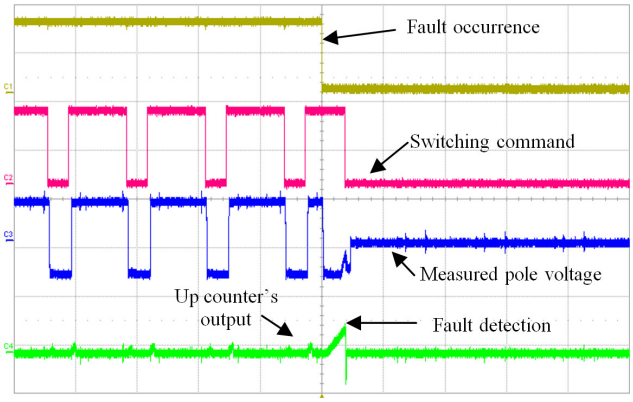

Fig. 27. Fault detection signals in case 1- from top to bottom: fault occurrence- switching command T_1- measured pole voltage $V_{a1o,m}$ (200V/div)- up-counter's output in the detection block. Time scale: 100 μs/div.

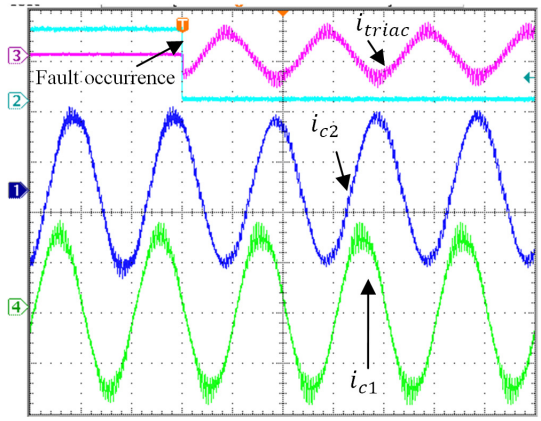

Fig. 28. Fault detection in case 2- from top to bottom: fault- triac current (20A/div)- faulty phase current (5A/div)– source current(10A/div)- time scale: 10ms/div.

effective in this case as well. The THD for i_{c1} and i_{c2} is increased slightly from 3.55% and 3.45% to 4.16% and 7.28% respectively.

Finally for a fault in the load side (case 3), the experimental results are shown in Figs 30 and 31. Here the fault is applied to the leg 5. Currents of the output phase which was connected to this leg (i_{b2}) and the leg 1 which is an input phase, as well

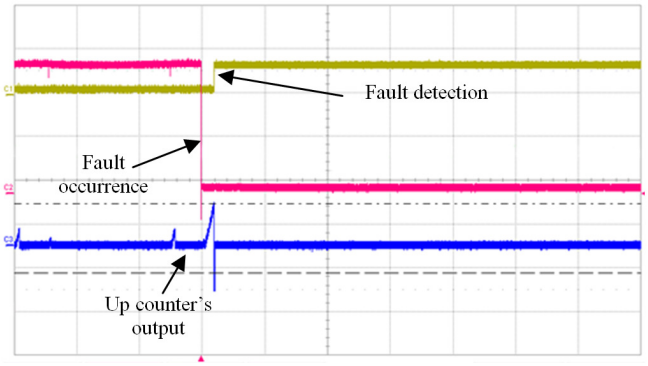

Fig. 29. Fault detection in case 2-from top to bottom: fault- fault detection- up-counter's output in the detection block. Time scale: 200 μs/div.

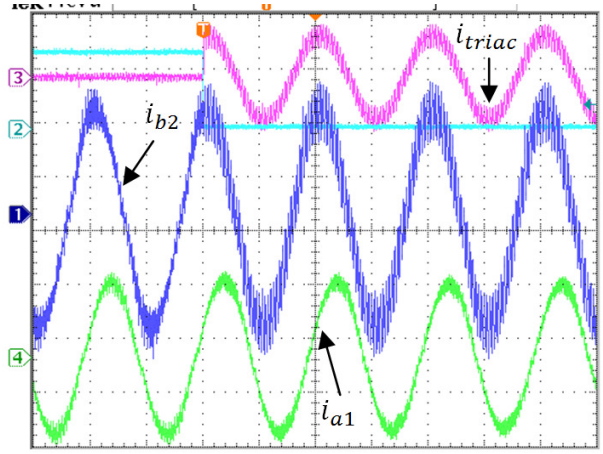

Fig. 30. Fault detection in case 3-from top to bottom: fault- triac current (5A/div)- faulty phase current (2A/div)– load current (5A/div)- time scale: 10ms/div.

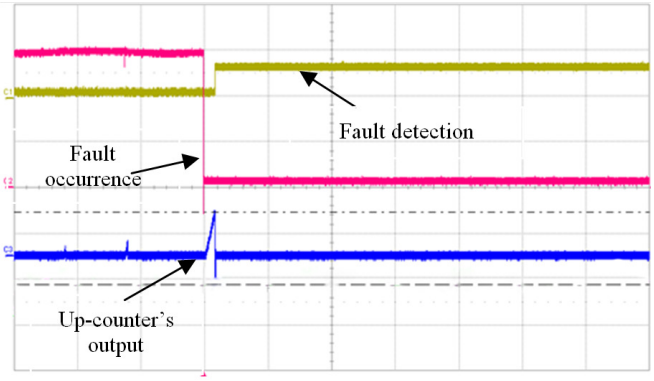

Fig. 31. Fault detection in case 3-from top to bottom: fault- fault detection- up-counter's output in the detection block. Time scale: 200 μs/div

as the current of the corresponding triac are provided in Fig.30. Fig. 31 shows the detection signals in this case. It is visible that once again, fault detection and reconfiguration is fast and effective. Again in this case, the THD of the faulty phase is increased after reconfiguration. THD of i_{b2} is increased from 4.40% to 9.74%, while the THD of i_{a1} is remained constant (3.28% to 3.27%). THD of the other load phase (i_{a2}) shows only a slight increase from 4.83% to 5.63%.

Based on these experimental results, it can be concluded that fast fault detection and smooth reconfiguration is possible

for this fault tolerant topology, and that the converter can continue supplying the load for a balanced operation, even after an open-switch fault in one of its switches. The THD of the faulty phase may increase after reconfiguration, but since the most important aspect here is the continuity of service and fault tolerance, the slight increase in the currents THD is not a major concern.

VII. Conclusion

Five-leg converter is an interesting component minimized converter, however it is sensible to a failure in one of its semiconductor switches. In this paper, a fault tolerant five-leg converter is proposed which will continue to operate with four legs after an open-switch fault. An FPGA-based reconfigurable control is proposed for this topology. In the proposed method, it is possible to implement both the control and the fault detection tasks on a single FPGA chip. Using this approach, fast detection and reconfiguration is possible, and an increase in the cost of system due to the use of two digital targets is avoided. For evaluation, first all possible cases of fault are studied and the simulated using Matlab/Simulink. Then the fault detection and then the proposed reconfigurable control schemes are implemented on an FPGA board and fully experimental tests are carried out to evaluate the effectiveness of the proposed topology and its control for all three possible cases. Simulation and experimental results show that the fault tolerance is achieved and that the converter can continue to supply the load in all cases.

References

[1] A. M. S. Mendes and A. J. M. Cardoso, "Fault-tolerant operating strategies applied to three-phase induction-motor drives," IEEE Transactions on Industrial Electronics, vol. 53, pp. 1807-1817, Dec 2006.

[2] B. A. Welchko, T. A. Lipo, T. M. Jahns, and S. E. Schulz, "Fault tolerant three-phase AC motor drive topologies: A comparison of features, cost, and limitations," IEEE Transactions on Power Electronics, vol. 19, pp. 1108-1116, Jul 2004.

[3] M. H. Kim, S. Lee, and K. C. Lee, "Kalman predictive redundancy system for fault tolerance of safety-critical systems," IEEE Transactions on Industrial Informatics, vol. 6, pp. 46-53, 2010.

[4] A. Yazdani, H. Sepahvand, M. L. Crow, and M. Ferdowsi, "Fault Detection and Mitigation in Multilevel Converter STATCOMs," IEEE Transactions on Industrial Electronics, vol. 58, pp. 1307-1315, 2011.

[5] P. Lezana, R. Aguilera, and J. Rodríguez, "Fault detection on multicell converter based on output voltage frequency analysis," IEEE Transactions on Industrial Electronics, vol. 56, pp. 2275-2283, 2009.

[6] M. Rodriguez, A. Claudio, G. Vela-Valdes, P. Sibaja-Teran, L. Hernandez-Gonzalez, and J. Aguayo-Alquicira, "A failure detection strategy for IGBT based on gate voltage behavior applied to a motor drive system," IEEE Transactions on Industrial Electronics, vol. 58 , pp. 1625–1633, 2011.

[7] P. Duan, K. Xie, L. Zhang, and X. Rong. 2011, “Open-switch fault diagnosis and system reconfiguration of doubly fed wind power converter used in a microgrid,” IEEE Transactions on Power Electronics, vol. 26, pp. 816-821, 2011.

[8] S. Cruz, M. Ferreira, A. Mendes, and A. J. M. Cardoso, "Analysis and Diagnosis of Open-Circuit Faults in Matrix Converters," IEEE Transactions on Industrial Electronics, vol. 58, pp. 1648–1661, May 2011.

[9] D. Campos-Delgado and D. Espinoza-Trejo, "An Observer-Based Diagnosis Scheme for Single and Simultaneous Open-Switch Faults in Induction Motor Drives," IEEE Transactions on Industrial Electronics, vol. 58, pp. 671-679, 2011.

[10] W. Sleszynski, J. Nieznanski, and A. Cichowski, "Open-transistor fault diagnostics in voltage-source inverters by analyzing the load currents," IEEE Transactions on Industrial Electronics, vol. 56, pp. 4681-4688, 2009.

[11] S. Karimi, A. Gaillard, P. Poure, and S. Saadate, "FPGA-Based Real-Time Power Converter Failure Diagnosis for Wind Energy Conversion Systems," IEEE Transactions on Industrial Electronics, vol. 55, pp. 4299-4308, Dec 2008.

[12] S. Karimi, P. Poure, and S. Saadate, "FPGA-based fully digital fast power switch fault detection and compensation for three-phase shunt active filters," Electric Power Systems Research, vol. 78, pp. 1933-1940, Nov 2008.

[13] D. U. Campos-Delgado, D. R. Espinoza-Trejo, and E. Palacios, "Fault-tolerant control in variable speed drives: a survey," IET Electric Power Applications, vol. 2, pp. 121-134, Mar 2008.

[14] R. L. D. Ribeiro, C. B. Jacobina, E. R. C. da Silva, and A. M. N. Lima, "Fault-tolerant voltage-fed PWM inverter AC motor drive systems," IEEE Transactions on Industrial Electronics, vol. 51, pp. 439-446, Apr 2004.

[15] W. Sae-Kok, D. M. Grant, and B. W. Williams, "System reconfiguration under open-switch faults in a doubly fed induction machine," IET Renewable Power Generation, vol. 4, pp. 458-470, Sep 2010.

[16] C. B. Jacobina, R. L. D. Ribeiro, A. M. N. Lima, and E. R. C. da Silva, "Fault-tolerant reversible AC motor drive system," IEEE Transactions on Industry Applications, vol. 39, pp. 1077-1084, Jul-Aug 2003.

[17] M. Jones, S. N. Vukosavic, D. Dujic, E. Levi, and P. Wright, "Five-leg inverter PWM technique for reduced switch count two-motor constant power applications," IET, Electric Power Applications, vol. 2, pp. 275-287, 2008.

[18] Y. Kimura, M. Hizume, and K. Matsuse, "Independent vector control of two PM motors with five-leg inverter by the expanded two-arm modulation method," in European Conference on Power Electronics and Applications, 2005.

[19] C. B. Jacobina, I. S. de Freitas, E. R. C. da Silva, A. M. N. Lima, and R. L. D. A. Ribeiro, "Reduced Switch Count DC-Link AC-AC Five-Leg Converter," IEEE Transactions on Power Electronics, vol. 21, pp. 1301-1310, 2006.

[20] E. Ledezma, B. McGrath, A. Munoz, and T. A. Lipo, "Dual AC-drive system with a reduced switch count," IEEE Transactions on Industry Applications, vol. 37, pp. 1325-1333, 2001.

[21] C. B. Jacobina, I. S. de Freitas, and A. M. N. Lima, "DC-Link Three-Phase-to-Three-Phase Four-Leg Converters," IEEE Transactions on Industrial Electronics, vol. 54, pp. 1953-1961, 2007.

[22] E. Monmasson, L. Idkhajine, M. N. Cirstea, I. Bahri, A. Tisan, and M. W. Naouar, "FPGAs in Industrial Control Applications," IEEE Transactions on Industrial Informatics, vol. 7, pp. 224-243, May 2011.

[23] D. Dujic, M. Jones, S. N. Vukosavic, and E. Levi, "A General PWM Method for a (2n + 1)-Leg Inverter Supplying n Three-Phase Machines," IEEE Transactions on Industrial Electronics, vol. 56, pp. 4107-4118, 2009.

[24] R. Bojoi, P. Guglielmi, and G. M. Pellegrino, "Sensorless direct field-oriented control of three-phase induction motor drives for low-cost applications," IEEE Transactions on Industry Applications, vol. 44, pp. 475-481, 2008.

[25] J. R. Rodríguez, J. W. Dixon, J. R. Espinoza, J. Pontt, and P. Lezana, "PWM regenerative rectifiers: State of the art," IEEE Transactions on Industrial Electronics, vol. 52, pp. 5-22, 2005.

[26] P. Delarue, A. Bouscayrol, and E. Semail, "Generic control method of multileg voltage-source-converters for fast practical implementation," IEEE Transactions on Power Electronics, vol. 18, pp. 517-526, Mar 2003.

[27] F. Abrahamsen, F. Blaabjerg, K. Ries, H. Rasmussen, "Fuse Protection of IGBT’s against Rupture", IEEE Nordic Workshop on Power and Industrial Electronics, pp. 64-68, 2000.

[28] M. Malinowski, "Sensorless control strategies for three-phase PWM rectifiers," Ph.D thesis, Warsaw University of Technology, Poland, 2001.

[29] S. Karimi, P. Poure, and S. Saadate, "An HIL-Based Reconfigurable Platform for Design, Implementation, and Verification of Electrical System Digital Controllers," IEEE Transactions on Industrial Electronics, vol. 57, pp. 1226-1236, Apr 2010.

[30] S.Karimi, A.Gaillard, P.Poure and S.Saadate, “Current sensor fault-tolerant control for WECS with DFIG,” IEEE Transactions on Industrial Electronics, vol. 56, pp. 4660-4670, 2009.

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