Improvement of Post-Fault Performance of Cascaded H-bridge Multilevel Inverter

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Abstract—**This paper is focused on improving the post-fault performance of Cascaded H-bridge Multilevel Inverters by decreasing the common mode voltage. First, an algorithm is proposed to determine the optimal post-fault state among all possible states which have the same maximum available voltage. Furthermore, a modified technique is proposed to calculate the references of inverter phase voltages under faulty conditions. This technique leads to a decrease in the common mode voltage when the required output voltage is less than its maximum value. These solutions are mutually employed in the post-fault control system.**

Simulation and experimental results confirm the effectiveness of the proposed solutions in comparison with the existing methods in different cases.

***Index Terms*— Cascaded H-Bridge Multilevel Inverter, Common Mode Voltage, Fault-Tolerant Inverter.**

NOMENCLATURE

n_i	Number of operative cells in each phase, $\forall i \in \{a,b,c\}$.
n_a-n_b-n_c	Operating state of CHB-MLI.
v_{ng}	Common mode voltage.
v_{ig}	Inverter phase voltages, $\forall i \in \{a,b,c\}$.
v_{in}	Output phase voltages, $\forall i \in \{a,b,c\}$.
g	CHB-MLI neutral point.
n	Load neutral point.
V_{mn}	Required output phase voltage amplitude.
$V_{p,max}$	Maximum available phase voltage amplitude in the faulty condition.
$V_{l,max}$	The maximum available line-line voltage amplitude in the faulty condition.
f	Output voltage fundamental frequency.
u_u, u_d	Upper and Lower boundaries of common mode voltage, respectively.

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I. INTRODUCTION

MULTILEVEL inverters are widely used in industry in many high power applications [1-3]. Among the conventional multilevel topologies [4-5], Cascaded H-Bridge Multilevel Inverter (CHB-MLI) is popular in high-power medium-voltage applications thanks to its modular structure [6-7]. Because of this modularity, it is possible to increase inverter reliability by using redundant cells, which become operative once the faulty cells are bypassed. Hence the inverter can continue working similar to its pre-fault condition.

However, if the number of redundant cells is increased in order to provide higher reliability, the cost will also significantly increase [8]. Furthermore, owing to the large number of semiconductors used in CHB-MLIs, these inverters are severely subjected to failure as a consequence of failure in semiconductors, driver circuits and/or DC-link electrolytic capacitors. Moreover, high-power applications of CHB-MLIs require service continuation even under faulty conditions. This so-called "fault-tolerance" is considered as an important specification for CHB-MLIs [9-11].

Fault detection is the first step to achieve fault-tolerance. Some fast and accurate methods are proposed in order to diagnose the malfunctioning cell (or cells) in CHB-MLIs [12-15]. In [12] a quick but complicated detection method is suggested, where the methods proposed in [13] and [14] are simpler and with acceptable detection time (less than one switching period). The method proposed in [15] is simple, however it is relatively slow and needs more than one fundamental period to detect the fault occurrence.

After fault detection, fault-tolerant schemes are required to guarantee inverter operation as close to normal operation as possible [16]. Some techniques are proposed in [17-22] to achieve this ability in CHB-MLIs. In these methods, after bypassing faulty cells, the goal is to reach maximum available balanced line-line voltages. To achieve this, a common mode voltage is added to all phase voltages, causing a shift in neutral point of the inverter. This technique is called the "Neutral Shift" (NS) method [17, 23]. Although the common mode voltage does not appear in output line-line voltages, it

can lead to unbearable voltage stress on the motor bearings and shaft (usually grounded), causing damage and aging [24]. Depending on the procedure of the reference voltage calculation to achieve balanced line-line voltages, the NS methods can be classified in two major groups: Vector-Based (VB) and Waveform-Based (WB) method [23].

Fundamental Phase-Shift Compensation (FPSC) post-fault algorithm is a VB method, where the modified phase voltages are obtained by using an offline phasorial calculation [20]. It is worth noting that these values are for maximum line-line voltage, and by decreasing the required line-line voltage, the magnitude of the phase voltages is proportionally decreased. The extended FPSC proposed in [19], is another VB method that resolves the conventional FPSC method's disadvantages such as having no solution or optimal solution in some faulty conditions.

Another set of the NS techniques are WB methods. The primary idea is proposed in [17-18], which is an extension of the peak reduction method used in normal condition. Another WB method, Geometric method, is based on the geometrical approach [21]. As shown in [23], WB methods provide higher maximum available voltage in comparison with VB methods, due to their peak reduction characteristic.

The Geometric method is more applicable owing to the higher maximum available voltage and unique solution for all faulty conditions. Despite common mode voltage's harmful effect on motor parts, the common mode voltage reduction has yet to be investigated. This may be due to the fact that the system is not to operate in faulty conditions for an extended period. Meanwhile common mode voltage reduction can be a plus and can be considered, especially if it does not need any additional sensors or measurements (costs).

Therefore, this paper focuses on improving the Geometric method, aiming to minimize common mode voltage injected to inverter phase voltages. The improvements are considered in two solutions. Solution I proposes an algorithm to choose the optimal post-fault state among all possible states which have the same maximum available voltage. Using the optimal state leads to generation of the maximum available voltage with the lowest common mode voltage. Solution II presents a modified algorithm to calculate the phase reference voltages in the post-fault condition. The advantage of using this solution in comparison with the Geometric method is that the common mode voltage is reduced when the required output voltage is less than its maximum value.

It is worth mentioning that in the post-fault control system, both solutions are involved. Solution I finds the optimal operating state for the faulty inverter. After that, Solution II generates the references of inverter phase voltages considering the required output voltage and the optimal state obtained by Solution I.

Simulation and experimental results are presented to verify the performance of the proposed methods.

This paper is organized in the following sections. In section II, operation of CHB-MLI under faulty conditions is investigated. In this section, after explaining CHB-MLI structure, the Geometric technique is described as a post-fault control method. The two mentioned solutions to improve the performance of CHB-MLI under faulty conditions are presented and explained in section III. Finally, an 11-level CHB-MLI prototype is implemented to verify the validity of the proposed methods' performance, and the results are shown in section IV. The paper is concluded in section V.

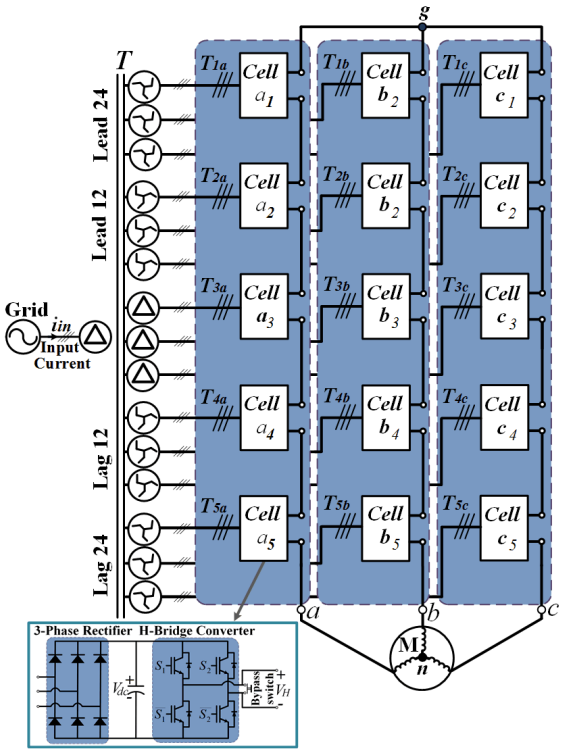

Fig. 1. An 11-level Cascaded H-bridge Multilevel Inverter.

II. Cascaded H-Bridge Multilevel Inverter Operation under Faulty Condition

A. Cascaded H-Bridge Multilevel Inverter Structure

In Fig. 1 an 11-level cascaded H-Bridge multilevel inverter with five cells in each phase is shown. Each cell is an H-Bridge inverter fed by a three-phase rectifier and multi-winding transformer in order to provide isolation between DC links. To minimize the system input current distortion, each set of the rectifier side windings of the transformer are designed to adjust the phase differences between two adjacent windings. This displacement angle (θ_d) depends on the number of cells in each phase (n) and is calculated by

$$\theta_d = \frac{60^o}{n} \tag{1}$$

For an 11-level CHB-MLI ($n = 5$), $\theta_d = 12^\circ$ as shown in Fig. 1. This type of transformer is called a "Phase-Shifted Transformer" and is explained in [25].

Each inverter phase voltage is a summation of its cells voltages. This voltage has a fundamental component with frequency f and is shown as $v_{ag,1}$, $v_{bg,1}$, and $v_{cg,1}$ for phase 'a', 'b', and 'c' respectively, and expressed by

$$v_{ig,1} = n_i\, m_i V_{dc}\, sin(2\pi f t + \varphi_i),\ \ \forall i \in \{a,b,c\} \tag{2}$$

where n_i is the number of cells, and m_i is the modulation index which is equal for all phases in normal operation. φ_i is the initial phase angle, and their difference is 120° for normal condition.

Considering V_{dc} as the base value, $v_{ig,1}$ can be re-written in per unit (p.u.) as:

$$v_{ig,1}[p.u.] = n_i\, m_i\, sin(2\pi f t + \varphi_i), \forall i \in \{a,b,c\} \tag{3}$$

Although the number of cells in each phase is equal in normal operation, once a fault occurs, the faulty cell (or cells) is bypassed by a switch located at the output of each cell, as

shown in Fig. 1. Fault detection system determines the number of remaining healthy cells in each phase (n_a-n_b-n_c) which will be used by post-fault control system. Any of the aforementioned methods [12-15] can be used for fault detection.

After bypassing the faulty cell (or cells), a fault-tolerant control algorithm must be utilized to control the inverter. Since this paper focuses on improving the Geometric method, this technique is explained in Part B as a post-fault control method.

B. The Geometric Post-Fault Control Method

As mentioned in the Introduction, to provide balanced line-line output voltages under faulty condition, a common mode voltage is added to all the phase voltages. The post-fault control method determines this common mode voltage.

In [21], a WB post-fault control method is suggested using the geometric approach that is called "Geometric" method. In this method, inverter phase voltages (v_{ag}, v_{bg}, v_{cg}) are considered as a summation of common mode voltage (v_{ng}) and the required output phase voltages (v_{an}, v_{bn}, v_{cn}).

$$v_{ig} = v_{in} + v_{ng}, \qquad \forall i \in \{a, b, c\} \tag{4}$$

If the amplitude of these waveforms is considered in p.u. (base value is V_{dc}), to prevent over-modulation operation, (5) expresses the criteria of the inverter phase voltages according to the related number of operative cells.

$$-n_i < v_{ig} < n_i \,, \forall\, i \in a, b, c \tag{5}$$

By substituting v_{ig} from (4) into (5), the common mode voltage (v_{ng}) must be restricted as:

$$-n_i - v_{in} < v_{ng} < n_i - v_{in} \,, \qquad \forall i \in \{a, b, c\} \tag{6}$$

To guarantee the satisfaction of (6) for all possible conditions, v_{ng} must comply by

$$u_d < v_{ng} < u_u \tag{7}$$

, where u_u and u_d are defined in

$$\begin{cases} u_u = min(n_i - v_{in}) \\ u_d = max(-n_i - v_{in}) \end{cases}, \qquad \forall i \in \{a, b, c\} \tag{8}$$

Although v_{ng} can be any value which satisfies (7), the mean value of u_u and u_d is chosen in [21]. Hence, v_{ng} is calculated from

$$v_{ng} = \frac{u_u + u_d}{2} \tag{9}$$

The maximum available line-line voltage ($V_{l,max}$) for WB methods can be calculated from

$$V_{l,max}[p.u.] = n_a + n_b + n_c - max(n_a, n_b, n_c) \tag{10}$$

Since common mode voltage contains higher order harmonic component for WB methods, it is expected that the amplitude of maximum available voltage is either higher or equal in comparison with VB methods [23].

III. PROPOSED METHOD

Although the most important task of the inverter when a fault occurs is to continue servicing as close to normal as possible, other features should be considered as well. One of the features can be the common mode voltage generated by the inverter. While common mode voltage reduction leads to a decrease in voltage stress on the motor bearings, it also reduces the inverter phase voltages' imbalance. The input current distortion is another concern that should be considered when in faulty condition. Since the input transformer is designed according to the nominal number of inverter's cells, the post-fault algorithms should provide equal loading between all cells in each phase as much as possible to minimize the input current distortion.

Due to merits of the Geometric method [21], particularly higher maximum available voltage as well as peak reduction ability, the proposed method is based on the Geometric approach, whilst trying to improve its performance. To do that, two solutions are proposed; Solution I and Solution II.

Since the maximum available voltage under some different faulty conditions may be equal, the proposed method in Solution I is focused on selecting the optimal post-fault state among them. The main object of this minimization is to achieve the lowest amount of Fundamental Component of Common Mode (FCCM) voltage for the same maximum available voltage.

The next solution, Solution II, proposes a modified post-fault control algorithm which leads to a decrease in the FCCM voltage for a given operating state where the required output voltage is less than its maximum value. These solutions are explained in Part A and Part B, respectively.

A. Solution I

The maximum available line-line voltage depends on the remaining cells in each phase as shown in (10). It is clear that $V_{l,max}$ may be the same for some different operating states. For example both operating states 5-4-3 and 4-4-3 give 7pu as the maximum balanced line-line voltage. On the other hand, in case of the 5-4-3 operating state, it is possible to reach the 4-4-3 state by intentionally bypassing one extra cell from phase 'a'. Hence, for the 5-4-3 state two strategies can be considered. First, all the 12 remaining cells participate in generating the maximum line-line voltage. Second, 11 cells (operating in the 4-4-3 state) generate the same maximum line-line voltage. In other words, by bypassing one extra cell in phase 'a', the state 4-4-3 can generate the same line-line voltage which can be generated by the state 5-4-3. This degree of freedom can be used for further improvement of the faulty CHB-MLI.

By considering this, it is a challenge to choose the optimal state in order to generate the maximum available voltage with minimum FCCM voltage. To determine the procedure for finding the optimal state, the operation of an 11-level CHB-MLI under two aforementioned states is investigated.

The common mode voltage, its spectrum, and the reference voltages derived from the Geometric method for the 5-4-3 and 4-4-3 operating states are depicted in Fig. 2 and Fig. 3, respectively, where the output line-line voltage is 7pu. Comparing the common mode voltage spectrums (Fig. 2(b), and Fig. 3(b)), the FCCM voltage substantially decreases from 0.948p.u. to 0.572p.u., where the 4-4-3 state is utilized. It can be concluded that among the 5-4-3 and 4-4-3 states, the 4-4-3 state is preferred due to its lower amount of the FCCM voltage value.

Although, the FCCM voltage reduces around 40% by using the 4-4-3 state instead of 5-4-3 state, dismissing one healthy cell in phase 'a' weakens this benefit. As mentioned before, to minimize the input current distortion, it is required to use all healthy cells as well.

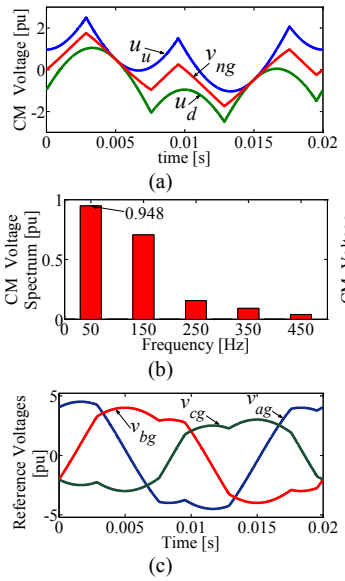

Fig. 2. Waveforms for a 5-4-3 operating state. (a) Common mode voltage with its boundaries. (b) Common mode voltage spectrum. (c) References of inverter phase voltages.

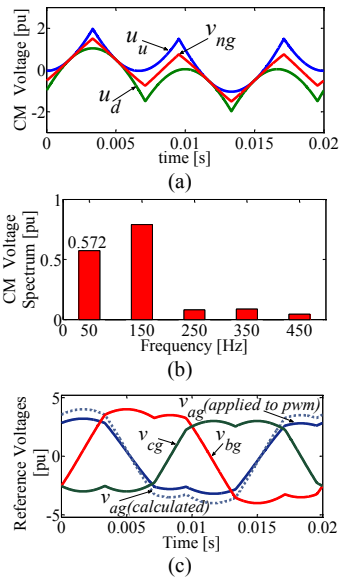

Fig. 3. Waveforms for a 4-4-3 operating state. (a) Common mode voltage with its boundaries. (b) Common mode voltage spectrum. (c) References of inverter phase voltages.

To overcome this flaw, a technique is proposed to utilize all the healthy cells as well as minimizing the FCCM voltage.

In this method, the optimal state (i.e. 4-4-3) is still selected to calculate the reference voltages by using the Geometric method.

Now, if the number of operative cells in phase 'a' becomes '5' instead of '4', it is possible to modify these voltages in order to achieve the same output voltage.

Achieving this, since the reference voltage of phase 'a' is calculated for $n_a = 4$, it must be multiplied by ratio of considered cells number in phase 'a' (i.e. 4) to the operative cells number in this phase (i.e. 5). These references voltages, applied to a PWM block and the previously calculated one for phase 'a' (dashed waveform) are depicted in Fig. 2(c), and Fig. 3(c) for both states.

Additionally, the input current spectrum and its total harmonic distortion (THD) are exhibited and compared for normal condition (i.e. 5-5-5) and three post-fault conditions: 5-4-3 state using the Geometric and the proposed methods, and 4-4-3 state using the Geometric method in Fig. 4. As expected, the input current distortion is reduced by using the proposed method and the FCCM voltage is minimized as well.

Four example cases for this condition are listed in Table I, and the FCCM voltages in two related operating states are presented for each case. Although the maximum line-line voltage for both states in each case is the same, by selecting State 2 to generate the references of phase voltages, the FCCM voltage significantly decreases.

As a conclusion, if the number of remaining cells in each phase after fault occurrence satisfies (11), Solution I can find the optimal operating state. Otherwise, the current state is considered as the optimal one.

$$n_i > n_j \geq n_k \,, \forall i,j,k \in \{a,b,c\}, \;\; and \; i \neq j \neq k. \qquad (11)$$

For further explanation, without the loss of generality, let's consider the condition (12). Obviously for other post-fault conditions (e.g. if $n_b > n_a \geq n_c$) similar analysis can be

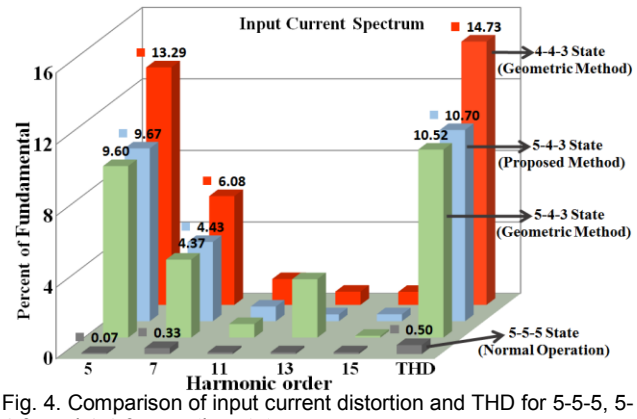

Fig. 4. Comparison of input current distortion and THD for 5-5-5, 5-4-3, and 4-4-3 operating state.

TABLE I
FOUR CASES INVESTIGATED FOR THE SOLUTION I.

Case	Operating state	FCCM Voltage [p.u]	$V_{l,max}$ [p.u.]
Case 1	State 1 (5-4-4)	0.53	8
	State 2 (4-4-4)	0	
Case 2	State 1 (5-4-3)	0.948	7
	State 2 (4-4-3)	0.572	
Case 3	State 1 (5-3-3)	0.976	6
	State 2 (3-3-3)	0	
Case 4	State 1 (5-3-2)	1.28	5
	State 2 (3-3-2)	0.579	

carried out. In this case, the number of healthy cells in phase 'a' is replaced with n_b in the post-fault calculation block.

$$n_a > n_b \geq n_c \qquad (12)$$

Since the number of operative cells in phase 'a' is still n_a, the calculated reference voltage of phase 'a' must be multiplied by $\frac{n_b}{n_a}$ for correct operation of the inverter.

To analyze the boundary of application of Solution I, an 11-level CHB-MLI example is considered. For this inverter, all the possible post-fault states are 114 cases, while 60 states among them (53%) satisfy the condition (11).

B. Solution II

In variable-speed drive application of CHB-MLI, the inverter output voltage changes based on the required speed. Therefore, the maximum available voltage may not be needed for all conditions. A comprehensive post-fault algorithm must consider this situation. To improve the inverter performance under such conditions and to decrease the FCCM voltage, it is proposed to proportionally reduce the common mode voltage when the required output voltage decreases. The reduction factor (D_n) is determined as the ratio of the required output phase voltage amplitude (V_{mn}) to the maximum available phase voltage in the faulty condition ($V_{p,max}$) as in

$$D_n = \frac{V_{mn}}{V_{p,max}} \qquad (13)$$

Hence, the modified common mode voltage ($v_n^{modified}$) is calculated by

$$v_{ng}^{modified} = \frac{u_d(t) + u_u(t)}{2} \times D_n \qquad (14)$$

Fig. 5 depicts the block diagram of the Solution II which is a modification of the Geometric method.

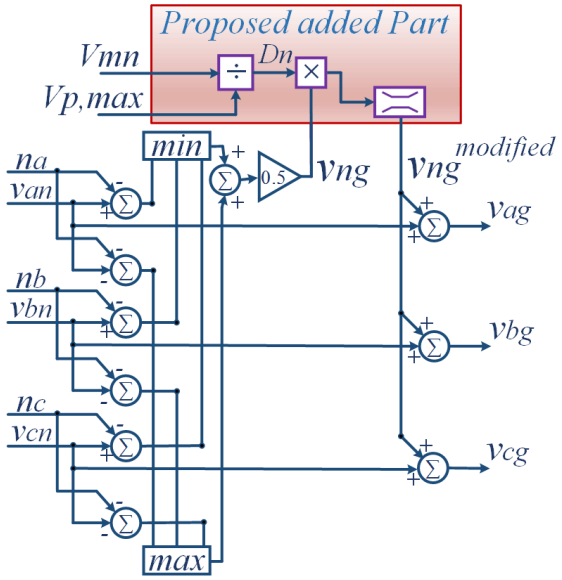

Fig. 5. Block diagram of the proposed method in Solution II.

To show the effectiveness of the proposed method, an 11-level inverter in operating state 5-5-3 is considered, where the output voltage modulation index (m) is 0.7, and hence $D_n = 0.76$. In Fig. 6(a) common mode voltage using the Geometric method and proposed method is shown with its top and bottom limits calculated from (8). It is clear that the modified common mode voltage is still located in the permitted boundary. According to the spectrum of the common mode voltage shown in Fig. 6(b), it can be verified that the FCCM voltage is decreased by 24% (0.285p.u.) by using the proposed method. Finally, the phase reference voltages for both methods are exhibited in Fig. 6(c).

For further investigation, another operating state, 5-5-1 is considered where $m = 0.46$ and $D_n = 0.67$. The common mode voltage and its spectrum using the Geometric and proposed method are shown in Fig. 7(a)-(b). It is clear that common mode voltage contains only a fundamental component which is reduced by 33% (0.77p.u.) in the proposed method. Additionally, it is expected that the only

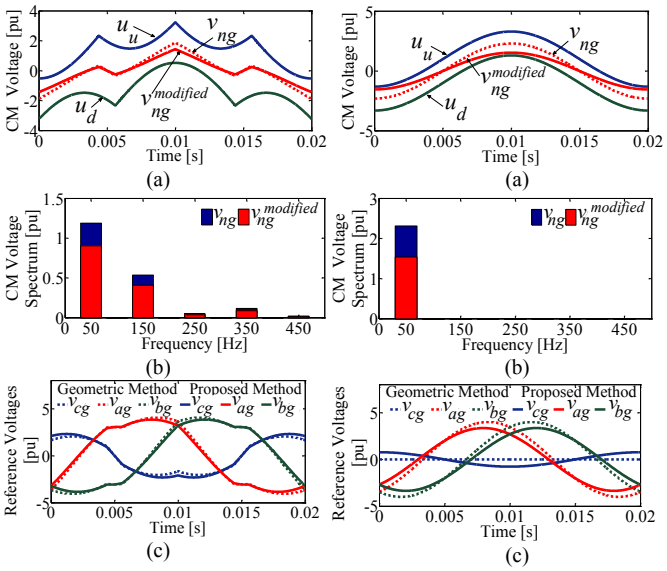

Fig. 6. Waveforms for 5-5-3 operating state with $m = 0.7p.u.$ (a) Common mode voltage with its boundaries. (b) Common mode spectrum. (c) References of inverter phase voltages.

Fig. 7. Waveforms for 5-5-1 operating state with $m = 0.46p.u.$ (a) Common mode voltage with its boundaries. (b) Common mode spectrum. (c) References of inverter phase voltages.

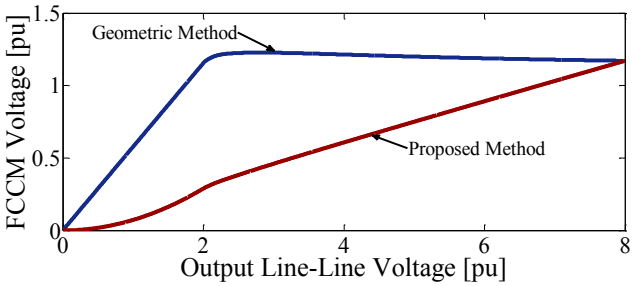

Fig. 8. Comparison magnitude of FCCM voltage for the Geometric, and the proposed method under operating state 5-5-3.

healthy cell in phase 'c' must be taken into account in order to provide the required voltage.

However, as shown in Fig. 7(c), the phase 'c' reference voltage is zero when using the Geometric method, whereas the proposed method leads to utilizing this phase as well. In other words, by applying the proposed method not only the FCCM voltage is reduced, but also the capacity of all healthy cells can appropriately be employed.

For more details, the magnitude of the FCCM voltage is compared for the Geometric and the proposed method, where an 11-level CHB-MLI works under 5-5-3 operating state and the output line-line voltage varies from zero to its maximum value (8p.u.). Fig. 8 shows that the value of the FCCM voltage can be reduced if the proposed method is employed.

Similar to (7), $v_{ng}^{modified}$ must meet the criteria (15) in order to prevent over-modulation

$$u_d < v_{ng}^{modified} < u_u \tag{15}$$

To verify this, three different conditions are considered. First let's assume $u_d < 0, u_u > 0$, then it is clear that since $0 < D_n \leq 1$, hence

$$u_d < v_{ng} < u_u \Rightarrow u_d < v_{ng} \times D_n < u_u \tag{16}$$

, and (15) is satisfied.

Secondly assuming $u_d > 0, u_u > 0$, it is enough to assure that:

$$u_d < v_{ng} \times D_n \tag{17}$$

In order to verify (17), the boundary value of D_n (D_{nb}) is defined as:

$$D_{nb} = max(\frac{u_d}{v_{ng}}) \tag{18}$$

Then, if

$$D_{nb} < D_n \tag{19}$$

, it can be guaranteed that the criteria of (17) is met.

Similarly, for the third condition in which $u_d < 0, u_u < 0$, it is necessary to confirm the validity of

$$D'_{nb} < D_n \tag{20}$$

Where $D'_{nb} = \max(\frac{u_u}{v_{ng}})$. Hence it can be assured that

$$v_{ng} \times D_n < u_u \tag{21}$$

, and the criteria of (15) is satisfied.

Numerical investigation has been carried out to find out the situations in which (19) and (20) are satisfied. The results show that the worst cases occur where the difference between

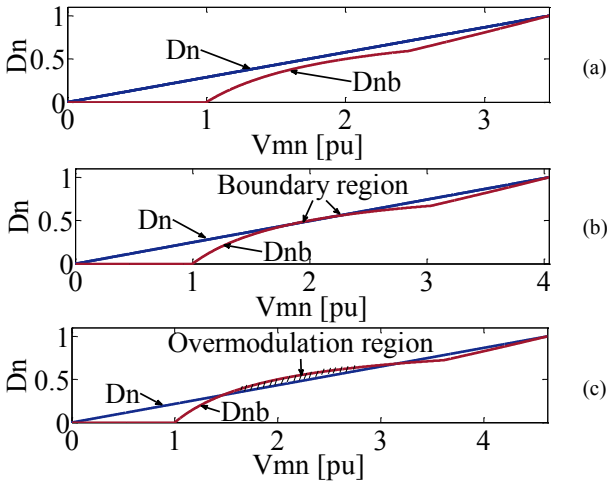

Fig. 9. Investigation of criteria (19) satisfaction for 5-5-1, 6-6-1, and 7-7-1 operating state.

number of healthy cells in phases are very big. For instance, in 11-level inverter, D_n is closer to the boundary values in 5-5-1 operating state compared to the state 5-5-2.

In Fig. 9, D_n and D_{nb} are compared for 11, 13, and 15-level inverters, where the worst case for each inverter (i.e. 5-5-1, 6-6-1, and 7-7-1 states) are considered. Fig. 9(a) guarantees that the criteria (19) is satisfied for all situations in an 11-level inverter, while the boundary condition may happen for a 13-level inverter as shown in Fig. 9(b) . However as shown in Fig. 9(c), since $D_{nb} > D_n$, the criteria (19) is not satisfied at some phase voltages. Therefore in order to avoid over-modulation, it is necessary to limit $v_{ng}^{modified}$ by using the limiter block demonstrated in Fig. 5. It is notable that since the results when u_u and u_d are negative are similar to the previous results, the related figure is not presented to prevent duplication.

To demonstrate what happens when $v_{ng}^{modified}$ is restricted to its boundary values, a 15-level inverter is considered where it works in 7-7-1 operating state with $V_{mn} = 2.3p.u.$ Fig. 10(a) shows $v_{ng}^{modified}$ in which it is saturated at some instants. According to the phase reference voltages for both methods (i.e. the Geometric and the proposed method) as shown in Fig. 10(b), it can be inferred that by using the proposed method, not only the magnitude of the phase 'a' and 'b' voltages are reduced, but also the remaining healthy cell in phase 'c' is utilized, on the contrary to the Geometric method. Furthermore, the magnitude of the FCCM voltage drops around 50% by using the proposed method [see Fig. 10(c)].

Consequently, the block diagram shown in Fig. 11 illustrates the proposed post-fault control system by considering Solution I and Solution II. Once again it should be noted that this block diagram is for the case where $n_a > n_b \geq n_c$, but due to the symmetry of the inverter, for other cases similar analysis can be carried out.

Once the fault is diagnosed in the fault detection block (any of the references mentioned in introduction [12-15] can be utilized), the number of remaining healthy cells in each phase (n_a, n_b, n_c) is determined and inserted in (12). If it is satisfied, the optimal operating state (n_b-n_b- n_c) is selected by using Solution I, in order to use in the block diagram of Solution II (Fig. 5). Otherwise, n_a, n_b, n_c are directly applied to this block diagram to determine the reference of inverter phase voltages.

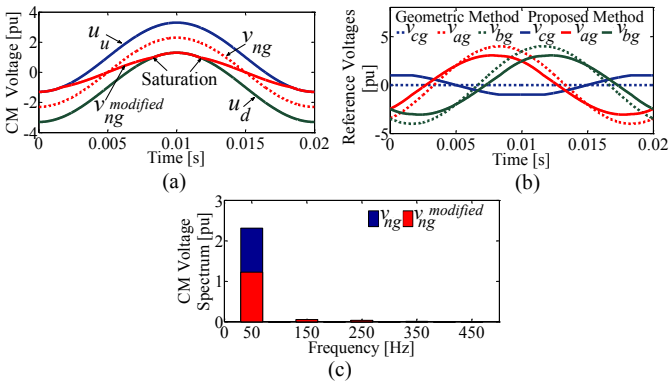

Fig. 10. Waveforms for 7-7-1 operating state, and $V_{mn} = 2.3p.u.$ (a) Common mode voltage with its boundaries. (b) Common mode spectrum. (c) References of inverter phase voltages.

After that, Solution II must calculate the references of phase voltages which leads to reducing the common mode voltage if the output voltages are less than their maximum available voltage. It is clear that if the required output voltage is at its maximum value, $D_n = 1$ and, consequently $v_{ng}^{modified} = v_{ng}$. Finally, the reference voltage of phase 'a' is multiple by 1 or $\frac{n_b}{n_a}$ depending on the output of "if-block".

It can be concluded that since the proposed solutions reduce the common mode voltage in two different but not alternative aspects, they must mutually be considered in the post-fault control system. For example, if the condition (12) is not satisfied for a given operating state, Solution I cannot find the optimal state. But in the same operating state, if the required output voltage is less than its maximum value, Solution II leads to a decrease in the common mode voltage. Conversely, for an operating state which satisfies the condition (12), if the required output voltage is at its maximum value, only Solution I is applied and the Solution II is ineffective. Additionally, for an operating state which satisfies the condition (12), if the required output voltage is less than its maximum value both solutions lead to reducing the common mode voltage; Solution I by selecting the optimal state and Solution II by multiplying the common mode voltage with D_n.

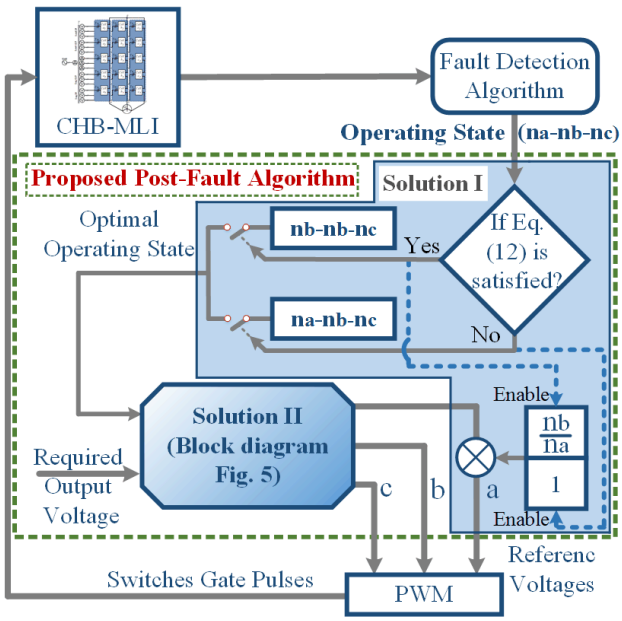

Fig. 11. Block diagram of the proposed post-fault control system.

IV. Experimental Results

To verify the performance of the proposed techniques, an 11-level 1.5kW CHB-MLI has been implemented, as shown in Fig. 12. Each cell is connected to a 60V DC-link voltage fed by an isolated 220/50V, 200VA, 50Hz transformer. This prototype uses IRF540M Power MOSFETs operating at 1kHz switching frequency and HIP4082IP drivers. A XC6SLX9 Xilinx FPGA is used to implement the Phase-Shift PWM method to control the inverter. Additionally the proposed fault-tolerant strategies are programed in the same board. The inverter output is connected to a three-phase induction motor (see Table II). To record the results, a GPS-1204c 4-channel signal storage oscilloscope and a Fluke 199 Scopemeter are used. Additionally, the currents are measured using LEM PR30 current probes.

The different cases of experimental tests are summarized in Table III.

A. Condition I: Solution I

The verification of the proposed method is carried out by considering two faulty conditions: 5-4-4 and 5-4-3 operating states.

Fig. 13 and Fig. 14 depict the experimental results for previously mentioned conditions. Each figure consists of four frames in which after 40ms the inverter incurs a faulty condition lasting 40ms. After that, the conventional post-fault control strategy is exerted for 40ms in order to achieve the maximum available balanced line-line output voltages. Eventually, the proposed fault-tolerant method is applied at t=120ms.

Fig. 13 illustrates the waveforms related to 5-4-4 operating state. As shown in Fig. 13(a), the inverter phase voltages incur unbalanced situation due to fault occurrence at t=40ms. After that, by using the conventional post-fault strategy at t=80ms, in spite of unbalanced phase voltages, balanced output currents are obtained (see Fig. 13(c)).

The proposed method is applied at t=120ms considering the 4-4-4 operating state instead of the 5-4-4 condition. The common mode voltage, which is depicted in Fig. 13(b), confirms that the FCCM voltage which is added to phase reference voltages has been reduced by 100% in the proposed method in comparison with the previous method, while output currents remain in same conditions (Fig. 13(c)).

Furthermore, Fig. 14 illustrates the same sequential states for 5-4-3 operating state. The proposed fault-tolerant control method, which is applied at t=120ms, brings about 4-4-3 condition for the inverter instead 5-4-3 state. It causes 23.58V (42%) reduction in the FCCM voltage in comparison with the conventional method used at t=80ms, as shown in Fig. 14(b).

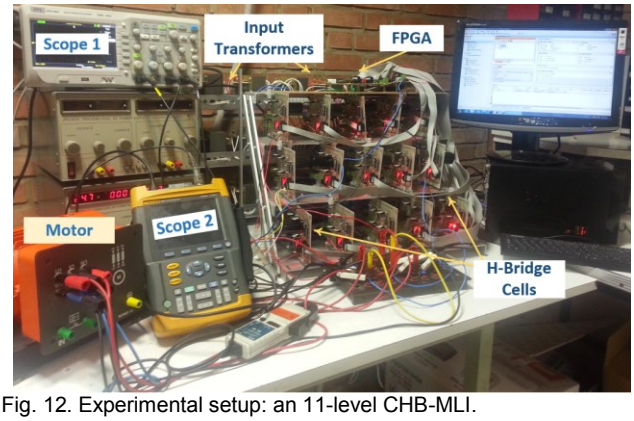

Fig. 12. Experimental setup: an 11-level CHB-MLI.

TABLE II
INDUCTION MOTOR CHARACTERISTICS

Power	Voltage	Current	PF	Speed
1kW	380V, 50Hz	2.1A	0.83	2900rpm

TABLE III
DIFFERENT CASES FOR THE EXPERIMENTAL TESTS.

Condition	Case	Operating state	Required output line-line voltage [p.u.]
Condition I	Case study 1	5-4-4	8
	Case study 2	5-4-3	7
Condition II	Case study 1	5-5-3	6.1
	Case study 2	5-5-1	4

The balanced operation of the inverter in post-fault condition is confirmed in Fig. 14(c).

B. Condition II: Solution II

Case 1) Two faulty cells in phase 'c':

In this case, inverter works in operating state 5-5-3. The electrical variables for the inverter are depicted in Fig. 15, where the system operates in normal condition up to t = 20ms. Since the balanced references waveforms are generated in PWM block, it is clearly seen in Fig. 15(a) that the balanced phase voltages are provided in inverter output. Additionally, the common mode voltage through Geometric method doesn't contain a fundamental component [see Fig. 15(b)]. Contrary to previous condition—*Condition I*, the maximum achievable line-line voltage is not required and m is 0.7 at normal condition, hence the phase voltages have four levels out of all five healthy ones to establish the required voltage.

The fault occurs at t=40ms. The effect of the fault occurrence on the voltage and current waveforms is shown in Fig. 15, where the faulty phase (phase 'c') operates with seven levels instead of nine levels, and the load currents are unbalanced. This leads to an increase in the FCCM voltage (Fig. 15(b)).

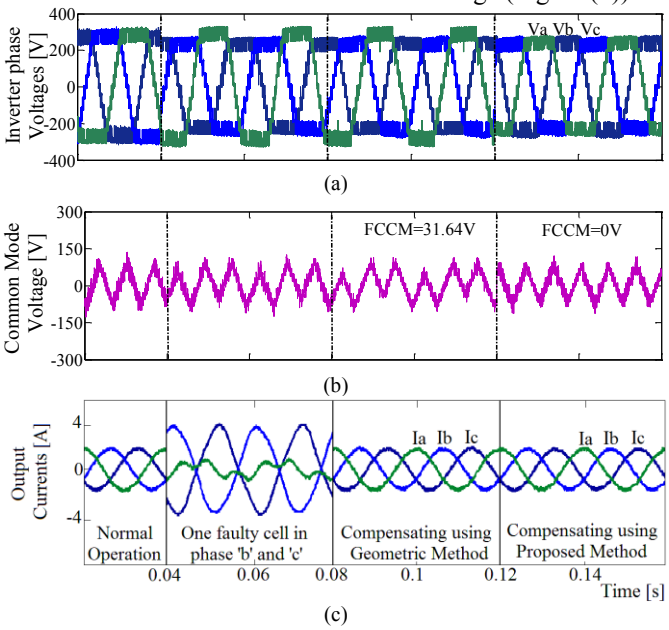

Fig. 13. Waveforms for 5-4-4 operation state. (a) Inverter phase voltages. (b) Common mode voltage. (c) Output currents.

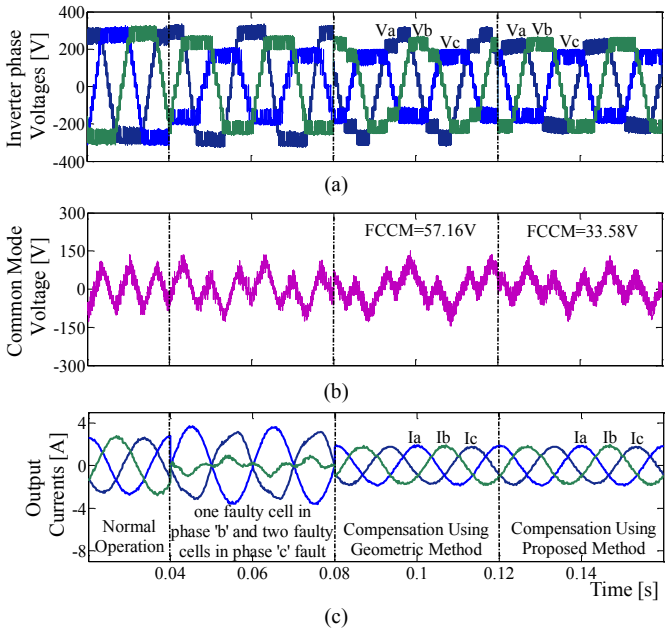

Fig. 14. Waveforms for 5-4-3 operation state. (a) Inverter phase voltages. (b) Common mode voltage. (c) Output currents.

After diagnosing the fault and bypassing faulty cells, the Geometric post-fault method is used to control the inverter and the results are illustrated in Fig. 15, at interval of t=80ms to t=120ms. According to the balanced load current, as shown in Fig. 15(c), it is clear that the inverter line-line voltages are also balanced. It is worth mentioning that the common mode voltage contains a fundamental component equal to 72.94V [see Fig. 15(b)].

Finally, the proposed method is applied at t=120ms. According to Fig. 15(c), the current waveforms remain unchanged and it can be inferred that the line-line voltage amplitude is the same as in the previous interval, while the common mode voltage has a 22% reduction in the fundamental component [see Fig. 15(b)].

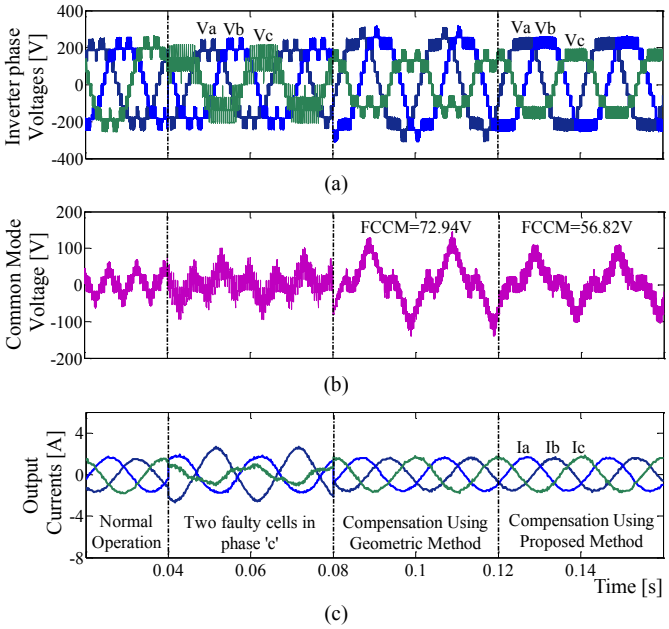

Fig. 15. Waveforms for 5-5-3 operation state and $m = 0.7$. (a) Inverter phase voltages. (b) Common mode voltage. (c) Output currents.

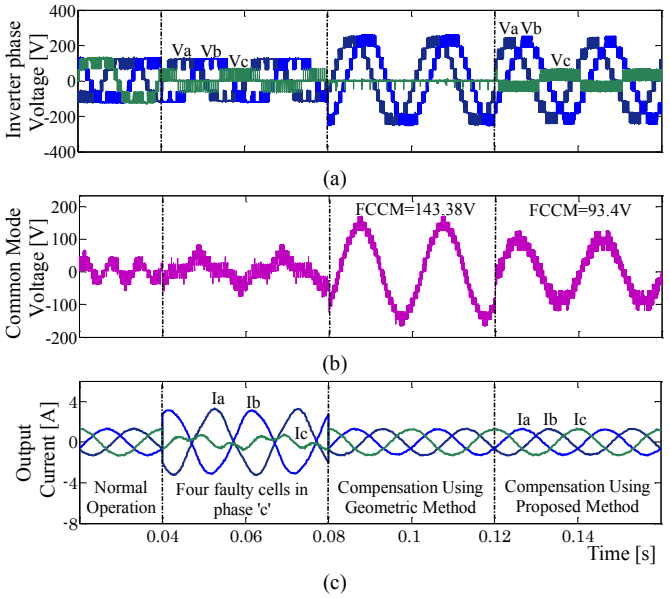

Fig. 16. Waveforms for 5-5-1 operation state and $m = 0.46$. (a) Inverter phase voltages. (b) Common mode voltage. (c) Output currents.

Case 2) Four faulty cells in phase 'c':

Another faulty condition (four faulty cells in phase 'c') is implemented in the experimental prototype in order to verify the effectiveness of the proposed method, and its results are depicted in Fig. 16, where the inverter works with $m = 0.46$ in pre-fault condition. The inverter works under normal conditions until the fault occurs at t = 40ms. Like the previous case, at interval between fault occurrence and detection, phase voltages and load currents are unbalanced (as shown in Fig. 16(a) and 16(c)).

Although by applying the Geometric post-fault method at t=80ms, the load current (Fig. 16(c)), and consequently, line-line voltages become balanced, the one remaining healthy cell of phase 'c' isn't working as illustrated in Fig. 16(a). By using the proposed method this problem can be solved as shown in the interval of t=120ms to t=160ms in Fig. 16(a). It is clear that the output voltage of phase 'c' is not zero anymore, where the output currents (Fig. 16(c)), and consequently, output line-line voltage still remain at their same previous values. Additionally, the common mode voltage decreases in such a way that its fundamental component is reduced to 93.4V from 143.38V.

It can be concluded that the proposed method not only leads to a decrease in the FCCM voltage, but also it utilizes all of the healthy cells.

V. Conclusion

This paper has concentrated on the improvement of Cascaded H-bridge Multilevel Inverter performance under faulty conditions aiming to reduce the common mode voltage. Two solutions have been proposed. Solution I tries to reduce the common mode voltage by selecting the optimal post-fault state among all possible states with the same maximum available voltage. However, to achieve lower amount of input current distortion, all remaining healthy cells must be utilized to generate the output voltage. To do that, the previously calculated reference voltages are modified before being applied to the PWM unit.

By using Solution II which is a modification of the Geometric method, it is possible to decrease the common mode voltage when the required output voltage is less than its maximum available value.

Computer simulations are carried out to evaluate the proposed methods. Moreover, a prototype has been implemented. Simulation and experimental results are in accordance and show that using the proposed methods, the fundamental component of common mode voltage is reduced in comparison with the existing methods.

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