Challenges and prospects for developing CdS/CdTe substrate solar cells on Mo foils

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ABSTRACT

ITO/ZnO/CdS/CdTe/Mo solar cells have been grown in the substrate configuration by a combination of close-space sublimation and RF sputtering. A peak efficiency of 8.01% was achieved. A two stage CdCl$_2$ annealing process was developed, with the first stage contributing to CdTe doping and the second being linked to CdTe/CdS interdiffusion by secondary ion mass spectrometry analysis. The inclusion of a ZnO layer between CdS and ITO layers improved performance significantly (from $\eta=6\%$ to $\eta=8\%$) by increasing the shunt resistance, R_{SH}, from 563 Ω cm^2 to 881 Ω cm^2. Cross-sectional scanning electron microscopy highlighted the importance of the resistive ZnO layer as numerous pinholes and voids exist in the CdS film. Solar cell performance was also investigated as a function of CdTe thickness, with optimal thicknesses being in the range 3–6 μm. All devices were deemed to be limited principally by a non-Ohmic back contact, the Schottky barrier height being determined to be 0.51 eV by temperature dependent J–V measurements. Modelling of device performance using SCAPS predicted efficiencies as high as 11.3% may be obtainable upon formation of an Ohmic back-contact. SCAPS modelling also demonstrated that a quasi-Ohmic back-contact may be achievable via inclusion of a highly p-doped ($\sim 10^{18}$ cm^{-3}) buffer layer, between CdTe and Mo, which also has an optimal electron affinity (4.2 eV). The evaluation of device processing and the in-depth characterisation presented here provides a number of insights towards the continued improvement of substrate cell performance.

1. Introduction

Recent significant increases in CdTe photovoltaic device performance [1] has followed a 20 year period of more modest progress [2]. The principal limitation that remains is considered to be the low open-circuit voltage, V_{OC} that is presently achievable (champion devices have V_{OC} in the range 850–900 mV) relative to CdTe's optical band gap (~ 1.5 eV): the inability to achieve sufficient doping densities ($> 10^{16}$ cm^{-3}) due to self-compensation [3] and recombination at the CdS/CdTe interface [4] are likely explanations. Currently, the vast majority of CdTe solar cell research is based on the metal/CdTe/CdS/TCO/glass 'superstrate' configuration (where TCO is transparent conducting oxide) whereby device layers are deposited onto a glass superstrate [5–7]. An alternative is the development of the TCO/CdS/CdTe/metal 'substrate' configuration (whereby the metal used is typically Mo due to it having a thermal expansion coefficient

similar to that of CdTe). The substrate configuration offers two significant advantages: (a) the stages of CdTe doping and CdTe/CdS junction formation may be optimised independently and (b) the use of low cost, flexible metal substrates may enable roll-to-roll cell production and allow a wide range of applications, including building- and vehicle-integrated PV.

Research into substrate devices has been limited to date, with the best reported performances being shown in Table 1 [8–14]. The common finding for all substrate devices is that generating an Ohmic back contact is problematic. As noted in Table 1, this may be overcome by the inclusion of a 'buffer layer' between the Mo substrate and CdTe layer to improve the contact. For instance, the devices reported by Kranz et al. [8] and Dhere et al. [10], use Te/MoO$_3$ and CuTe buffer layers respectively. However, since the back contact is formed early in the process, it must not degrade throughout the remaining high temperature processes. In superstrate cells on the other hand, back contact formation is the final procedure of device fabrication and this is not an issue. Note that the 13.6% Kranz [8], 11.3% Gretener [9] and 11.0% Dhere [10] devices were grown on Mo/glass substrates: The best reported substrate CdTe device on a *metal* substrate is Kranz's 11.5% device on Mo foil [8].

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Table 1

Efficiency of CdTe devices grown in substrate configuration on Mo substrates. The 'buffer layer' referred to is situated between Mo and CdTe for all devices.

Reference	Best efficiency (%)	Comments
[8]	(a) 13.6 (Mo/glass substrate), (b) 11.5 (Mo foil substrate)	Te/MoO$_3$ buffer layer+Cu doping
[9]	11.3 (Mo/glass substrate)	Cu/Te/MoO$_3$ buffer layer
[10]	11.0 (Mo/glass substrate)	Cu$_x$Te buffer layer
[11]	7.8	ZnTe:N buffer layer
[12]	6.5	RF sputtered CdTe+unnamed buffer
[13]	6.0	ZnTe buffer layer
[14]	6.0	CuTe buffer layer

Table 2

Annealing processes applied to substrate solar cells. Each annealing step was carried out in air for 30 min.

Treatment	After CdTe dep.	After CdS dep.	After ITO dep.
A	–	200 nm CdCl$_2$ T_{CdCl2}=420 °C	–
B	200 nm CdCl$_2$ T_{CdCl2}=420 °C	–	–
C	200 nm CdCl$_2$ T_{CdCl2}=420 °C	–	T_{anneal}=480–580 °C
D	–	–	T_{anneal}=480–580 °C

Whereas most reports of substrate devices so far have tended to focus on the optimisation of performance rather than in-depth characterisation and modelling, here, all of these aspects are considered as we believe they are critical for identifying device limitations. First, we present optimisation studies of the post-growth device processing in order to obtain high efficiency substrate devices, with particular focus on the sequencing of the Cl-doping stage. Second, an extensive study of the effect of annealing temperature and absorber layer thickness on device performance is presented. In-depth characterisation of substrate devices is provided by focussed ion beam-scanning electron microscopy (FIB-SEM), external quantum efficiency (*EQE*) and current–voltage–temperature (*J–V–T*) measurements. Finally, device modelling, using SCAPS [15], is presented. We report a peak efficiency of 8.01% for ITO/ZnO/CdS/CdTe/Mo substrate cells (where ITO is indium tin oxide), grown by a combination of close-space sublimation and RF sputtering.

2. Experimental

2.1. Fabrication of ITO/CdS/CdTe/Mo substrate devices

The 50 mm × 50 mm Mo foil substrates (Advent, 3 N pure) were cleaned ultrasonically in de-ionised water and dried with a N$_2$ air gun. CdTe films were close space sublimation-deposited, with a powdered source (Alfa Aesar, 5 N pure) heated to 605 °C and the substrate held at 530 °C. Growth was performed via a two stage process; firstly, under a static pressure of 25 Torr N$_2$ for 2–10 min, and then under low vacuum (10^{-1} Torr) for 1 min. Growth at the higher pressure has been shown to nucleate larger grains [6], but since it also acts to slow the growth rate, the films were completed by growth at the lower pressure. This process generated films of thickness 1.8–10 μm. CdS window layers of thickness ~200 nm were RF sputtered under 5 mTorr Ar for 30 min, using a target power of 60 W, with the substrate held at 200 °C. The ITO front contact layer was also deposited by sputtering, under 1 mTorr Ar for 120 min, using a target power of 70 W and with the substrate at 350 °C. Whilst this completed the basic layer structure, in some samples an intrinsic ZnO film was included between the CdS and ITO layers, this also being grown by sputtering, at room temperature, under 1 mTorr Ar for 20 min, using a target power of 100 W.

Table 3

A comparison of the performance parameters of devices subjected to different post-growth annealing processes (see Table 2 and text).

Treatment	η (%)	J_{SC} (mA/cm^2)	V_{OC} (mV)	FF (%)	R_S (Ω.cm^2)	R_{SH} (Ω.cm^2)
A	0.62	7.22	251	34.1	18.9	75
B	1.96	15.1	365	35.5	16.2	434
C (T_{2nd}=560 °C)	6.05	20.2	635	47.1	12.3	563
D (T_{2nd}=560 °C)	1.14	9.06	367	34.2	20.4	111

The 50 mm × 50 mm samples were then quartered into 25 mm × 25 mm plates for device processing.

Preliminary growth runs indicated that the standard CdCl$_2$ annealing process used for superstrate devices (typically a 20–30 min anneal of the CdS/CdTe stack at 420 °C following CdCl$_2$ evaporation [16]) was ineffective for substrate cell activation. Hence, in order to optimise the device processing, four different CdCl$_2$ post-growth treatments were tested, these being summarised in Table 2 and now described:

Treatment A: After CdS deposition, 200 nm CdCl$_2$ was thermally evaporated and the structures were annealed in air at 420 °C for 30 min, with ITO being subsequently deposited, and no further treatment being applied.

Treatment B: CdCl$_2$ deposition and annealing conditions were identical to treatment A but were applied *prior* to CdS and ITO deposition, i.e. only the CdTe layer was treated.

Treatment C: As treatment B (i.e. after CdTe deposition) but with the addition of a *second* annealing step after ITO deposition, in air at 480–580 °C air for 30 min, with no additional CdCl$_2$ deposition.

Treatment D: No CdCl$_2$ deposition and just a single annealing step, after ITO deposition, in air at 480–580 °C for 30 min.

For clarity, for the remainder of this paper, the temperature of the CdCl$_2$ annealing step after CdTe or CdS deposition is denoted as T_{CdCl2}, and the temperature of the annealing step after ITO deposition is denoted as T_{anneal}. After layer growth and annealing, devices were defined by mechanical scribing into 2.5 mm × 2.5 mm squares. Device performance parameters quoted in Tables 3 and 4 are from individual devices, whereas those plotted in Fig. 4 are averages taken from each plate (each having 16 individual devices).

Table 4
The best contacts from the series of devices presented in Section 3.3, showing the effect of CdTe thickness and annealing temperature. For averaged data, see Fig. 4.

T_{anneal} (°C)	Thickness (μm)	η (%)	J_{SC} (mA/cm^2)	V_{OC} (mV)	FF (%)
540	1.8	0.49	5.63	219	39.8
540	3.4	0.74	9.35	261	30.4
540	6.1	3.01	18.4	478	34.2
540	10	2.08	10.5	560	35.4
560	1.8	2.08	15.9	339	38.5
560	3.4	2.98	19.8	400	37.6
560	6.1	4.29	18.0	541	44.1
560	10	2.49	9.25	622	43.4
580	1.8	5.30	21.6	581	42.3
580	3.4	5.08	22.1	578	39.7
580	6.1	4.55	18.9	581	41.5
580	10	4.29	20.4	601	35.0

2.2. Characterisation and modelling

J–V measurements were carried out under AM1.5 illumination using an Oriel solar simulator, and J–V–T measurements were conducted in the dark, in the temperature range 200–350 K. EQE data was collected using a Bentham PVE 300 EQE system with white light bias. For secondary electron mass spectrometry (SIMS) analysis, a O^{2+} ion gun (Hiden Analytical) was used to sputter the sample (using a beam energy of 5 keV) and secondary ions were analysed by a quadrupole detector. Cross-sectional SEM images were generated using a FIB-milling procedure [16] in a FEI Helios Nanolab 600: After C and Pt coating of the sample, a focussed beam of Ga$^+$ ions were used to mill a trench in the sample, and to polish a cross-section. This was then imaged in secondary electron mode in the same instrument. Modelling of solar cell J–V curves and electronic band-diagrams was carried out using SCAPS, v3.2.00 [15].

3. Results and discussion

3.1. The impact of the CdCl$_2$ activation step

Fig. 1 shows the J–V curves of the best performing ITO/CdS/CdTe/Mo devices obtained from each of the post-growth treatments A–D, the shapes of the curves being representative of each respective sample set. Table 3 shows the photovoltaic performance parameters of these 'best devices'. All devices described in this comparison had a CdTe thickness, $X = 4 \pm 0.5$ μm and did not include a ZnO layer. Those subject to treatments C and D were done so using $T_{anneal} = 560$ °C.

All devices subject to post-growth treatment A, i.e. annealing after CdS deposition and with no further annealing, performed very poorly, the majority of contacts were short-circuits while the remainder typically had $\eta < 0.5\%$ due to low fill-factor, FF ($< 30\%$), short-circuit current, J_{SC} (< 5 mA/cm^2), and V_{OC} (< 300 mV). The best-device from this sample set had $\eta = 0.62\%$, limited by a series resistance ($R_S = 18.9$ Ω cm^2) that is considerably greater than that of high efficiency CdTe/CdS devices, and low R_{SH} (75 Ω cm^2). Here, direct CdCl$_2$ treatment of the CdS could induce densification and pinholing, and hence the creation of shunting pathways. More-over, Singh et al. [14] report that upon direct Cl-treatment of the CdS layer in substrate devices, there is an excessive intermixing at the CdS/CdTe interface resulting in the entire CdS layer being consumed and becoming CdTe$_x$S$_{1-x}$, lowering V_{OC} to ~ 0 V. Indeed, the presence of Cl is known to enhance S diffusion into CdTe [17].

Devices subject to post-growth treatment B, i.e. annealing after CdTe deposition and with no further annealing, also performed poorly, with the highest efficiency achieved being $\eta = 1.96\%$.
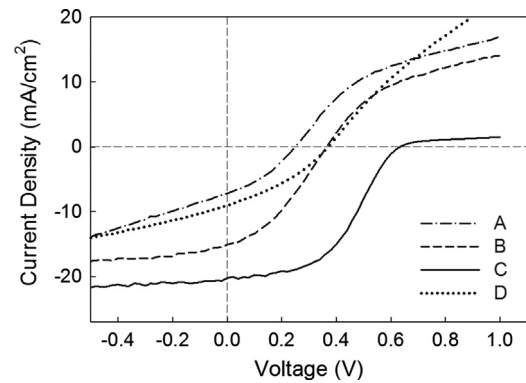

Fig. 1. J–V curves of the best performing substrate devices obtained from each of the post-growth treatments A–D. See Table 2 and the text in Section 2 for a description of these treatments, and Table 3 for the associated solar cell performance parameters.

Nevertheless, relative to treatment A, these devices had slightly improved V_{OC} (in the range 200–400 mV), and J_{SC} (5–15 mA/cm^2), whilst FF remained $< 35\%$. Since treatment B yielded slightly higher R_{SH} (434 Ω cm^2 for the best device, ~ 400 Ω cm^2 being typical for the sample set) than treatment A, it appears as though direct CdCl$_2$-treatment of CdTe is more effective than treatment of CdS/CdTe stacks in terms of avoiding pinholing. Nevertheless R_{SH} remains much lower than that of high efficiency devices, and R_S is too high (16.2 Ω cm^2 for the best device, ~ 20 Ω cm^2 being typical for the sample set).

Post-growth treatment C yielded significant performance enhancements, this differing from treatment B only by the inclusion of a second annealing stage following ITO/CdS deposition. Whereas the peak efficiency for treatment B was $\eta = 1.96\%$, a device subject to treatment C with $T_{anneal} = 560$ °C had $\eta = 6.05\%$. This was principally a result of enhancements to V_{OC} (from 365 mV for treatment B to 635 mV for treatment C) and FF (from 35.5% to 47.1%), implying an improvement in junction quality, this being discussed below with support from compositional data. For treatment C, R_S (12.3 Ω cm^2) was lower than for either treatments A or B, and R_{SH} (563 Ω cm^2) was higher.

All devices that were subject to treatment D, which consisted of a single annealing stage after ITO deposition but with no prior Cl-doping, had efficiencies, $\eta < 1.2\%$. The low V_{OC} (367 mV for the best device) is to be expected for devices that are not CdCl$_2$-treated since Cl-doping is typically necessary in order to attain sufficiently high p-type doping densities.

For all devices, there is a strong roll-over of the J–V curve in the first quadrant, which indicates a significantly poor back-contact. This was expected owing to the low work function of Mo (~ 4.36–4.95 eV) [18] relative to CdTe (> 5.7 eV) and the absence of a back contact buffer layer. The effect of the back contact on device performance is investigated in more detail in Section 3.6.

From these results, it is clear that the most effective post-growth treatment was that of using a twice-annealing process (treatment C). Whilst the first annealing stage, i.e. Cl-activation of the CdTe layer, is presumed to p-type dope the CdTe, the impact of the second annealing stage on the composition in the devices was investigated using SIMS profiling. Two devices were analysed, one subject to treatment B (having $\eta = 1.96\%$) and one subject to treatment C (having $\eta = 6.05\%$). Figs. 2a and b shows the S and Cl distributions respectively as a function of etch time for both devices. The left edge of the plots represents the front surface of the cell, i.e. the ITO surface. We do not quote the actual depth that the etch time correlates to, but we infer that the depth of the CdS layer is represented by the S peak of the single-annealed sample (B). It is clear from the data that S diffusion into the CdTe layer is
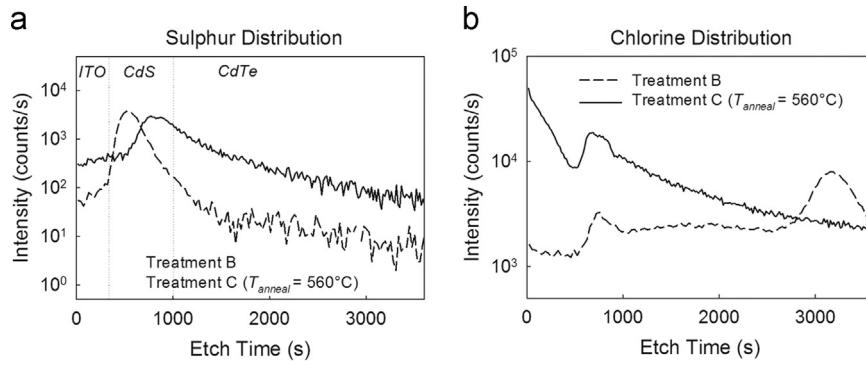
Fig. 2. SIMS depth-profiles of (a) sulphur and (b) chlorine concentrations in a device subject to treatment B (single-anneal) and a device subject to treatment C (double-anneal, $T_{anneal}=560$ °C). The left edge of the plots represents the front surface of the cell, i.e. the ITO surface.
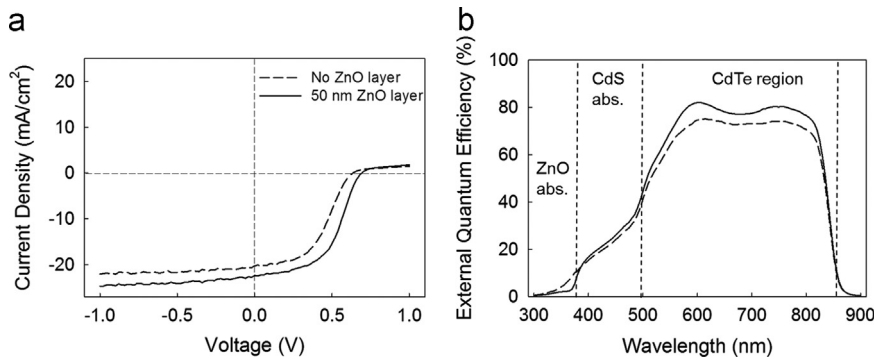

Fig. 3. (a) J–V curves and (b) EQE response of devices subject to treatment C at $T_{anneal}=560$ °C with and without the inclusion of a ZnO layer.

enhanced by the second annealing stage. Whilst excessive inter-diffusion is detrimental to device performance (causing CdS consumption), a certain level of interdiffusion is thought to assist in the passivation of surface defects at the interface and therefore lead to reduced interface recombination. The improvements in V_{OC} and J_{SC} affected by the second annealing step are consistent with this. There is also a distinct difference in the Cl-profiles of the two devices. In the device subject to just one annealing stage (B), there is an excess of Cl deep in the CdTe layer, towards the CdTe/Mo interface. In the device subject to two annealing stages (C), the deep Cl peak is not seen but there is a higher Cl concentration in the CdS layer and throughout the remainder of the CdTe, pre-sumably having diffused from deep in the CdTe following the second-annealing stage. This is likely to induce morphological changes in the junction region.

3.2. Inclusion of ZnO layer and EQE of best device

Fig. 3a shows the J–V response of devices subject to treatment C at $T_{anneal}=560$ °C with and without the inclusion of a ZnO layer between the CdS and ITO layers. The device without ZnO was the device having $\eta=6.05\%$ that was presented in the previous section.

Upon inclusion of the ZnO layer, device performance is clearly enhanced, the efficiency increasing to $\eta=8.01\%$. This resulted from improvements to J_{SC} (from 20.2 mA/cm^2 to 22.4 mA/cm^2), V_{OC} (from 635 mV to 690 mV) and FF (from 47.1% to 51.9%). Notably R_{SH} is significantly improved upon inclusion of the ZnO layer, from 563 Ω cm^2 to 881 Ω cm^2. This device had the best η achieved in these experiments. The mechanism of improvement upon use of such a high resistive layer is thought to be that it limits perfor-mance losses by electrically 'blocking' shunting paths and weak ITO/CdTe diodes (caused by pinholes), therefore increasing R_{SH} and V_{OC}, this being consistent with the results presented here.

Fig. 3b shows the EQE response measured from this device. The main features of the response from the device including a ZnO layer are now described. A relatively flat response is observed in the spectral region 600–860 nm, peaking at ~80% – the drop at ~860 nm being at the CdTe band-edge. There are significant losses in the above-gap region of the CdS (i.e. ≤ 500 nm) and a further reduction in EQE for $\lambda < 390$ nm associated with absorption by the ZnO. Note also the gradual decrease in EQE in the 500–550 nm wavelength region, presumably associated to absorption in alloyed CdS$_{1-y}$Te$_y$ for which the band-gap is lower than CdS. A similar response was observed for the device without ZnO, the only differences being (a) a lower efficiency in the CdTe region and (b) the absence of the ZnO related absorption cut-off at 390 nm.

3.3. Effect of CdTe thickness

A series of devices with CdTe thickness, X, in the range 1.8–10 μm were grown, subject to treatment C at $T_{anneal}=540$–580 °C. For all these devices, a 50 nm ZnO film was included between the CdS and ITO layers. The average performance parameters as a function of X and T_{anneal} are plotted in Fig. 4. The parameters of the best contacts from each plate are listed in Table 4 for reference, although the discussion that follows generally refers to the averaged data. In Fig. 5, typical J–V curves for devices subject to treatment C with $T_{anneal}=580$ °C, having different X are shown. Note that this was an entirely new sample set and the 'best' device reported in the previous section was not part of this set.

Regardless of annealing temperature the optimum CdTe thick-ness was $X=3$–6 μm, the average η being ~4% in this range for $T_{anneal}=580$ °C. The thickness-dependency of η closely followed that of J_{SC}, which peaked at 18.9 ± 2.1 mA/cm^2 with an absorber thickness of 3.4 μm, also for $T_{anneal}=580$ °C.
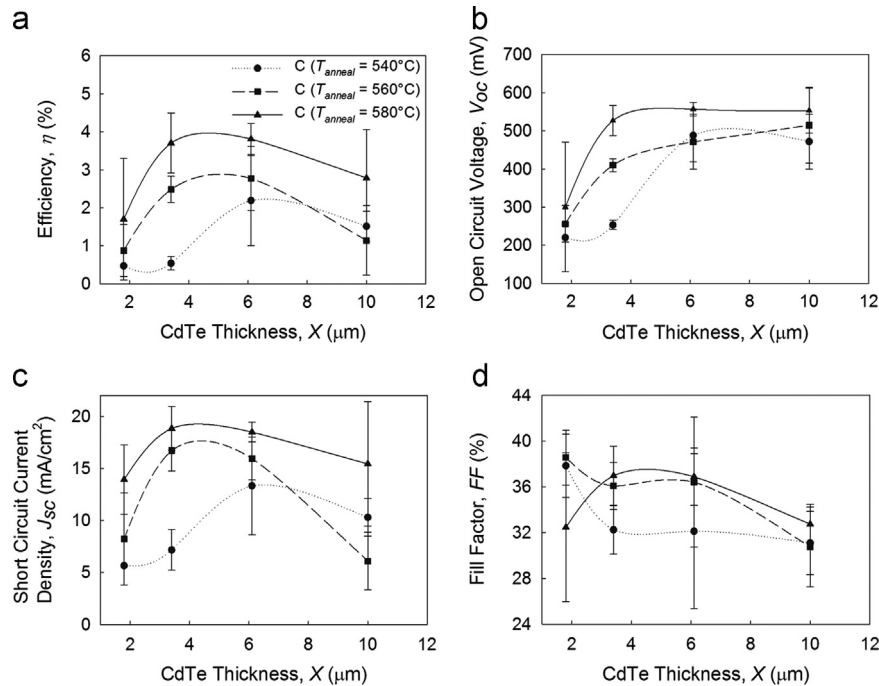
Fig. 4. Dependence of (a) η, (b) V_{OC}, (c) J_{SC} and (d) FF as a function of CdTe thickness for a range of annealing temperatures (T_{anneal}=540–580 °C). Lines added as a guide to the eye. The data points show the averages and standard deviation for up to 16 devices. See Table 4 for the best contacts from each plate.
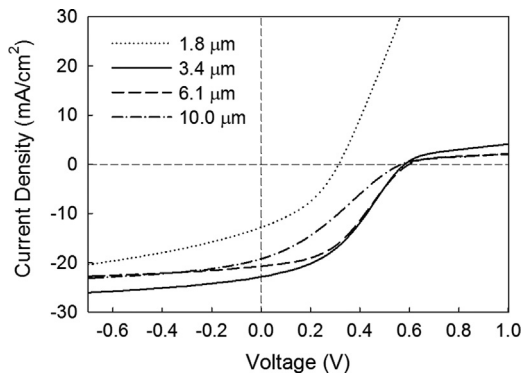

Fig. 5. Typical J–V curves for devices subject to treatment C (T_{anneal}=580 °C), with different CdTe thicknesses (1.8–10 μm).

As well as having lower average J_{SC} (< 14 mA/cm^2), the thinnest devices ($X=1.8$ μm) typically suffered from much lower average V_{OC} (< 300 mV) than the rest of the samples resulting in average efficiencies of $\leq 1.8\%$ for all annealing temperatures. This may directly result from the presence of micro-shorts in the thinner CdTe layers, as suggested by Clayton et al. [19], although this should also result in a reduction of FF which is not consistently observed here. Instead, it may be attributed to the Schottky back contact at the Mo/CdTe interface: devices with a significant back contact barrier are usually modelled to consist of two independent and opposing diodes [20] (whereby the back contact diode acts to increase R_S), but in the case of thin absorber layers the depletion region of the back contact will overlap with that of the main junction and therefore the V_{OC} will be reduced. In accordance with the failure of the independent two-diode model, no rollover should be observed, as is the case here for the thinnest device (1.8 μm) in Fig. 5. The performance from these thinnest devices was notably inconsistent, with one device having an efficiency as high as $\eta=5.3\%$ (see Table 4).

The highest V_{OC}s (approaching 600 mV) were achieved when using the highest annealing temperature, implying greater levels

of S and Te intermixing and/or recrystallisation of CdTe/CdS layers. For all annealing temperatures, the V_{OC} plateaus above a CdTe thickness of 6 μm.

The thickest devices (10 μm) suffered from lower FF (30–35%) for all annealing temperatures. Indeed, for the series of devices annealed at T_{anneal}=580 °C, R_S increased with CdTe thickness: R_S was calculated from the slope of the typical J–V curves (Fig. 5) in forward bias to be 8.1 Ω cm^2 (for CdTe thickness of 1.8 μm), 14.1 Ω cm^2 (3.4 μm), 14.8 Ω cm^2 (6.1 μm) and 22.3 Ω cm^2 (10.0 μm). This may be due to the higher probability that there exist grain boundaries perpendicular to current flow in thicker CdTe films, or simply due to the intrinsic resistance of the CdTe itself. Notably, however, when using a lower annealing temperature of 540 °C, the R_S for thinner CdTe films (3–6 μm) was equivalent to that for the 10 μm CdTe films that had been annealed at 580 °C, this implying that high R_S is attributed to CdTe films being 'undertreated'.

3.4. FIB-SEM

Fig. 6 shows secondary electron SEM images of a FIB-milled cross-section from a ITO/ZnO/CdS/CdTe/Mo device. This device was subject to treatment C (T_{anneal}=580 °C), having a CdTe thickness of ~ 1.8 μm and efficiency of 5.3% (taken from the sample set presented in Section 3.2). The grains in the CdTe layer are relatively large, extending the entire width of the film and up to 4 μm in width. There are low-energy twin boundaries present, but these are considered to be non-electrically active [21]. Most notable is the existence of voids (diameter ~ 100 nm) both in the bulk of the CdTe and in the CdS. Moreover, the higher magnification image (Fig. 6b) shows that there are discontinuities (or pinholes) in the CdS film, resulting in the ZnO coming into contact with the CdTe. This further emphasises the importance of using a ZnO layer if the CdS uniformity is insufficient, as it minimises the impact of weak diode regions (e.g. ITO/CdTe) which are detrimental to V_{OC}. It was also observed that the CdS layer is significantly thinner (~ 120 nm) after the second annealing step than directly after growth (~ 200 nm). This further supports the SIMS data that S diffusion into the CdTe occurs during annealing.
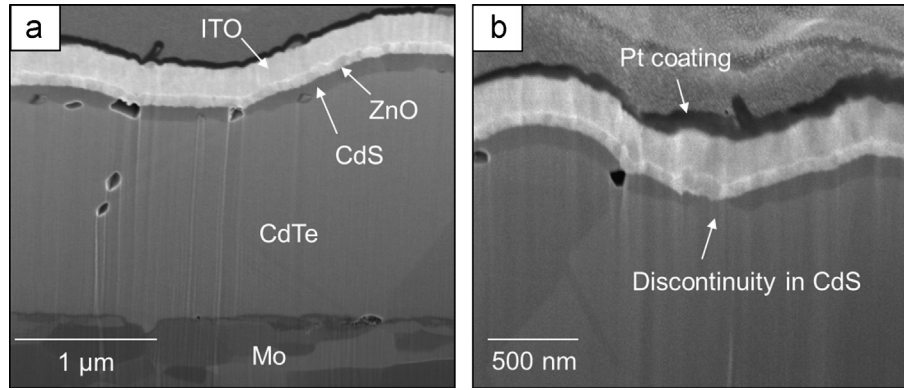
Fig. 6. Secondary electron images of FIB-milled ITO/ZnO/CdS/CdTe/Mo device cross-section: (a) Full device structure and (b) the junction region. The device was subject to treatment C, i.e. the double-anneal process, with $T_{2nd} = 580\ ^{\circ}$C, and had efficiency, $\eta = 5.3\%$.
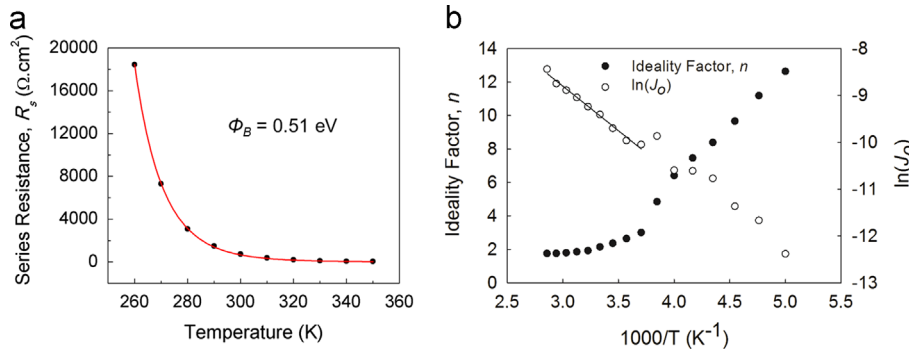

Fig. 7. (a) The temperature dependence of R_S, used to determine the back contact barrier height, ϕ_B. (b) Temperature dependence of the ideality factor, n, and the saturation current, J_0. This data was taken from a device subject to treatment C ($T_{anneal} = 580\ ^{\circ}$C), having a CdTe thickness of $\sim 6\ \mu$m and for which $\eta = 5.5\%$.

3.5. J–V–T measurements

J–V–T measurements were used to determine the back contact barrier height of a device subject to treatment C at $T_{anneal} = 580\ ^{\circ}$C and having a CdTe thickness of $\sim 6\ \mu$m and $\eta = 5.5\%$ (taken from a new sample set). The barrier height, φ_B, may be extracted from the temperature dependence of R_S via the method of Bätzner et al. [22], which assumes that R_S can be expressed as a summation of an Ohmic and an exponential component. Here, at each temperature, R_S was calculated from the slope in the forward bias region of dark J–V curves. Fig. 7a shows the experimental R_S–T data for this device, fitted with Bätzner's model, which yields a barrier height of $\phi_B = 0.51$ eV. Demtsu et al. [20] state that in the two-diode model of a photovoltaic device any barrier height that exceeds 0.5 eV is detrimental to the FF, although not necessarily to V_{OC}.

Furthermore, by investigating the temperature dependence of the ideality factor, n, and saturation current, J_0, information about the charge transport mechanisms operating within a device may be yielded, as reviewed extensively by Alturkestani [23]. At each temperature, n and J_0 may be extracted from the gradient and x-axis intercept of dark $\ln(J) - V$ plots respectively, provided the following assumption to the Shockley equation is made:

$$J = J_0 \left[\exp\left(\frac{qV}{nk_BT}\right) - 1 \right] \approx J_0 \exp\left(\frac{qV}{nk_BT}\right) \quad (1)$$

where q is the electron charge and k_B is Boltzmann's constant. Fig. 7b shows the temperature dependence of the ideality factor, n, and saturation current, J_0 for the same device as above (subject to treatment C, $X = 6.1\ \mu$m, $\eta = 5.5\%$). In the temperature range 270–350 K, $n \sim 2$ which indicates that transport occurs via recombination in the depletion region [24]. The $\ln(J_0) \propto -1/T$ dependence is also indicative of a recombination regime in this temperature

range [24]. However, below 270 K, n increases as the temperature is reduced, which indicates that charge transport is dominated by a multi-step tunnelling regime [25].

3.6. SCAPS modelling and use of back contact buffer layers.

Device modelling was carried out using the SCAPS simulation tool developed by Burgelman et al. [15] in order to verify the J–V characteristics of the best performing device of this study and to determine to what extent the poor back contact limits device efficiency. The program enables the definition of the film stack, the assignment of material properties (e.g. optical band gap, doping density and type, density of states) to each film and the inclusion of defect states in the bulk of films and at interfaces. For the back contact the only variables are the work function and barrier height. To simulate the devices reported here the material properties used by Gloeckler et al. [26] in a SCAPS simulation of a CdTe/CdS superstrate cell ($\eta = 16.4\%$) were used as a starting point (these include band gaps, optical properties, trap parameters) and then the model was modified to include (a) a back contact with a work function of ~ 5.25 eV to represent Mo; (b) a CdTe electron affinity, E_{ea}, of 4.5 eV; (c) a maximum CdTe doping density of $N_A = 2 \times 10^{15}$ cm^{-3}, as determined from preliminary capacitance–voltage measurements (not shown); (d) reduced N_A in the CdTe layer towards the back contact due to the depletion of holes affected by the Schottky barrier; and (e) increased R_S, comparable to devices reported here ($10\ \Omega$ cm^2). J–V curves were simulated under AM1.5 illumination the device, and this was repeated once the option for 'Ohmic contact' was selected, which generates an Ohmic contact regardless of the properties of metal and CdTe. Fig. 8 shows the experimental J–V curve for the best performing device, the simulated J–V curve that represents this device, and a simulated curve of the device with an Ohmic contact. A good

agreement between the experimentally determined performance parameters (η=8.01%, J_{SC}=22.4 mA/cm^2, V_{OC}=690 mV, FF=51.9%) and the simulated parameters (η=8.02%, J_{SC}=22.4 mA/cm^2, V_{OC}=694 mV, FF=51.6%) was achieved. Upon implementation of an

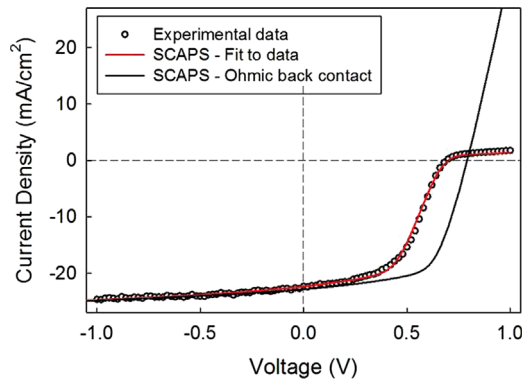**Fig. 8.** J–V data for highest efficiency (η=8.01%) substrate cell overlapped with modelled J–V data from SCAPS software (η=8.02%). By inclusion of an Ohmic back contact in the model, the predicted performance was improved to 11.3%.

Table 5
Performance characteristics of substrate configuration devices given by SCAPS software when various back contact buffer layers are added to the original structure.

Buffer layer N_A	Buffer layer E_{ea}	Buffer thickness	η (%)	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)
No buffer (CdTe)	–		8.02	694	22.4	51.6
10^{15} cm^{-3}	4.2 eV	500 nm	10.61	791	22.4	59.9
10^{18} cm^{-3}	4.5 eV	500 nm	9.65	772	22.3	56.1
10^{18} cm^{-3}	4.2 eV	500 nm	11.32	794	22.5	63.4

Ohmic contact, the simulation suggests these may be increased to η=11.3%, J_{SC}=22.9 mA/cm^2, V_{OC}=792 mV and FF=62.3%, with the curve showing no rollover. This demonstrates that the back contacting to our device is significantly hindering device performance and that the efficiency shortcoming of our devices relative to those of Kranz et al. [8] is largely attributable to the poor back contact.

The SCAPS model was also used to assess the impact of including various types of back contact buffer layer (with high p-type doping and/or optimised electronic band structure), between Mo and CdTe. A buffer layer of 500 nm thickness was added to the device model between CdTe and Mo, with all properties being kept the same as that of CdTe (e.g. optical band-gap, dielectric permittivity, densities of states, electron and hole mobilities), but with the value of its electron affinity, E_{ea}, or p-type doping density, N_A, being modified. The chosen values of the buffer layers' doping density and electron affinity are listed in Table 5, along with the simulated performance parameters of the devices upon the buffer layers' inclusion. The electronic band diagrams at the Mo/buffer layer/CdTe interfaces, also generated by SCAPS (at zero bias in the dark), for each of the simulated buffer layers are shown in Fig. 9.

With no buffer layer present the modelling was exactly the same as for the fit to the experimental data in Fig. 8 for which the efficiency was 8%. The band diagram for this device (Fig. 9a) shows there is a barrier height of 0.38 eV, this being slightly lower than the experimental value (presumably due to the simulation being carried out at zero bias).

By choosing a buffer layer with an electron affinity (4.2 eV) such that it's work function, ψ, lies between the values of the metal and CdTe (i.e. 5.25 eV < ψ < 5.9 eV), the barrier at the back contact can be split into two smaller barriers (Fig. 9b). The effect of this was to significantly improve the V_{OC} (from 690 mV to 790 mV) and consequently η (from 8.0% to 10.6%). Alternatively, by choosing a highly p-doped (10^{18} cm^{-3}) buffer layer, the barrier at the metal/buffer interface is large but narrow (Fig. 9c), allowing tunnelling to occur, and an improvement in η (to 9.7%) is achieved. Indeed, this
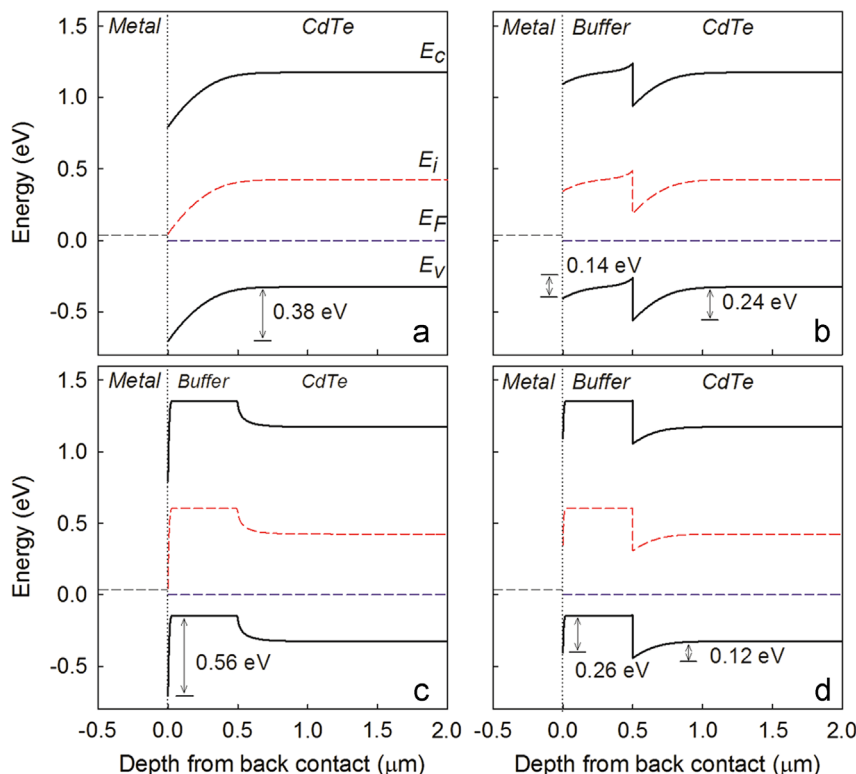

Fig. 9. Electronic band diagrams (at zero bias in the dark) generated using SCAPS focussing on the back contact region and the effect of the use of various buffer layers, each having a thickness of 500 nm. (a) No buffer layer, (b) N_A=10^{15} cm^{-3} and E_{ea}=4.2 eV, (c) N_A=10^{18} cm^{-3} and E_{ea}=4.5 eV, (d) N_A=10^{18} cm^{-3} and E_{ea}=4.2 eV.

approach is used for the formation of Ohmic contacts to super-strate CdTe devices: the CdTe back surface is usually chemically etched to generate a Te-rich surface making it highly p-type. However, for substrate cells, etching of the back surface is not possible. To yield a performance as high as that achieved with an Ohmic contact (11.3%, represented by the solid J–V curve in Fig. 8), a buffer layer that is both highly doped and has an ideal electron affinity should be included (Fig. 9d), this generating one small barrier at the buffer layer/CdTe interface (0.12 eV) and one narrow barrier at the metal/buffer layer interface (0.26 eV). These results demonstrate what properties a buffer layer must possess, and they imply that the shortcoming of our devices is dominated by the non-Ohmic back contact. Fahrenbruch [27] has reviewed similar methods to those proposed here, citing Cu_xTe, Sb_2Te_3 and ZnTe:N as potential buffer layer materials with sufficiently high N_A ($\sim 10^{21}$, $\sim 10^{20}$ and $\sim 10^{18}$ cm^{-3} respectively) but no materials with $\psi_{metal} < \psi < \psi_{CdTe}$.

4. Conclusions

A peak efficiency of 8.01% has been achieved for substrate configuration CdTe solar cells, with the device architecture ITO/ZnO/CdS/CdTe/Mo.

Initially, the effect of varying the sequence of the CdCl$_2$ activation step was investigated. It was shown to be optimal to use a double-annealing process; (a) CdCl$_2$ deposition onto the CdTe layer acts to dope the CdTe and (b) high temperature ($> 560\,°C$) annealing following CdS and ITO deposition improves the junction quality by enhancing S and Te interdiffussion. Increased S diffusion into the CdTe layer following the second annealing stage was demonstrated using SIMS analysis and supported by the observation that the CdS layer is thinner following the second anneal than immediately after growth. Other post-growth treatments that involved just a single-annealing step resulted in generally low efficiencies ($\eta < 2\%$).

Improvements to device efficiency were made by including a ZnO layer between the CdS and ITO. These improvements were mainly realised through increased V_{OC} and R_{SH} therefore it is presumed that the ZnO layer limits the detrimental effects caused by pinholes. Indeed, voids and pinholes in the CdS layer were observed in FIB-SEM images.

The effect of the thickness of CdTe on device performance was also studied, with the optimum thickness being in the range 3–6 μm. Devices with thinner CdTe (1.8 μm) suffered from poor V_{OC}, whereas those with thicker CdTe layers (10 μm) had low FF due to increased R_S.

The J–V curves of all devices studied here exhibited significant roll-over, this being attributed to a non-Ohmic back contact, the barrier height being determined to be as high as 0.51 eV from J–V–T measurements. J–V–T measurements also indicate that in the temperature range 270–350 K, charge transport is dominated by recombination in the depletion region, whereas at lower temperature a multi-step tunnelling regime operates.

SCAPS modelling implied that the non-Ohmic contact was the principal limiting factor to efficiency for these devices, and that the successful formation of an Ohmic contact would yield efficiencies equivalent to the highest reported for substrate cells. A quasi-Ohmic contact may be achieved through inclusion of a buffer layer (at the Mo/CdTe interface) which is highly p-doped (10^{18} cm^{-3}) and has an electron affinity ~ 4.2 eV.

Acknowledgements

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