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Compatibility Issues with Irregular Current Injection Islanding Detection Methods and a Solution

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Abstract: Islanding detection methods, based on injecting high-/low-frequency currents or negative sequence fundamental frequency currents and observing the resultant responses, are collectively referred to as irregular current injection methods in this paper. In multi-distributed generation (DG) operation, if there is no restriction to the phase of injected irregular currents, the currents at the same frequency may cancel each other out, and then their convergent current may be too small to cause a detectable response, for which reason islanding detection will be severely affected. Accordingly, this paper raises a compatibility issue, which requires the phase difference between any two injected irregular currents to be within a certain interval. In response to this issue, a solution is proposed. According to this solution, the terminal voltage of DG units is referenced to conduct irregular currents injection, and only certain high-frequency currents are used as injected currents. If this solution is adopted by as many manufacturers as possible, the effect and reliability of such methods will be greatly improved.

Keywords: compatibility; current injection; islanding detection; multi-DG; terminal voltage reference

1. Introduction

In distributed generation (DG), DG units are dispersed in various areas with associated loads. If a main grid is lost for some reason, the DG units and loads connected with it before will form an electricity island. In this island, if the power is matched, the DG units and loads will continue to run. This situation is out of power dispatching and monitoring and is harmful to personal and equipment safety, for which reason it must be detected rapidly. Islanding detection arises from this. So far, a large number of islanding detection methods have emerged. In general, these methods are divided into remote methods, passive methods and active methods. The active methods are very cost-effective and thereby attract a lot of studies. This paper will discuss a main type of active method named the irregular current injection method.

According to the irregular current injection method, a DG unit (seen as a current source) injects high/low frequency currents or negative sequence fundamental frequency currents into the network and observes the resultant voltages to detect an island [1–18]. In practice, there are some special circuit topology and control algorithms, and then how to inject a harmonic under such conditions is an interesting topic [1,4]. Regarding the specific implementation of harmonic injection, a scheme based on a d-q reference frame was proposed in [2], which was similar to a fundamental current control, and another scheme based on static reference frame and PR (Proportional Resonant) regulators was proposed in [7]. To cope with unbalanced grid impedance scenarios in islanding detection, a scheme was proposed in [3], which injected dual-frequency harmonic currents. Besides the sinusoidal current injection, a pulse current injection is also an option and has been studied in [5]. Negative

sequence fundamental currents have been widely used in literature, for they have been extensively studied in other fields, and the manner in which such currents can be exploited for islanding detection was introduced in [6,9,12]. In addition, it is also very common to measure network impedance by means of the harmonic voltages and currents, for an island event may result in a surge of the network impedance [10,11]. Island misjudgment is a problem that must be faced in islanding detection. In [18], a scenario that may result in a misjudgment was discussed; the reason for the misjudgment was analyzed and a solution was proposed. On the contrary, in [13–17], irregular voltage injection was exploited for islanding detection, by which the DG units were presented as voltage sources, and the problems with multi-DG operation were addressed.

Moreover, many other islanding detection methods are also widely used. A frequency shift method, which is another classic type of active method, was introduced in [19]. Actually, this frequency shift method was mixed with a passive method, and such a hybrid method was the future development trend. A passive method based on measuring the frequency-dependent impedance at an inverter terminal was employed in [20]. A remote method exploiting the phasor measurement unit to collect the related information of an island was employed in [21]. Additionally, the control strategy during islanding operation was also explored in some literature. [22,23] contributed two schemes for controlling DG units during grid-connected and islanding operation.

The above section has mentioned that the principle of irregular current injection methods is to inject irregular current first and then observe the response. This paper will focus on the issue at the injection stage. Since generally there is no communication between DG units, the injected irregular currents cannot be coordinated. Thus, in particular, their phases are independent, for which reason the irregular currents at the same frequency may cancel each other out and thereupon their convergent current may be too small to cause a detectable response. This issue is called the compatibility issue in this paper, and it may severely affect islanding detection. This paper will analyze this issue in detail and study how to cope with it.

Furthermore, the above compatibility issue is based on the currents at the same frequency. The currents at different frequency (and their responses) can be extracted from their syntheses, and thus there is no such issue between the methods that inject different frequency currents, while these methods will not affect each other either with respect to islanding detection. In fact, for islanding detection methods, all the active methods thereof have the compatibility issue due to their exciting-observing response mechanism. For frequency shift methods, a design criterion from the requirement of synergy between DG units has been derived in [24], which can actually be seen as a strategy coping with the compatibility issue.

This paper is organized as follows: Section 2 explains the compatibility issue of irregular current injection methods; Section 3 introduces a solution to this issue; Section 4 discusses some other factors relating to irregular current injection; Section 5 summarizes the results obtained from the previous theoretical analyses; Section 6 verifies the solution by both simulations and experiments; and finally, a conclusion is drawn.

2. Compatibility Issue of Irregular Current Injection Methods

2.1. Compatibility Issue

Figure 1 shows a diagram of multi-DG operation, where all the presented irregular currents/voltages are of the same frequency. The closing and opening of switch S_g represents an interconnection and an island state, respectively. Under an interconnection state, the equivalent network impedance Z_{eq} (specifically represented by $Z_{eq(grid)}$) is equal to the parallel impedance of load impedance Z_{load} and grid impedance Z_{grid}; while under an island state, Z_{eq} (specifically represented by $Z_{eq(island)}$) is equal to Z_{load}. Since Z_{grid} is much smaller than Z_{load}, $Z_{eq(grid)}$ is also smaller than $Z_{eq(island)}$. Accordingly, an island event can be determined by a surge of $|Z_{eq}|$.

On the other hand, according to the equation below, where $\dot{I}_{agg\_ir}$ and $\dot{U}_{ir}$ are the aggregate irregular current and the measured irregular voltage, respectively, the surge of $|Z_{eq}|$ can be reflected

by that of U_{ir} [5,6]. In contrast to $|Z_{eq}|$, U_{ir} can be measured directly. Hence, DG units monitor U_{ir} or calculate $|Z_{eq}|$ through the equation below to detect an island. In terms of this, in any case, the performance of $\dot{U}_{ir}$ is critical.

$$\dot{U}_{ir} = \dot{I}_{agg\_ir} Z_{eq}$$

As shown in Figure 1, in an island condition, there is the following equation:

$$\dot{U}_{ir} = (\dot{I}_{DG1} + \ldots + \dot{I}_{DGi} + \ldots + \dot{I}_{DGN}) Z_{eq(island)} = \dot{I}_{agg\_ir} Z_{eq(island)}$$

In existing irregular current injection methods, $\dot{I}_{DG1}, \ldots,$ and $\dot{I}_{DGN}$ are independent of each other, and in particular, their phases are not coordinated, for which reason they may cancel each other out, and I_{agg_ir} may be even smaller than individual injected irregular currents (magnitude). If I_{agg_ir} is so small that the expression below is established, where U_{th_i} is the threshold that DGi ($1 \le i \le N$) unit uses to determine an island, the DGi unit will be unable to detect the island:

$$U_{ir} = I_{agg\_ir} |Z_{eq(island)}| < U_{th\_i}$$

Hence, an issue with irregular current injection methods is how to avoid the mutual offset between irregular currents in multi-DG operation, i.e., the compatibility issue with such methods. This issue has been mentioned to a certain extent in [25]. Nevertheless, a more systematic study is needed. If this issue is solved, the islanding detection performance of a DG unit in multi-DG operation will not be lower than in single-DG operation.

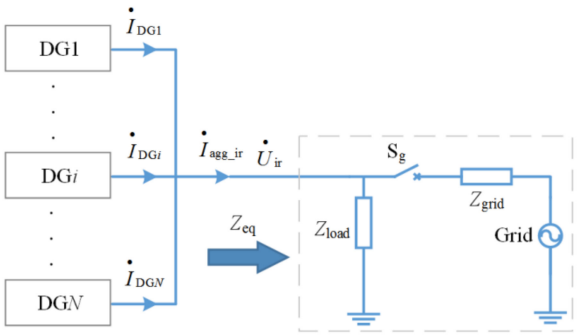


Figure 1. Irregular currents and voltage in multi-DG operation.

2.2. Requirement Resulting from the Compatibility Issue

As shown in Figure 1, the compatibility requires that (1) should be met:

$$I_{agg\_ir} > I_{DGi}, 1 \le i \le N \quad (1)$$

Before studying how to satisfy this inequality, there are the following suppositions:

$$\dot{I}_{DGi} = I_{DGi} \angle \phi_i$$

$$\Delta\phi_{ij} = \phi_i - \phi_j$$

And then there is:

$$I_{agg\_ir} = |\sum_{i=1}^{N} \dot{I}_{DGi}| = \sqrt{\sum_{i=1}^{N} {I_{DGi}}^2 + 2\sum_{i=1}^{N} I_{DGi} \sum_{j=i+1}^{N} I_{DGj} \cos \Delta\phi_{ij}}$$

It can be seen that the optimal condition is $\Delta\phi_{ij} = 0$, by which all the injected currents are in phase and the maximum I_{agg_ir} can be obtained. This condition has been discussed in [26]. However, a general condition is that $\Delta\phi_{ij}$ (in rad), i.e., the phase difference between any two injected irregular currents, is just in the $[-\pi/2, \pi/2]$ interval in order to ensure (1). This condition is what will be discussed in this paper.

3. A Solution to the Compatibility Issue

Considering that there is no communication between DG units, to make the aforementioned phase difference within $[-\pi/2, \pi/2]$, a common reference quantity is introduced to conduct irregular current injection. The terminal voltage of DG units, i.e., utility grid voltage, is a natural reference throughout the available quantities. This section will expound how to obtain compatibility on the basis of a terminal voltage reference.

3.1. Injection Pattern

In this paper, for a DG unit, such as an inverter, in order to facilitate the implementation, an irregular current is injected in this pattern: the first zero phase of the irregular current i_{ir} lags a zero phase of the terminal voltage u_{tm} by T_{lag} (time), which is less than a period of both i_{ir} and u_{tm}, as shown in Figure 2. T_{lag} is expressed in terms of time rather than angle because the frequencies of the irregular current and terminal voltage may be different. Additionally, it is found that other injection patterns based on a terminal voltage reference can actually be attributed to this pattern.

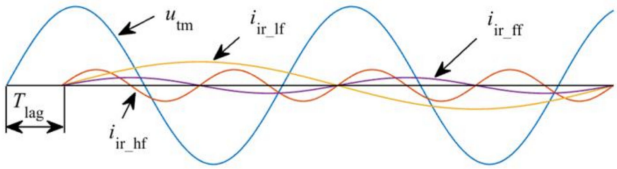


Figure 2. Injection pattern of irregular currents. u_{tm}: terminal voltage; i_{ir_hf}: high frequency current; i_{ir_lf}: low frequency current; i_{ir_ff}: negative sequence fundamental frequency current.

The following takes the DG1 and DG2 units in Figure 1 as an example to analyze how to achieve the mentioned phase difference requirement. If i_{DG1} and i_{DG2} are injected one after the other, the resultant waveforms are shown in Figure 3.

The relationship in (2) can be obtained from Figure 3:

$$T_{Pu} = nT_{Piir} + kT_{Piir.} \tag{2}$$

where T_{Pu} and T_{Piir} are the periods of the terminal voltages and irregular currents, respectively; m is a positive integer; n is a non-negative integer; and there are:

$$\begin{cases} n \geq m \geq 1 \text{ and } -1/2 \leq k \leq 1/2, \text{ for high frequency currents} \\ m \geq n \geq 0, \ m \geq 1, \text{ and } -1/2 \leq k \leq 1/2, \text{ for low frequency currents} \\ n = m \geq 1 \text{ and } k = 0, \text{ for negative sequence fundamental frequency currents} \end{cases}$$

Mathematically, in Equation (2), n and kT_{Piir} can be seen as the quotient and remainder of mT_{Pu} divided by T_{Piir}, respectively. The relationship between m and n can be obtained from Figure 3 and the relationship between T_{Pu} and T_{Piir}. For example, for high frequency currents, there is $T_{Pu} > T_{Piir}$. If $n < m$, there will be $n + k < m$, and then Equation (2) cannot be established. Thus, there must be $n \geq m$.

Equation (2) can be also rewritten as in (3), where f_u and f_{iir} are the frequencies of the terminal voltages and irregular currents, respectively, i.e., $1/T_{Pu}$ and $1/T_{Piir}$.

$$f_{iir}/f_u = (n + k)/m \tag{3}$$

To obtain compatibility, from Figure 3, k should be in the [−1/4, 1/4] interval, since it corresponds to $\Delta\phi_{12}$ (i.e., the phase difference mentioned in Section 2.2) in the [$-\pi/2$, $\pi/2$] interval. f_u is certain and m represents the number of voltage cycles, which means m may be any positive integer. Thus, for a given f_{iir}, if any value of m (i.e., any positive integer) can make k within [−1/4, 1/4] according to (3), this f_{iir} is usable, otherwise it is unsuited to be used as an irregular current frequency. In other words, a usable f_{iir} must be verified by all values of m, whereas an unusable f_{iir} only needs to be verified by one value of m.

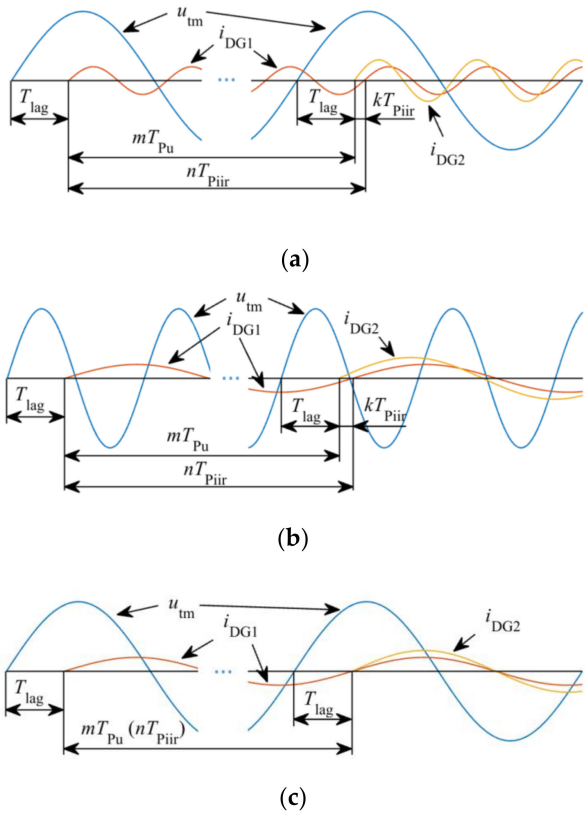


Figure 3. Scenarios that two irregular currents are injected. (**a**) High-frequency currents; (**b**) Low-frequency currents; (**c**) Negative sequence fundamental frequency currents.

3.2. High-Frequency Current

Equation (4) can be obtained by substituting $m = 1$ into (3):

$$f_{iir}/f_u = n_1 + k_1 \tag{4}$$

where n_1 and k_1 represent n and k when $m = 1$, respectively, as is the case hereafter; n_1 is a positive integer due to $f_{iir} > f_u$; and $-1/2 \le k_1 \le 1/2$ in accordance with (2).

According to the conclusion in Section 3.1, k_1 should be in [−1/4, 1/4]. Thus, f_{iir} which makes k_1 outside this interval is unusable and is not considered below.

Then, by substituting $m = 2$ into (3), there is (5):

$$f_{iir}/f_u = (n_2 + k_2)/2 \tag{5}$$

where n_2 is an integer greater than 1 and $-1/2 \le k_2 \le 1/2$.

The equation below can be derived from (4) and (5):

$$n_2 + k_2 = 2n_1 + 2k_1$$

So far, k_1 has been constrained to be in [−1/4, 1/4], and thus, according to the above equation, Equation (6) is true considering that n_1 and n_2 are non-negative integers:

$$k_2 = 2k \tag{6}$$

For $m = 2$, k_2 should be also within [−1/4, 1/4]. Thereupon, the usable interval of k_1 is compressed into [−1/8, 1/8] due to the above relationship, and the f_{iir} corresponding to those k_1 that have been filtered out will no longer be considered.

As above, when $m = 3$, the usable interval of k_1 is further compressed into [−1/12, 1/12]. Hence, the usable intervals of k_1 with the increase of m can be shown below.

m	Usable intervals of k_1
1	[−1/4, 1/4]
2	[−1/8, 1/8]
⋮	⋮
h	−1/(4h), 1/(4h)]
⋮	⋮

When $m \to +\infty$, k_1 can only be taken to zero, which means that k_2 can only be zero due to (6), and the same is true for $k_3, k_4, \ldots$. Consequently, considering—(4) and (5), there are the following equations:

$$\begin{cases} f_{\text{iir}} / f_{\text{u}} = n_1, \text{ when } m = 1 \\ f_{\text{iir}} / f_{\text{u}} = n_2/2, \text{ when } m = 2 \\ \vdots \\ f_{\text{iir}} / f_{\text{u}} = n_{\text{h}}/h, \text{ when } m = h \\ \vdots \end{cases}$$

Since a usable f_{iir} must be verified by all values of m, a usable f_{iir} must satisfy all of the above equations. Through the intersection operation on the above equations, the final expression of the usable f_{iir} can be derived, as shown in (7):

$$f_{\text{iir}} = pf_{\text{u}} \tag{7}$$

where p is an integer greater than 1.

The above expression shows that only the frequencies that are integer multiples of the terminal voltage frequency are usable for high frequency currents.

3.3. Low-Frequency Current

In the same way, when $m = 1$, (4) is still true, and for low frequency currents, there are $n_1 = 1$ or 0, and $-1/2 \le k_1 \le 1/2$ and $k_1 \neq 0$.

By following the derivation in Section 3.2, it can be found that there is not a suitable value for k_1 considering $k_1 \neq 0$. In other words, low frequency currents are unsuited to be used as injected currents.

3.4. Negative Sequence Fundamental Frequency Currents

This type of current only exists in three-phase systems. Up to now, such currents have seemed to be usable, since (2) indicated that $k = 0$, i.e., within [−1/4, 1/4].

3.5. Practical Applications in Three-Phase Systems

In inverter-based three-phase DG systems, due to a lack of a relevant knowledge, carelessness or some other reasons, there may be a fault whereby the phase symbols of an inverter do not correspond

to that of the system, while their phase sequence is the same. This fault is called a phase symbol fault in this paper, and it cannot be detected by a DG unit itself or even be seen as a fault. This scenario, as DG2 and DG3 units shown in Figure 4, is acceptable in terms of generation. Accordingly, irregular current injection islanding detection methods must also be able to tolerate this fault. As for the fault that a DG unit mismatches the phase sequence, as the DG4 unit shown in Figure 4, it will be detected by the DG unit. Depending on the technical route, the DG unit may adjust its inner phase sequence to adapt this fault, by which this fault is translated into a phase symbol fault, or the DG unit may refuse to start and issue a warning. Accordingly, this fault is seen as a phase symbol fault below.

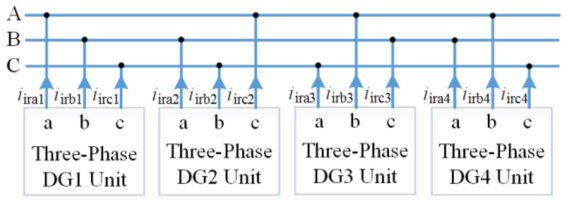
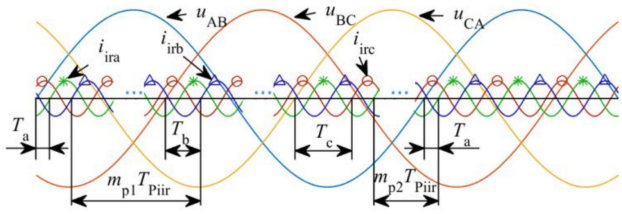


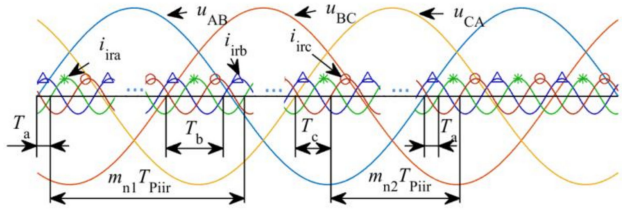
Figure 4. Multiple three-phase DGs.

(1) Positive Sequence High-Frequency Currents: We take the DG1 unit in Figure 4 as an example, where the reference terminal voltages of the irregular currents i_{ira1}, i_{irb1} and i_{irc1} are the line voltages (i.e., phase-to-phase voltage) u_{AB}, u_{BC} and u_{CA} respectively, and T_{lag} is appointed as T_a, T_b and T_c, respectively.

The time interval between the zero phase of a reference terminal voltage and the zero phase of an irregular current immediately following it is defined as the zero phase interval hereafter. The first zero phase interval must be T_{lag} for an irregular current in accordance with the aforementioned injection pattern, and once (7) is met, each subsequent zero phase interval will be T_{lag}. Thus, the positive sequence irregular current injection is shown in Figure 5a.



(**a**)



(**b**)

Figure 5. Injection of three-phase irregular currents. (**a**) Positive sequence irregular current; (**b**) Negative sequence irregular current.

In Figure 5, the phase difference of $2\pi/3$ between any two irregular currents corresponds to a time of $T_{Piir}/3$, while the phase difference of $2\pi/3$ between any two voltages corresponds to a time of $T_{Pu}/3$. Accordingly, Equations (8) can be obtained from Figure 5a:

$$\begin{cases} T_b = T_a + T_{Piir}/3 + m_{p1}T_{Piir} - T_{Pu}/3 \\ T_c = T_a + T_{Pu}/3 - T_{Piir}/3 - m_{p2}T_{Piir} \end{cases} \quad (8)$$

where m_{p1} and m_{p2} are non-negative integers, and each non-negative integer may be the value of m_{p1} and m_{p2}. For a certain irregular current (i.e., with a certain T_{Piir}), T_b and T_c are determined by T_a. Consequently, only T_a needs to be set for three-phase DG units.

In Figure 4, the actual reference terminal voltage of both i_{irb1} and i_{ira2} is u_{BC}, while their T_{lag} are T_b and T_a, respectively. To make the phase difference between i_{irb1} and i_{ira2} within $[-\pi/2, \pi/2]$ for they converge in phase B, the time difference between the zero phases of i_{irb1} and i_{ira2} should be in $[-T_{Piir}/4, T_{Piir}/4]$. Therefore, the inequality below should be satisfied, where T_{int} can be one value of 0, $-T_{Piir}$ and T_{Piir}, and the three values correspond to the three scenarios shown in Figure 6:

$$-T_{Piir}/4 \le T_b + T_{int} - T_a \le T_{Piir}/4$$

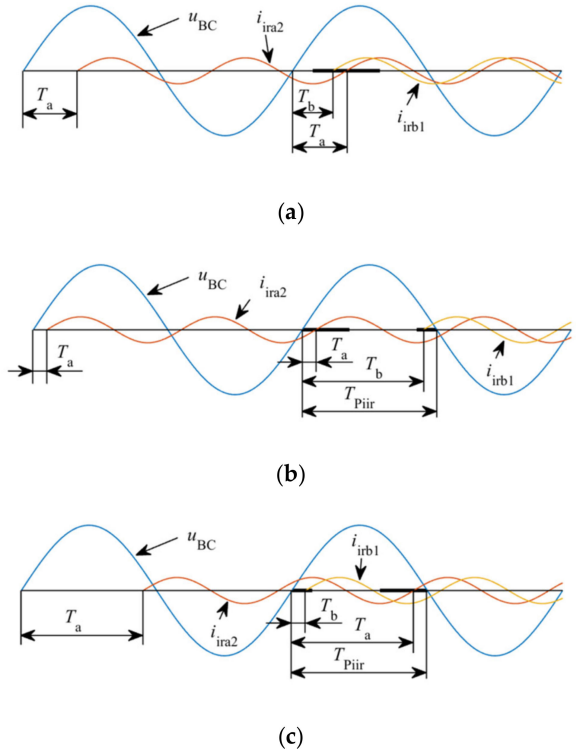


Figure 6. Possible relationship between T_a and T_b to achieve the mentioned phase difference. (**a**) $T_{int} = 0$; (**b**) $T_{int} = -T_{Piir}$; (**c**) $T_{int} = T_{Piir}$. The bold lines represent the proper position for the first zero phase of i_{irb1} to make the phase difference between i_{irb1} and i_{ira2} within $[-\pi/2, \pi/2]$.

Then, Equation (9) can be derived from the above inequality and (8), where q is a positive integer. For the other irregular currents in Figure 4, this equation can also be derived:

$$f_{iir}/f_u = 3q + 1 \tag{9}$$

(2) Negative Sequence Fundamental/High-Frequency Currents: The injection of such currents is shown in Figure 5b. As in (8), there are similar equations, as shown in (10):

$$\begin{cases} T_b = T_a + m_{n1}T_{Piir} - T_{Pu}/3 - T_{Piir}/3 \\ T_c = T_a + T_{Pu}/3 + T_{Piir}/3 - m_{n2}T_{Piir} \end{cases} \tag{10}$$

where m_{n1} and m_{n2} are non-negative integers, and each non-negative integer may be the value of m_{n1} and m_{n2}.

By following the derivation for positive sequence high frequency currents above, Equation (11) can be obtained:

$$f_{\mathrm{iir}}/f_{\mathrm{u}} = 3q - 1 \tag{11}$$

Equations (9) and (11) show further constraints on the frequencies of positive sequence current and negative sequence current, respectively. In addition, since the right side of (11) cannot be 1, the negative sequence fundamental frequency currents are unusable.

3.6. Practical Applications in Single-Phase Systems

For ease of use, the parameters of a single-phase DG unit, including the T_{lag}, do not need to be modified when the phase that it is connected to is changed. Thus, the single-phase DG units in Figure 7 must adopt the same T_{lag}, which is denoted as T_{l} in this paper. Since a single-phase DG unit can distinguish a live wire from a neutral wire, there is not a phase symbol fault as above.

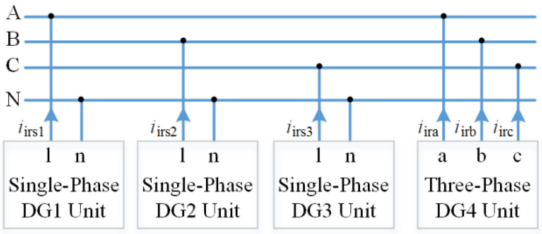


Figure 7. Hybrid of single-phase and three-phase DG.

Meanwhile, single-phase DG units should be compatible with three-phase DG units. Thus, in Figure 7, the phase difference between irregular currents i_{irs1} and i_{ira} must be in $[-\pi/2, \pi/2]$ (i.e., the time difference between the zero phases of i_{irs1} and i_{ira} should be in $[-T_{\mathrm{Piir}}/4, T_{\mathrm{Piir}}/4]$), as for the other irregular currents. Since the reference terminal voltage of a single-phase DG unit is a phase voltage, e.g., u_{AN} for i_{irs1}, considering that u_{AN} lags u_{AB} by $\pi/6$ (time of $T_{\mathrm{Pu}}/12$), as shown in Figure 8, T_{l} should be set as (12), where m_{a} (as well as m_{b} and m_{c}, to be mentioned later) is an integer.

$$-T_{\mathrm{Piir}}/4 \le (T_{\mathrm{l}} + T_{\mathrm{Pu}}/12) - T_{\mathrm{a}} - m_{\mathrm{a}}T_{\mathrm{Piir}} \le T_{\mathrm{Piir}}/4 \tag{12}$$

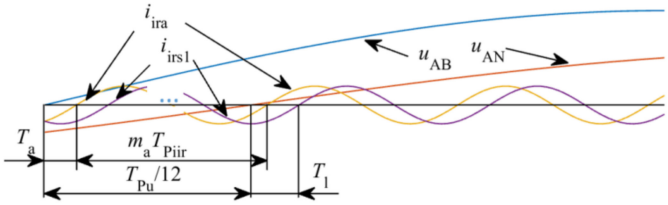


Figure 8. Relationship between T_{a} and T_{l}.

Moreover, for phases B and C, the relationships below should be met:

$$-T_{\mathrm{Piir}}/4 \le (T_{\mathrm{l}} + T_{\mathrm{Pu}}/12) - T_{\mathrm{b}} - m_{\mathrm{b}}T_{\mathrm{Piir}} \le T_{\mathrm{Piir}}/4$$

$$-T_{\mathrm{Piir}}/4 \le (T_{\mathrm{l}} + T_{\mathrm{Pu}}/12) - T_{\mathrm{c}} - m_{\mathrm{c}}T_{\mathrm{Piir}} \le T_{\mathrm{Piir}}/4$$

As (12) is mandatory with the setting of T_{l}, the main thing is how to ensure that the above two inequalities are true. If i_{ira}, i_{irb} and i_{irc} in Figure 7 are positive sequence currents, by substituting (8) into the above two inequalities and considering (12), a relationship like (9) can be derived with regard to f_{iir}. In addition, if i_{ira}, i_{irb} and i_{irc} are negative sequence currents, by substituting (10) into the above

two inequalities and considering (12), a relationship like (11) can be derived. In other words, the frequencies determined by (9) and (11) (disregarding the phase sequence) are usable for single-phase DG units.

After the above analysis, it is found that the usable irregular currents are those with the frequencies determined by (7), i.e., integer multiple harmonics. The orders of $3q + 1$ are assigned to positive sequence currents and single-phase currents, while the orders of $3q - 1$ are assigned to negative sequence currents and single-phase currents, and the remainder are the orders of $3q$. It seems that the orders of $3q$ can be used by single-phase currents, since they are used by neither positive sequence nor negative sequence currents and there is no compatibility issue between irregular currents at different frequencies. The following will study whether it is feasible.

As shown in Figure 7, it is assumed that the magnitudes of i_{irs1}, i_{irs2} and i_{irs3} are the same. Their injections are shown in Figure 9, where i_{irs1} leads i_{irs2} by T_{12} (Time); i_{irs2} leads i_{irs3} by T_{23}; and m_s is a non-negative integer.

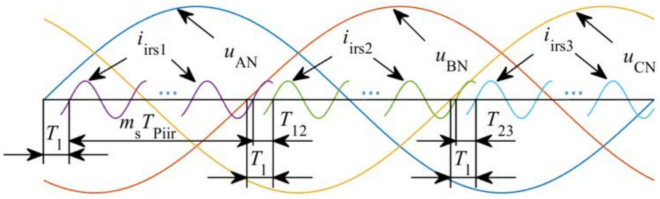


Figure 9. Phase relationship between the single-phase irregular currents.

From Figure 9, there is the following relationship:

$$m_s T_{Piir} + T_{12} = T_{Pu}/3$$

It can be rewritten as the following equation, where $0 \le T_{12}/T_{Piir} < 1$:

$$T_{12}/T_{Piir} = f_{iir}/(3f_u) - m_s$$

By substituting the preceding mentioned three sets of frequencies into the above equation, the results of T_{12}/T_{Piir} can be obtained below:

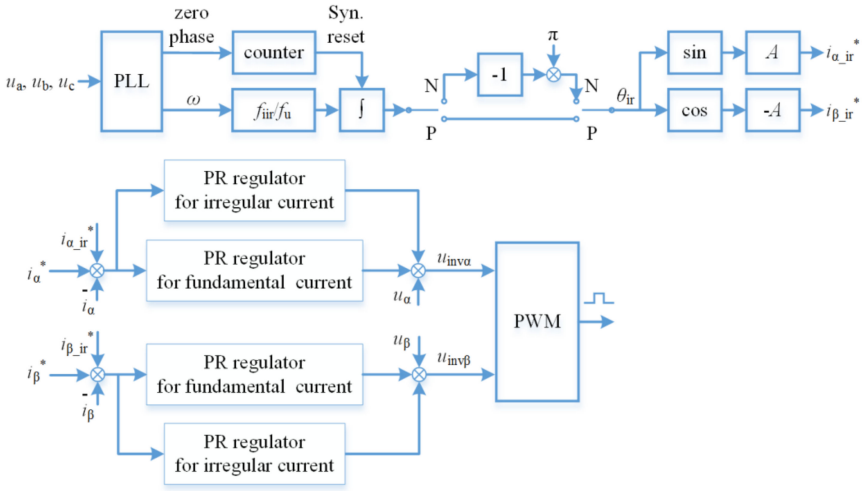
$$\frac{T_{12}}{T_{Piir}} = \begin{cases} 1/3, \text{ if } f_{iir} = (3q+1)f_u \\ 0, \text{ if } f_{iir} = 3qf_u \\ 2/3, \text{ if } f_{iir} = (3q-1)f_u \end{cases}$$

For T_{23}/T_{Piir}, the same results as above can be obtained by following the preceding derivation. These results reflect that if the frequency of i_{irs1}, i_{irs2} and i_{irs3} is $(3q + 1)f_u$, i_{irs1} leads i_{irs2} by $2\pi/3$ while i_{irs2} leads i_{irs3} by $2\pi/3$, which means that i_{irs1}, i_{irs2} and i_{irs3} are present as a set of positive sequence currents in the system; if their frequency is $(3q - 1)f_u$, they will present as a set of negative sequence currents, and if their frequency is $3qf_u$, they will present as a set of zero sequence currents. However, zero sequence currents may bring some problems to the system. For example, they may affect zero-sequence relay protection [27]. When the single-phase DG units are evenly distributed on the three-phase lines, i_{irs1}, i_{irs2} and i_{irs3} are likely to possess the same or similar magnitudes. Accordingly, for the frequencies of single-phase currents, the orders of $3q$ are not recommended.

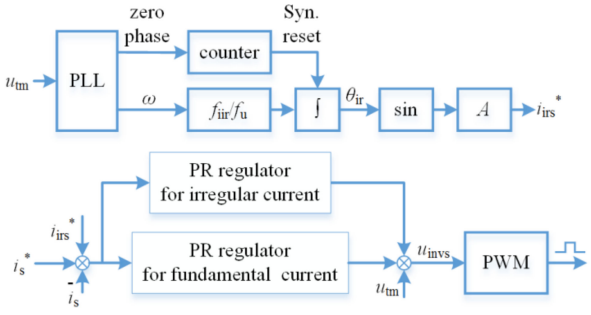
3.7. Implementation of the Proposed Solution

For inverter-based DG units, since both fundamental currents and irregular currents are sinusoid, to simplify the control, PR regulation based on α-β reference frame is suggested. The control block diagrams are shown in Figure 10.

In Figure 10a, P and N denote the connection position of the multi-route switches when injecting positive sequence and negative sequence irregular currents, respectively, and A denotes the amplitude of the irregular current. To avoid the accumulation of phase errors resulting from the measurement errors of voltage frequency (i.e., ω), the irregular current phase θ_{ir} should be reset periodically (shown as Syn. reset in Figure 10). For an irregular current whose frequency is an integer multiple of the voltage frequency, the irregular current phase should be reset once every voltage cycle. In addition, for the other irregular currents, for example, a current at 75 Hz, since two voltage (50 Hz) cycles include an integer number (three) cycles of this irregular current, the irregular current phase should be reset once every two voltage cycles. The counter in Figure 10 is used for counting voltage cycles.



(**a**)



(**b**)

Figure 10. Implementation of the proposed solution. (**a**) For three-phase inverters; (**b**) For single-phase inverters.

4. Other Factors Relating to Irregular Current Injection

(1) Mixed with Existing Irregular Current Injection Methods: Since the irregular currents based on existing methods are not injected according to the proposed solution, they may offset the irregular currents injected according to the solution. Thus, the islanding detection effect will not be improved if there are few DG units employing the proposed solution. In terms of this problem, manufacturers are strongly encouraged to adopt the proposed solution.

(2) T_{lag}: A unified T_{lag} is critical for the compatibility. This paper has indicated that T_a and T_l should meet (12). However, no performance index has been found related to T_{lag}, and thus there is not

a best value for T_{lag}. Accordingly, at present, a feasible way is to specify a value for it by the grid code makers. For example, T_{a} and T_{l} can be set as in Equation (13).

$$\begin{cases} T_{\text{a}} = T_{\text{Pu}}/12 \\ T_{\text{l}} = 0 \end{cases} \tag{13}$$

(3) Resonant Frequency of the Filter of an Inverter: For the most common voltage source inverters, essentially, the irregular current is excited by an output voltage component with the same frequency. Therefore, for an inverter adopting a LC or LCL filter, its irregular current frequency should avoid the resonant frequency of the filter so as not to cause a current spike [28].

(4) Variation of the Grid Impedance: Some literature has pointed out that grid impedance is frequency-variant, and may be larger than the load impedance at a large enough frequency [4,20]. From this point of view, the irregular current frequency should be as small as possible, since a small grid impedance is a necessary condition for irregular current injection methods.

(5) Large Line Impedance: There may be a large line impedance between DG units that are far from each other, by which the terminal voltages of these DG units may be out of phase and thereby the irregular currents cannot be controlled as accurately as expected. At present, there is no good solution to this problem without communication.

5. Discussion on the Proposed Solution

A solution to the compatibility issue can be summarized as the following three points:

(1) The terminal voltage of a DG unit is referenced, and the injection pattern of irregular currents is shown in Figure 2;
(2) The usable frequency orders for irregular currents are shown in Table 1;
(3) The used frequency should be as low as possible.

Furthermore, as a specific implementation of the proposed solution, the block diagram in Figure 10 can be employed by inverters.

In the meantime, it can be seen that along with the growing penetration of low and medium power DG units, particularly those of the plug and play variety, manufacturers, grid code makers and grid operators should cooperate to get both a satisfactory islanding detection effect.

This solution largely solves the compatibility issue, although not completely. In other words, if the phases of the irregular currents are still not managed as they are now, the effect of irregular current injection methods will be uncontrollable in multi-DG operation.

Table 1. Usable frequency orders for irregular currents.

Irregular Currents	Usable Orders [1]
Three-phase positive sequence currents	$3q + 1$
Three-phase negative sequence currents	$3q - 1$
Single-phase currents	$3q \pm 1$

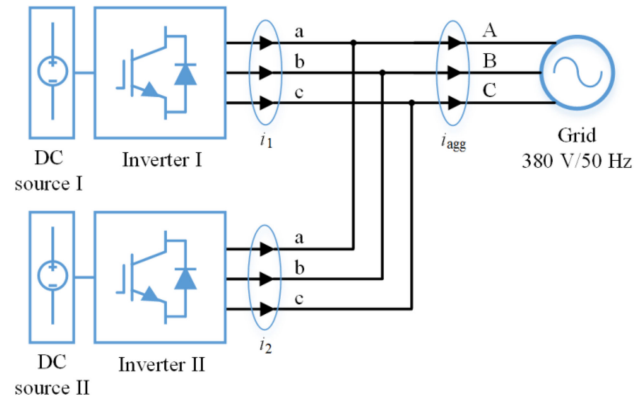
[1] q is a positive integer.

6. Simulations and Experiments

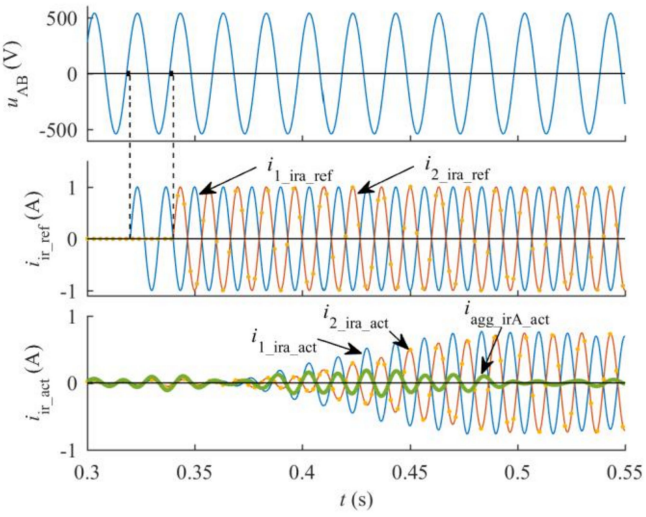
The proposed solution is implemented according to Figure 10 and T_{lag} is set as Equation (13).

6.1. Simulations

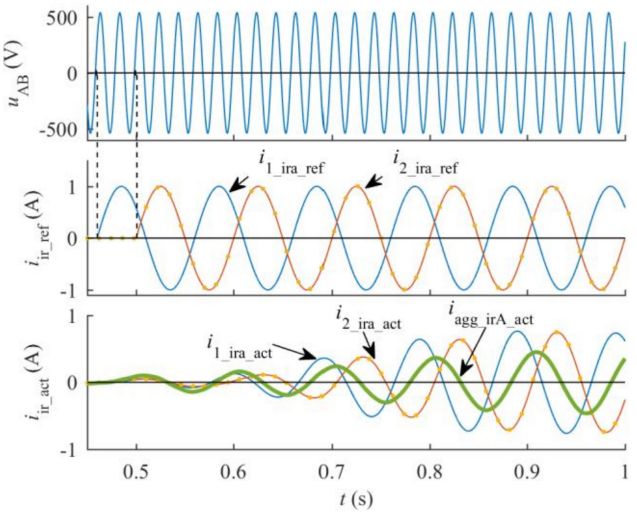
The three-phase inverter-based simulation platform is based on Matlab/Simulink (Matlab R2018a, Mathworks, Natick, MA, USA). The main circuits shown in Figures 11a and 12a represent a normal connection and a phase symbol fault, respectively.



(**a**)

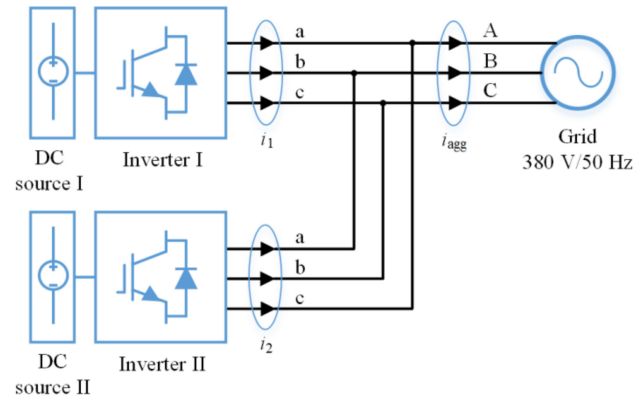


(**b**)

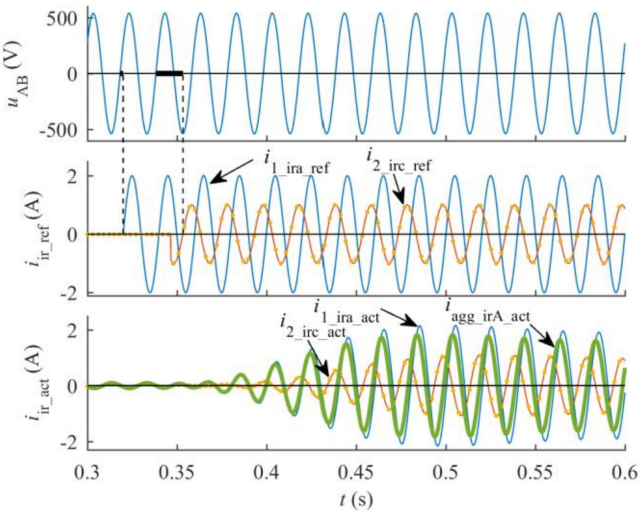


(**c**)

Figure 11. Waveforms under normal connection. (**a**) Main circuit; (**b**) Positive sequence high-frequency current (75 Hz); (**c**) Positive sequence low-frequency current (10 Hz). u_{AB}: reference terminal voltage (50 Hz). The meaning of the subscripts: ref, reference current; act, actual current; ira, irregular current of phase a; agg, aggregate current.



(**a**)



(**b**)

Figure 12. Waveforms under a phase symbol fault. (**a**) Main circuit with a phase symbol fault; (**b**) Negative sequence fundamental frequency current (50 Hz).

6.1.1. Tests under a Normal Connection

Positive sequence high frequency current (75 Hz) and positive sequence low frequency current (10 Hz) are tested. The simulation results are shown in Figure 11b,c, where the irregular current of each branch and their convergence are in phase A. The waveforms of i_{ir_act} are obtained by filtering (Band Pass) the output currents (i.e., i_1, i_2 and i_{agg}) in Figure 11a. The results show that the reference irregular currents i_{ir_ref} are generated in the predetermined manner, and the actual irregular currents i_{ir_act} are well controlled in terms of tracing performance. In the meantime, the aggregate irregular current $i_{agg\_irA\_act}$ is distinctly smaller than both of the branch irregular currents $i_{1\_ira\_act}$ and $i_{2\_ira\_act}$, which means that irregular currents at these two frequencies are unusable for islanding detection.

6.1.2. Tests under a Phase Symbol Fault

To simulate a phase symbol fault, the terminal phases a/b/c of inverter II are connected to the phases B/C/A of the power grid, respectively, as shown in Figure 12a. The test of negative sequence fundamental frequency current (50 Hz) is based on this circuit. The simulation results are shown in Figure 12b, where $i_{1\_ira\_act}$ and $i_{2\_irc\_act}$ converge on phase A and their T_{lag} are T_a and T_c, respectively. From the results, the reference irregular currents are still generated in the predetermined manner, and

the actual irregular currents are also well controlled. Additionally, the aggregate current $i_{agg\_irA\_act}$ is smaller than $i_{1\_ira\_act}$. In other words, the aggregate current is pulled down with the injection of $i_{2\_irc\_act}$. Thus, this irregular current is unusable when considering phase symbol faults.

In summary, the control of the irregular currents has reached the expected effect. As for unusable frequencies, the simulation results are consistent with the previous conclusions.

6.2. Experiments

6.2.1. Tests under a Normal Connection

This set of tests are based on the circuit in Figure 11a. From Figure 10, the related parameters are shown in Table 2, where k_P and k_R are the proportional and resonant coefficients of the PR regulators for fundamental currents, respectively; k_{P_ir} and k_{R_ir} are the proportional and resonant coefficients of the PR regulators for irregular currents, respectively; A_I and A_{II} are the amplitude of the irregular currents output by inverters I and II, respectively; and f_{PWM} is the switching frequency.

Table 2. Related parameters of the inverters.

k_P	k_R	k_{P_ir}	k_{R_ir}	A_I (A)	A_{II} (A)	f_{PWM} (kHz)
17.7	3289	5.06	1012	0.6/0.8	0.3/0.5	10

Moreover, in order to be more realistic, a hybrid of fundamental current and irregular current will be output by each inverter, and both the inverters are based on unity power factor control. Inverter I outputs a fundamental current of 5 A (amplitude) while inverter II outputs 3.5 A.

(1) Positive Sequence 75 Hz Current: Inverter I outputs an irregular current of 0.6 A (amplitude) while inverter II outputs 0.3 A. The experimental results are shown in Figure 13, where the irregular currents i_{1_ira}, i_{2_ira}, i_{agg_irA}, i_{1_irb}, i_{2_irb} and i_{agg_irB} are extracted from i_{1_a}, i_{2_a}, i_{agg_A}, i_{1_b}, i_{2_b} and i_{agg_B}, respectively. This extraction is realized through offline filtering of the currents at other frequencies (by band pass filters) and the opposite phase sequence current at the same frequency (by delayed signal cancellation algorithm) [29]. Although the filtered data will have a phase deviation, they are generally applicable for analysis.

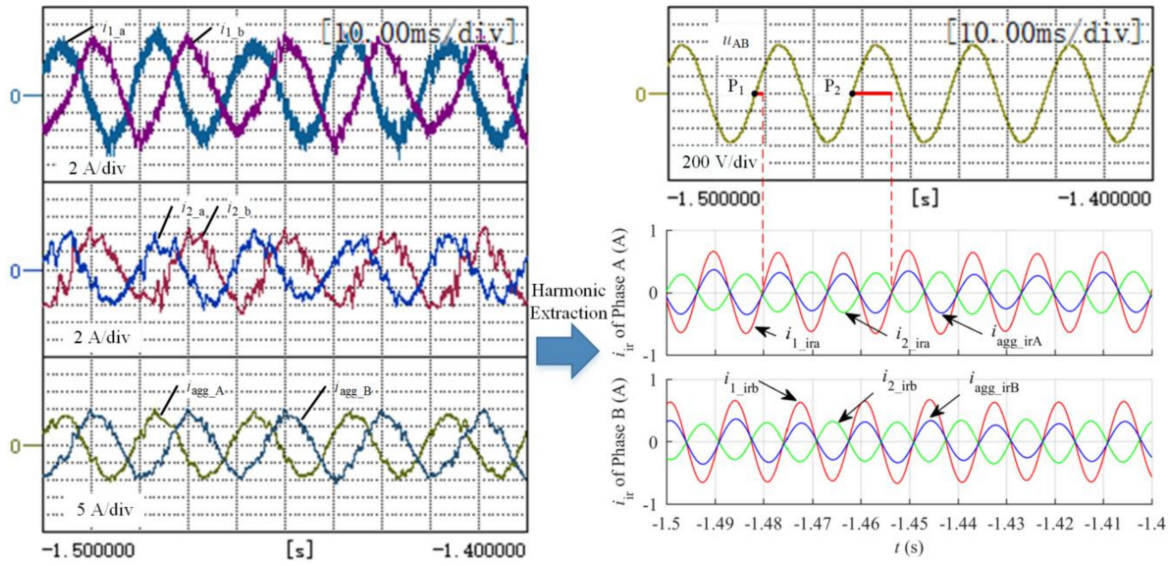


Figure 13. Actual positive sequence 75 Hz currents. Current i_{1_a} is output by the phase A of inverter I while i_{1_ira} is the irregular current therein, and the others can be analogized.

In the right side of Figure 13, the horizontal bold solid lines represent the zero phase interval, mentioned in Section 3.5, regarding i_{1_ira}. The zero phase interval near point P_1 (a zero phase of u_{ab}) is approximately $T_{Pu}/12$, and the one near point P_2 (another zero phase of u_{ab}) is approximately $5T_{Pu}/12$. It reveals that the zero phase intervals are different for this irregular current. Thereupon, if another irregular current starts to be injected after point P_1, it will be in phase with i_{1_ira} considering that T_a is set to $T_{Pu}/12$, whereas if it starts to be injected after point P_2, the phase difference between i_{1_ira} and it will not be within $[-\pi/2, \pi/2]$. This analysis reveals that the phase difference between such two currents injected at different times may be within or outside $[-\pi/2, \pi/2]$, and actually, both cases have occurred during the tests, although only the case whose phase difference is outside $[-\pi/2, \pi/2]$ is illustrated with Figure 13 (i_{1_ira} and i_{2_ira}). This phase difference is uncontrollable in applications, which is enough to indicate that this irregular current is unusable.

(2) Negative Sequence 10 Hz Current: The amplitudes of the irregular currents are the same as above. The experimental results are shown in Figure 14.

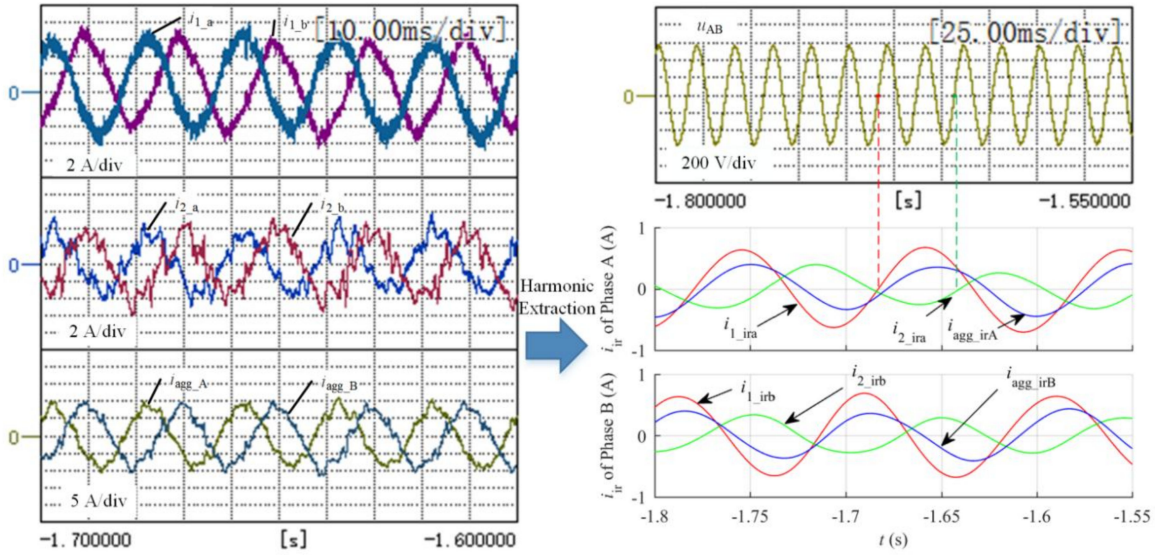


Figure 14. Actual negative sequence 10 Hz current.

In Figure 14, there are five cycles of u_{ab} in a cycle of i_{1_ira}. In other words, there are five zero phase points of u_{ab} in a cycle of i_{1_ira}. If another irregular current starts to be injected after one of the five zero phase points, the phase difference between i_{1_ira} and it is likely to be outside $[-\pi/2, \pi/2]$, as is the case shown in Figure 14 (i_{1_ira} and i_{2_ira}). This phase difference is still uncontrollable, which means that this irregular current is also unusable.

(3) Positive Sequence 200 Hz Current: Inverter I outputs such an irregular current of 0.8 A (amplitude) while inverter II outputs 0.5 A. The experimental results are shown in Figure 15.

In Figure 15, as mentioned in Section 3.5, every zero phase interval is the same for i_{1_ira} and i_{2_ira}, and is equal to T_a, i.e., $T_{Pu}/12$. Accordingly, i_{1_ira} and i_{2_ira} are in phase, as shown in Figure 15, and thereby this irregular current is usable.

(4) Negative Sequence 50 Hz Current: The amplitudes of the irregular currents are the same as above. The experimental results are shown in Figure 16.

In Figure 16, every zero phase interval is still the same. Thus, i_{1_ira} and i_{2_ira} are still in phase, and this irregular current is usable here.

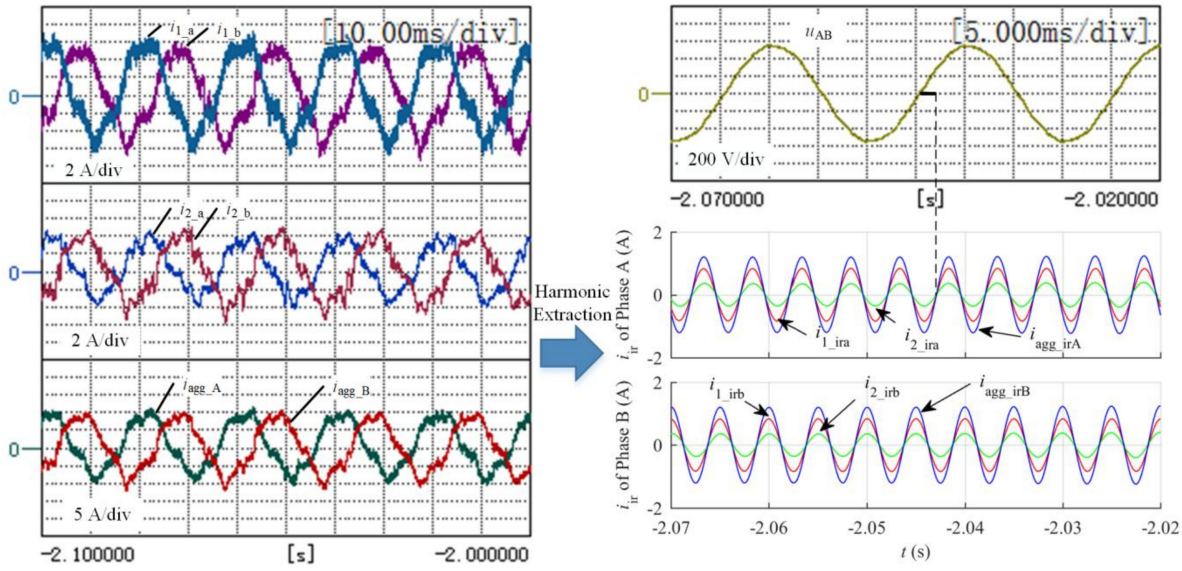


Figure 15. Actual positive sequence 200 Hz current.

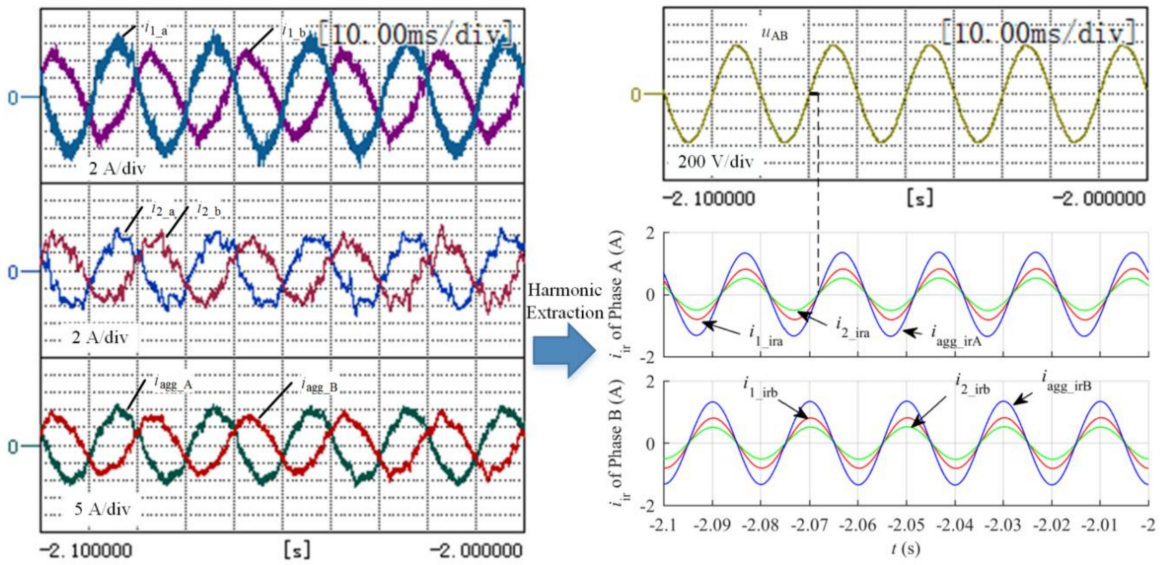


Figure 16. Actual negative sequence 50 Hz current.

6.2.2. Tests under a Phase Symbol Fault

This set of tests are based on the circuit in Figure 17. The related parameters and output of fundamental currents are the same as those in Section 6.2.1.

(1) Positive Sequence 200 Hz Current: Inverter I outputs an irregular current of 0.8 A (amplitude) while inverter II outputs 0.5 A. The experimental results are shown in Figure 18.

In Figure 17, i_{1_irc} and i_{2_ira} converge on phase A. According to the analyses in the previous subsection, the zero phase interval of i_{1_irc} is always T_c while that of i_{2_ira} is always T_a. At this point, there is exactly $T_a = T_c$. Accordingly, i_{1_irc} and i_{2_ira} are still in phase, as shown in Figure 18. Therefore, this irregular current is usable.

(2) Negative Sequence 50 Hz Current: The amplitudes of the irregular currents are the same as above. The experimental results are shown in Figure 19.

The zero phase intervals of i_{1_irc} and i_{2_ira} are still T_c and T_a, respectively. However, T_c is no longer equal to T_a. In Figure 19, i_{1_irc} approximately leads i_{2_ira} by $2\pi/3$, i.e., outside $[-\pi/2, \pi/2]$. Consequently, this irregular current is unusable, although it performs well under normal connection.

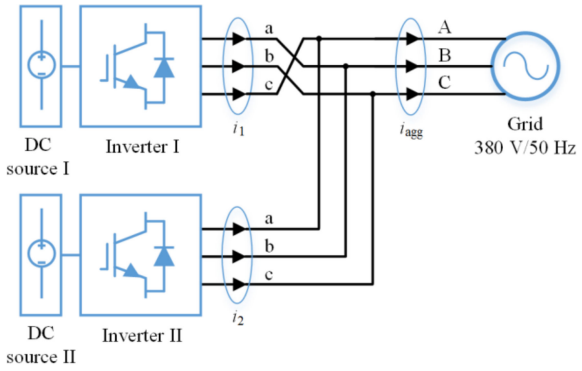


Figure 17. Main circuit in which inverter I has a phase symbol fault.

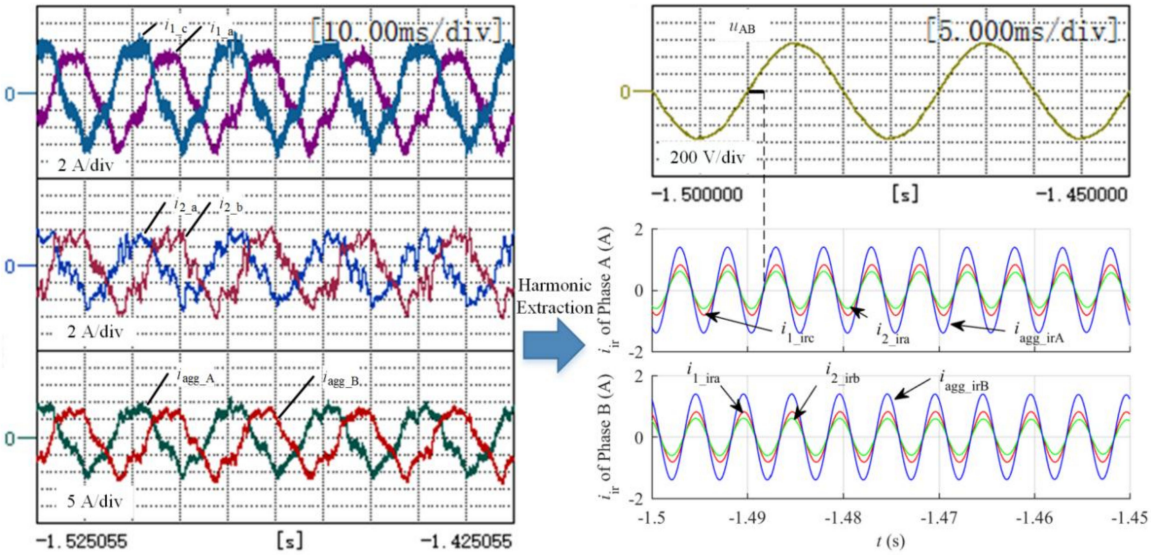


Figure 18. Actual positive sequence 200 Hz current.

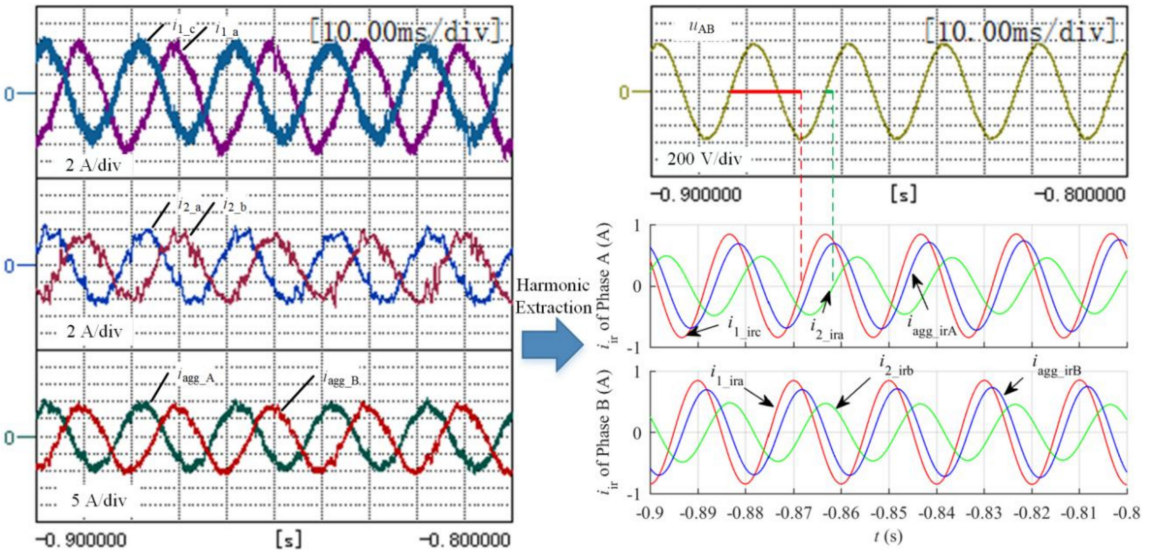


Figure 19. Actual negative sequence 50 Hz current.

Overall, of the several irregular currents tested, only the positive sequence 200 Hz current is usable, which is consistent with Table 1.

7. Conclusions

For irregular current injection islanding detection methods in multi-DG operation, if the phases of the injected irregular currents at the same frequency are not managed, the aggregate irregular current may be smaller than the individual injected irregular currents, which may result in a failed islanding detection. Accordingly, a compatibility issue is raised, which requires the phase difference between any two injected irregular currents within a certain interval. From this requirement, a solution is proposed, which references the terminal voltage of DG units to conduct irregular current injection and only employs the high frequency currents whose frequencies satisfy a certain constraint, as shown in Table 1. This solution can largely eliminate the phenomenon that irregular currents cancel each other out, and ensures that every injected irregular current can have a positive effect for islanding detection. Therefore, it is meaningful for practical applications. If this solution is employed, a good foundation will be laid for the next stage of islanding detection. Accordingly, a better effect and reliability can be expected.

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Conflicts of Interest: The authors declare no conflict of interest.

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