

RESEARCH ARTICLE

Assessment of photovoltaic junction position using combined focused ion beam and electron beam-induced current analysis of close space sublimation deposited CdTe solar cells

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ABSTRACT

A major limitation of the cross-section electron beam-induced current method—the use of roughly fractured surfaces to provide the cross-section—has been overcome with the use of focused ion beam microscope sample preparation. Using this method, it was possible to undertake a study of the relation between junction position and the corresponding external quantum efficiency (EQE) curves. For the case of cadmium telluride (CdTe) cells, it was demonstrated that the EQE curve shape that indicates a buried CdTe homojunction only arises if the junction is buried by more than 0.9 μm from the heterointerface. This highlights the limitations of interpreting EQE curve shape to determine junction position. It was also shown that extended postgrowth annealing degrades the cadmium sulfide by Kirkendall voiding, and this leads to efficiency loss. © 2014 The Authors. *Progress in Photovoltaics: Research and Applications* published by John Wiley & Sons, Ltd.

KEYWORDS

CdTe; EBIC; close space sublimation

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1. INTRODUCTION

Electron beam-induced current (EBIC) analysis is a scanning electron microscope-based technique wherein the current generated in a photovoltaic device under interrogation from an electron beam is recorded as a function of the beam position. This allows the electrical activity of electronic devices to be probed with submicron resolution. A number of variants of EBIC have been applied to solar cells such as front wall [1], back wall [2], cross-sectional and grain boundary EBIC (remote EBIC) [3,4]. Of these, cross-sectional EBIC is particularly useful as it allows direct visualisation of the device space charge region. Beam electrons incident on the space charge region are collected by the inbuilt electric field and flow through the external amplifier. This generates an EBIC current as

a function of beam position, with the peak of collection being observed at the strongest point of the inbuilt field. Manual preparation of cell cross-sections by cleaving of the glass often produces a rough surface [5], and it is invariably the case that the microscopy is to some extent compromised by surface morphology effects. In the case of cadmium telluride (CdTe) solar cells, damage caused to the soft CdTe layer by cleaving may introduce image contrast artefacts that obscure genuine sample-related effects, although a skilled operator may still produce useful results. An alternative to this is the use of focused ion beam (FIB) milling [6], to produce high quality cross-sectional cuts suitable for EBIC analysis. The use of FIB for EBIC sample preparation has previously been reported for microelectronics [7] and solar cells [8], and here, we use it as a characterisation tool for thin-film CdTe devices.

We also compare the information on junction position discernible by EBIC with external quantum efficiency (EQE) measurements. EQE measurements may be used to infer the junction position from the shape of the curve. For an EQE curve in which the response in the CdTe absorption range (~525–850 nm) is flat, or decreases for longer wavelengths, the junction is assumed to be at the CdTe/cadmium sulfide (CdS) interface. A ‘buried junction’ response is characterised by an increase in EQE towards longer wavelengths, often with a pronounced peak at the CdTe band edge [9]. This occurs when the active junction is a CdTe homojunction (i.e. p -CdTe/ n -CdTe) and is formed towards the device back surface. The more deeply penetrating photons (longer wavelength) are absorbed closer to the space charge region and thus are more likely to contribute to the EQE signal. The limitations of determining junction position from this technique are discussed.

In this work, a series of four close space sublimation (CSS) deposited CdTe solar cell devices with various cadmium chloride (CdCl₂) treatment times were compared using EBIC analysis of FIB-milled cross-sections to identify the junction position. For each device type, J - V and EQE measurements were performed prior to FIB milling and EBIC analysis. It was found that while the EQE curve shapes may infer a shallow junction, EBIC revealed that the junctions were buried by up to 0.9 μm .

1.1. Cell deposition

CdTe solar cell devices were fabricated in the ‘superstrate’ on commercial fluorine doped tin oxide-coated soda lime glass substrates (NSG C15 from NSG Ltd., Lathom, Ormskirk, Lancashire, UK). A ZnO buffer, or high resistivity transparent, layer was then added by reactively sputtering from a Zn target in the presence of oxygen. The CdS layer was deposited by RF sputtering using a power of 60 W and a substrate temperature of 200 °C. CSS deposition of the CdTe layer was performed in a custom all-quartz deposition chamber manufactured by Electro-Gas systems Ltd., (Stockport, Cheshire, England). Deposition was carried out at source and substrate temperatures of 615 °C and 520 °C, respectively, under a pressure of 30 Torr of nitrogen giving a thickness of ~4 μm . Prior to deposition of a 200 nm CdCl₂ layer by vacuum evaporation, the CdTe back surface was etched for 10 s in a nitric–phosphoric acid etch to remove any Cd-rich surface phases, which may inhibit Cl in-diffusion [10]. Postgrowth annealing was performed in air at 410 °C prior to the deposition of 0.25 cm² gold back contacts by vacuum evaporation. Prior to production of the samples discussed here, the CdCl₂ annealing time had been determined to be optimal at ~40 min. A series of four samples with various treatment times were produced to compare the impact of the CdCl₂ treatment on junction position: (i) as-grown, no CdCl₂ anneal; (ii) under treated, 5 min CdCl₂ anneal; (iii) optimised, 40 min anneal; and (iv) overtreated, 180 min anneal.

It should be noted that FF values for all measured cells are lower than would be typically achieved for these devices owing to the EBIC contacting requirements. Usually, the CdTe layer is scribed around the back contacts and conductive silver paint added in a surrounding ring to form a device front contact. This minimises the series resistance contribution of the transparent conducting oxide (TCO)/buffer layer stack. However, it has been found that this contacting method significantly increases the chances of shorting the device upon EBIC measurement. The device front contact was instead made directly to the TCO with no scribing, which is estimated to reduce the FF by ~10%.

1.2. Focused ion beam milling and electron beam-induced current analysis

To prepare the samples for EBIC analysis, FIB cross-section cuts were performed using a FEI Helios NanoLab 600 Dual Beam system, equipped with a focused Ga liquid metal ion source. Ion beam thinning was carried out at 52° with respect to the electron column for all samples. Initially a ‘rough cut’ was carried out after first depositing a protective platinum layer *in situ* using a gas injection system. A series of *in situ* polishing steps were then performed on the exposed cross-sections to produce a clean surface with minimal beam damage. High-resolution secondary electron imaging was carried out in the same system, with images being captured using a low kilovolts immersion lens. For EBIC analysis, samples were mounted onto a custom EBIC stage and placed into a Hitachi SU-70 microscope (Hitachi, Illinois, USA) with EBIC signals being collected through a Matelect ISM5 specimen current amplifier (Matelect Ltd, Harefield, UK).

It should be noted that because of the use of a Ga⁺ ion source for the FIB milling process, there is the potential that this may act as an n -type dopant within the CdTe layer and thus cause a shift in the junction position observed by EBIC. However, any doping occurring would be limited to the milled surface. Because of the bulk of the e-beam generation volume occurring at depths >150 nm, any surface doping is therefore not expected to impact on the EBIC signal.

1.3. Characterisation

J - V curves were recorded under AM1.5 illumination using a Oriel 81160 solar simulator. EQE measurements were made using a Bentham PVE300 system. In all cases, the EQE measurements were performed without light bias in order to ensure compatibility with the EBIC measurements.

2. DEVICE PERFORMANCE

Table I gives the average device performance values for nine contacts from each of the four samples, along with an estimation of the junction depth as determined from EBIC analysis (this shall be discussed later). Efficiency, fill factor, short-circuit current density and open-circuit voltage for each device contact measured are plotted as a

Table I. Average performance parameters for various CdCl₂ treatments.

CdCl ₂ treatment time	Efficiency (%)	Fill factor (%)	J _{sc} (mA/cm ²)	V _{oc} (V)
As-grown	1.64	28.04	9.04	0.63
5 min	4.83	41.32	17.59	0.66
40 min	9.23	56.92	20.92	0.78
180 min	4.69	53.96	15.64	0.56

function of CdCl₂ annealing time in Figure 1. It can be seen from Figure 1 that the device performance is at a peak after around 40 min annealing at 410 °C in air. Devices that have been purposefully undertreated (5 min anneal) and overtreated (180 min anneal) have annealing times chosen such that there is a near equivalent level of performance loss in comparison with the optimised device. Figure 2 shows *J-V* curves for the highest efficiency contacts from all four devices with associated EQE for these contacts given in Figure 3.

The as-grown sample shows low device performance ($\eta = 1.64\%$) with a very poor *J-V* curve shape resulting in an extremely low *FF* value (28.04%). This is not unexpected as it is widely known that the CdCl₂ activation step is key to achieving high efficiencies and that untreated cells rarely show efficiencies greater than 2%.

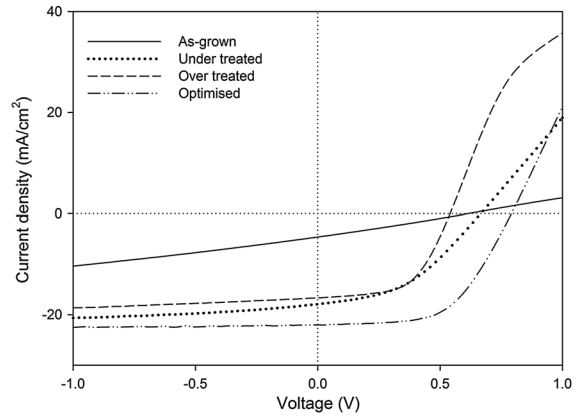


Figure 2. *J-V* curves for measured device contacts recorded prior to focused ion beam and electron beam-induced current analysis.

The EQE curve for this sample (Figure 3) shows the characteristic shape for a buried CdTe homojunction device [9], whereby collection reaches a peak at wavelengths closer to the CdTe band gap value. This accounts for the low level of device performance observed as a high proportion of high-energy photons absorbed near to CdS/CdTe interface do not contribute to current generation.

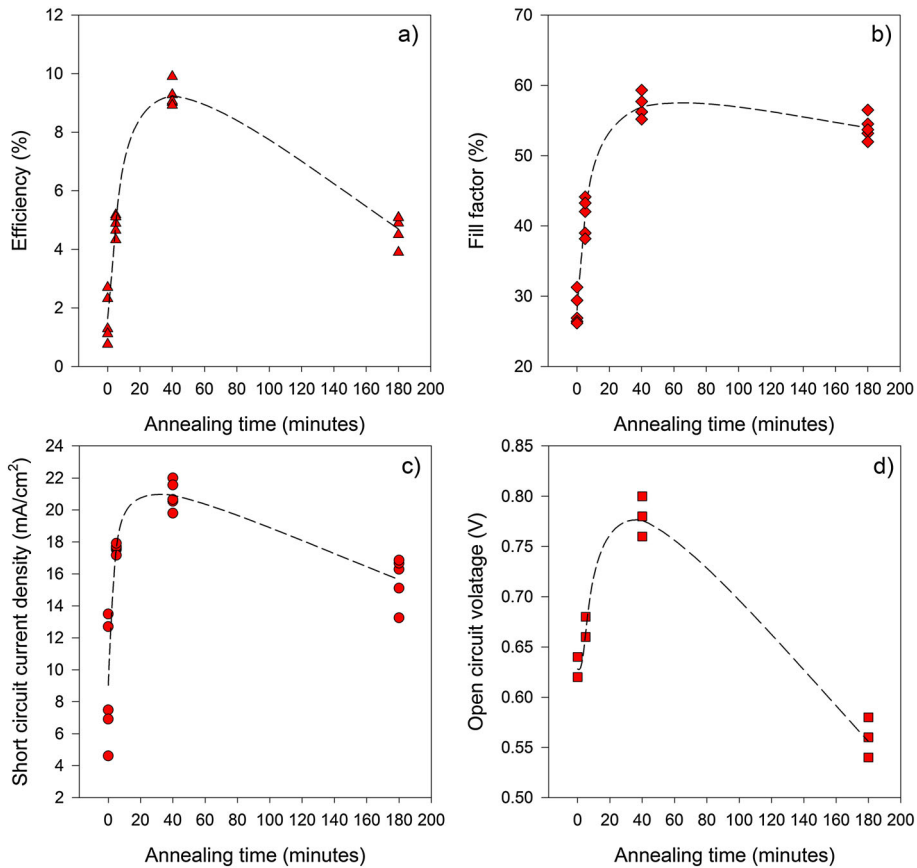


Figure 1. Device performance parameters as a function of CdCl₂ annealing time.

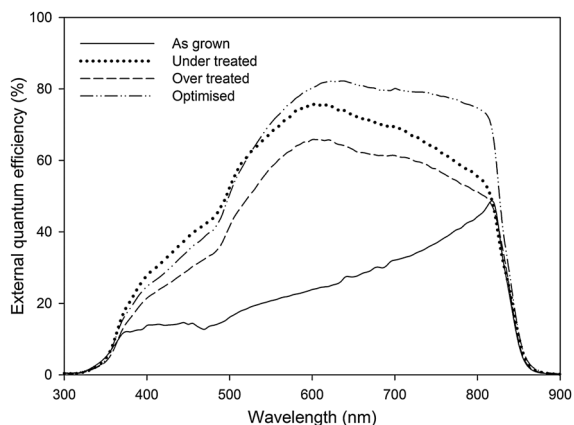


Figure 3. External quantum efficiency curves for measured device contacts shown in Figure 1 and recorded prior to focused ion beam and electron beam-induced current analysis.

For the undertreated device, efficiency has improved to an average of 4.83%, and the J - V curve has begun to display the characteristic shape expected for a functioning device. However, from the slope of the curve in forward and reverse bias, we can see that the shunt resistance is lower (reverse bias) and series resistance higher (forward bias) than for the optimised cell, hence, a lower FF and V_{oc} . The EQE curve for this device displays a typical heterojunction (i.e. p -CdTe/ n -CdS) response, with higher values at the shorter wavelength range. From EQE measurements, there is no evidence of a remaining buried junction in this device.

Device performance is highest for the sample annealed for 40 min, with an average efficiency of 9.23% (peak of 9.90%). While the sample has reasonable performance, some efficiency loss occurred because of the following: (i) high series resistance owing to the requirements of EBIC contacting and (ii) thinner than ideal CdS because of a decrease in sputtering rate from the CdS target (<70 nm deposited from an intended 100 nm). However, this device still displays around twice the efficiency of either the under or overtreated devices. Again, the EQE curve is a typical heterojunction response, showing particular improvement in the long wavelength response. This would typically be attributed to improved collection of deep penetrating photons, presumed to be due to an extended depletion region.

The overtreated device shows the majority of performance loss through a decrease in V_{oc} in comparison with the optimised device, falling to an average of 0.56 from 0.78 V. This is in fact significantly lower than for even the untreated device (0.63 V). As it is known, the device has been significantly overtreated; the typical explanation for this loss would be that the CdS layer has been consumed by intermixing, leading to the formation of CdTe/ZnO interface regions. These weaker diodes serve to reduce the device V_{oc} [11]. From the J - V curve in reverse bias, it can be seen that while some shunting has occurred, it has not completely destroyed the device

performance. This is attributed to the ZnO buffer layer minimising the effect of any shunts in the CdS layer. The J - V curve for this device also shows evidence of strong 'rollover' at high forward bias. We believe this may be due to the extended annealing time leading to the formation of oxide and chloride phases at the back surface that are deleterious to Ohmic contacting. The EQE curve for this device shows little shape change compared with the optimised device but rather an overall decrease in collection efficiency.

There have been some studies and some speculation on the point defect mechanism by which CdCl₂ treatment assists in the formation of strong p - n junctions in CdTe solar cells. It is an almost universal finding that while as-grown CdTe/CdS junctions have only weak photovoltaic response, the treatment increases it considerably. Early papers described this as 'type conversion' from n -type to p -type CdTe. However, this explanation is too simplistic, since as-grown devices do have a junction response, with EQE measurements indicating that the junction is buried in the CdTe, that is, there is a homojunction operating in which the near-CdS CdTe is n -type and that nearer the back contact is p -type. There is some evidence that dissolved CdS causes n -doping in CdTe [12], but this topic is underinvestigated. Instead, the literature has concentrated on the possible influences of chlorine in combination with native defects. Marfaing [13] points out that substituting chlorine onto the tellurium site would be expected to give donor rather than acceptor doping. Hence, it is widely speculated that p -doping in the CdTe is the result of the A-centre, a complex of a cadmium vacancy and substitutional chlorine—[V_{Cd} - Cl_{Te}]—that would act as a single acceptor centre [14]. Positron annihilation lifetime spectroscopy measurements do indeed indicate the importance of vacancy defects in CdTe films [15]. It has also been postulated that the effect of CdCl₂ treatment is also to electrically passivate the grain boundaries [12] and thus bring the material to a condition in which the impurity doping is effective. These mechanisms are in principle compatible with the promotion of p -doping from the free CdTe surface towards the CdTe/CdS junction by the advancement of a diffusion front. This would act to move the junction from the back to the front of the cell with increasing CdCl₂ treatment, and this is compatible with the results shown here.

2.1. Microstructure and electron beam-induced current analysis

After J - V and EQE analysis samples were prepared for EBIC analysis by FIB milling a cross-sectional pit in the sample. Samples were then removed and prepared for EBIC analysis by contacting the device to an external current amplifier and mounting the sample such that the beam was incident on all device layers. High-resolution secondary electron images of device cross-sections were taken after FIB cuts and polishing steps were completed.

Images that focus on the CdTe/CdS interface region for each of the four samples are shown in Figure 4.

Little change was observed in the bulk CdTe microstructure between samples. It has been reported that the CdCl₂ treatment can cause significant recrystallization and grain growth in CdTe films [16]. However, this is mainly observed for samples deposited using relatively low substrate temperatures and thus having a small as-grown grain size. For high temperature deposition, such as CSS employed for these samples, the as-grown grain size is relatively large (>1 μm), and therefore, little recrystallization is expected [17,18]. Twin boundaries were observed to be present in the CdTe layer for all samples.

By contrast, the CdS layer is seen to undergo a significant change during the annealing period. The CdS layer of the as-grown sample (Figure 4(a)) is continuous, ~65 nm thick and with a grain size of <100 nm. There are a few small void areas visible; however, these are formed at the interfaces with the CdTe or ZnO layers rather than within the CdS film. For the undertreated sample (Figure 4(b)), some recrystallization of the layer

has occurred, with a number of small voids being visible within the CdS layer. After annealing for 40 min (Figure 4(c)), recrystallization of the CdS layer has intensified, leading to the formation of larger void regions throughout the film. It is somewhat surprising that the device performance was not significantly compromised by the porous nature of the CdS layer. We attribute this to the ZnO buffer layer minimising the effect of the shunting pathways in the CdS layer. For the overtreated sample (Figure 4(d)), the visible voids have coalesced to form either vacant areas at the CdS/CdTe interface or regions that are devoid of CdS. This can be seen more clearly from the lower resolution secondary electron image in Figure 5(a). In some areas, the CdS remains the same thickness as for the as-deposited film (~65 nm) although with a larger grain size following recrystallization (~250 nm); whereas in other regions, the CdS is completely absent. Consumption of the CdS layer through intermixing with the CdTe layer is generally assumed to occur during CdCl₂ treatment, although some intermixing is anticipated to occur during CdTe deposition. It has been reported that overtreatment of devices leads to

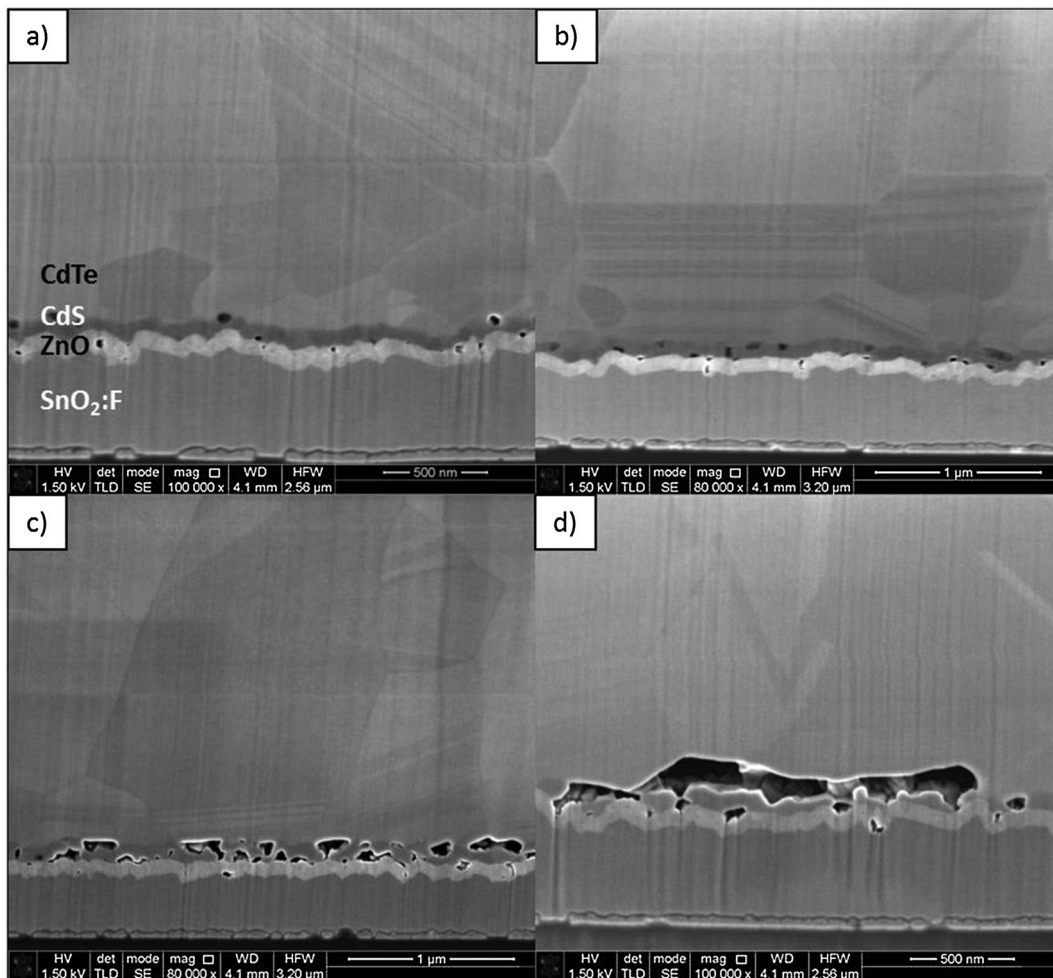


Figure 4. Secondary electron images of focused ion beam-milled cross-sections showing CdS/CdTe interface region for cells that are (a) as-grown; (b) undertreated, 5 min anneal; (c) optimised, 40 min anneal; and (d) overtreated 180 min anneal.

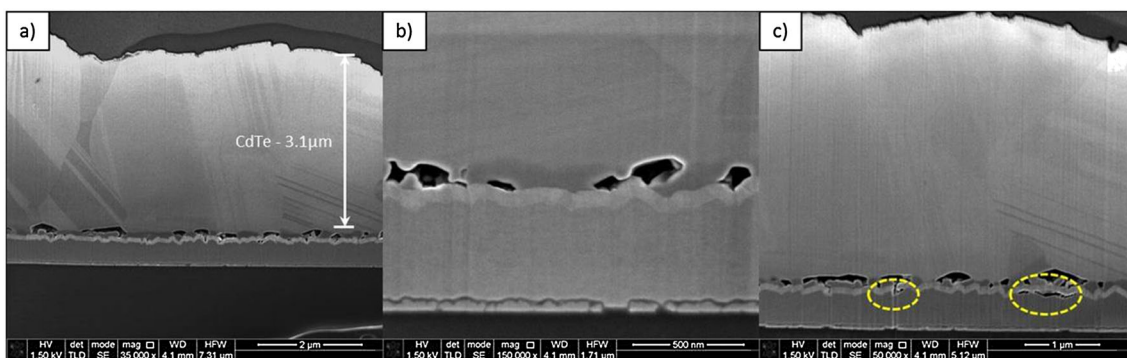


Figure 5. Secondary electron images of focused ion beam-milled cross-section of the over-treated (180 min anneal) CdTe cell showing (a) whole device structure with distinct regions of voiding, (b) close-up of CdS/CdTe interface region showing CdS voids and (c) void regions formed at the ZnO/SnO₂:F interface (ringed).

an overall thinning of the CdS layer resulting in performance loss [19]. What we observe here though is that this is not strictly the case. While the CdS does recrystallize, large regions of the film show no thickness reduction through CdCl₂ treatment. Rather, the CdS has been completely consumed in discrete regions, leaving other regions untouched as shown in Figure 5(b).

The inter-diffusion of CdTe and CdS layers is well established; the degradation and formation of voids in the CdS layer observed here is to an extent attributable to the Kirkendall effect. It predicts that for asymmetric atomic fluxes across an interface, the higher rate of out-diffusion of S into the CdTe will lead to a thinning of the CdS layer [20]. However, if bulk diffusion of the interface is inhibited, then the asymmetric diffusion will lead to the formation of Kirkendall voids. Recent work using scanning transmission electron microscopy and electron dispersion spectroscopy to examine S diffusion in CdTe solar cells [21] concluded that the amount of S out-diffusion from the CdS layer was principally determined by the ‘thermal load’ experienced by the device. It was found that the majority of S diffusion occurred during the higher temperature CdTe deposition rather than lower temperature CdCl₂ processing. It may be inferred from this that if any bulk thinning of the CdS layer occurs, it is during CdTe deposition. During the lower temperature (410 °C), the S diffusion rate is not as large, leading to the formation of Kirkendall voids that increase in size as the annealing period is extended. This eventually leads to the breakdown of a continuous CdS film and results in the observed device performance losses.

It is also worth noting that the voiding is not confined to the CdS layer with voids visible in both the region near to the CdTe/CdS interface (Figure 4(d)) and at the ZnO/SnO₂:F interface (Figure 5(c)). It is not possible to discern from this work whether there has been any intermixing between the ZnO and CdS layers and indeed if the Cl diffusion has propagated through the ZnO layer. It does appear however that there has been some delamination or recrystallization of the ZnO at the interface as a result of the CdCl₂ annealing process.

2.1.1. Electron beam-induced current determination of junction position.

In literature reports of the variations in junction position for conventional sublimation grown and CdCl₂-treated CdTe/CdS solar cells, the position was correlated with the postgrowth doping and processing of the devices [9]. It is considered that the junction position is determined by a perhaps complex interaction between in-diffusion of Cl, inter-diffusion of CdS and CdTe at the metallurgical interface and perhaps the interaction of the resulting impurities with native defects to form electrically active centres. In the previous section, we discussed the film structure changes that resulted from the CdCl₂ treatment, but the Cl diffusion front is considered to have a particularly strong effect. It is assumed, for example, that increased processing times act to bring the junction from the back to the front of the device. Here, through the EBIC cross-section analysis technique, we clearly demonstrate this to be the case.

Figure 6 shows cross-sectional EBIC signals (green) overlaid on secondary electron images (red) for each of the four devices. Unlike EBIC analysis where the sample is manually cleaved [9], the visible cross-sections are clean and smooth; thus, there is no interference from surface topography. The location of the EBIC signal represents the location of the active junction, with the peak of the EBIC signal assumed to be the peak of the inbuilt electric field. Here, EBIC contrast has been adjusted to improve image quality. Results are therefore qualitative rather than quantitative.

From EQE measurements of these devices, prior to EBIC analysis, it was anticipated that the as-grown sample, Figure 6(a), would contain a buried CdTe homojunction. This was indeed found to be the case, with the junction being located around the midpoint of the CdTe film, ~1.4 μm from the CdS/CdTe interface. This explains both the poor performance of the as-grown device and characteristic ‘buried’ shape of the EQE curve. In the undertreated sample, shown in Figure 6(b), the junction has moved towards the device front surface as a result of CdCl₂ treatment but still remains a homojunction buried

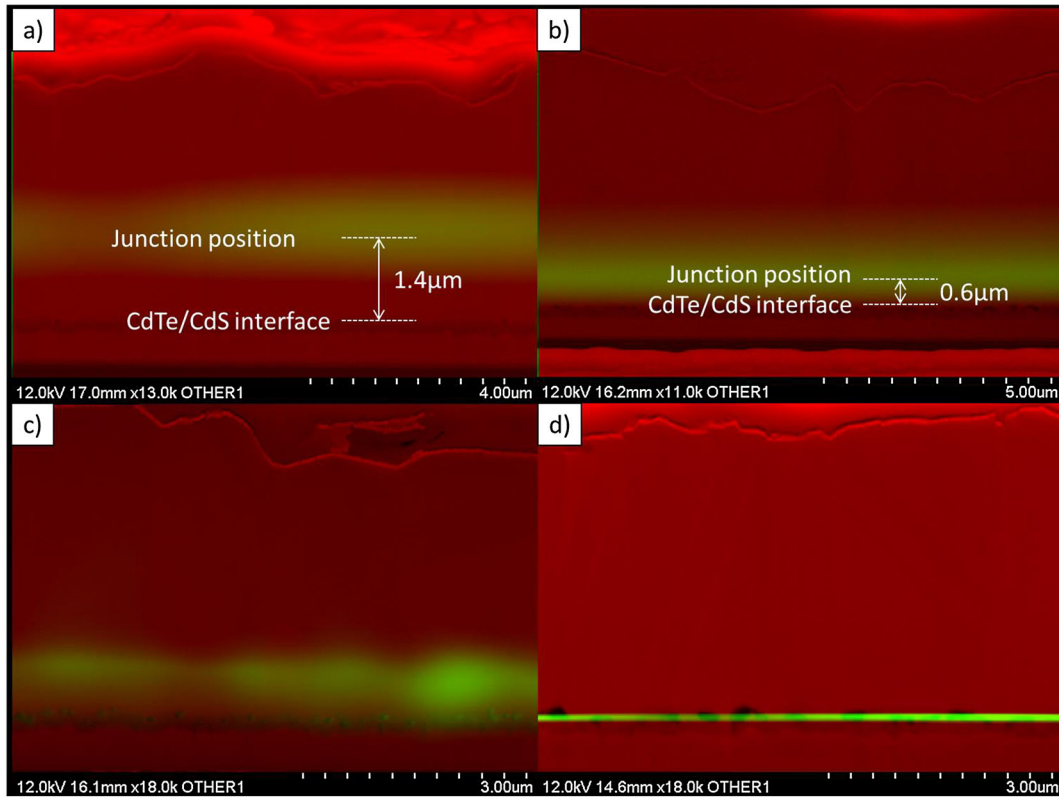


Figure 6. Combined secondary electron image (red) and electron beam-induced current signal (green) of focused ion beam-milled cross-sections showing CdS/CdTe interface region for cells that are (a) as-grown; (b) undertreated, 5 min anneal; (c) optimised, 40 min anneal; and (d) overtreated, 180 min anneal.

~0.6 μm from the metallurgical interface. Again, this burying of the junction away from the CdTe/CdS interface is likely to be the principle cause of the poor device performance. It is notable however that the EQE curve for this device (Figure 3) shows no evidence of a buried homojunction; rather, it gives a response shape normally attributed to a heterojunction. Clearly in this case, EQE spectrum shape cannot discriminate between shallowly buried homojunctions and genuine heterojunctions. We believe the reason for this is that the carrier diffusion length for CdTe is typically of the order of 1 μm. This

highlights the usefulness of cross-sectional EBIC analysis in device optimisation. For the optimised cell (Figure 6(c)), the junction is located at the CdTe/CdS interface and extends into the CdTe layer. The junction is taken to be centred at the interface as the depletion region is not anticipated to extend into the CdS layer. This is due to the high conductivity and low carrier lifetime in CdS that essentially creates a one-sided junction. This confirms that the device was indeed well optimised as the junction has been brought to the front surface and is direct evidence that the junction position in CdTe solar cells is controlled via the

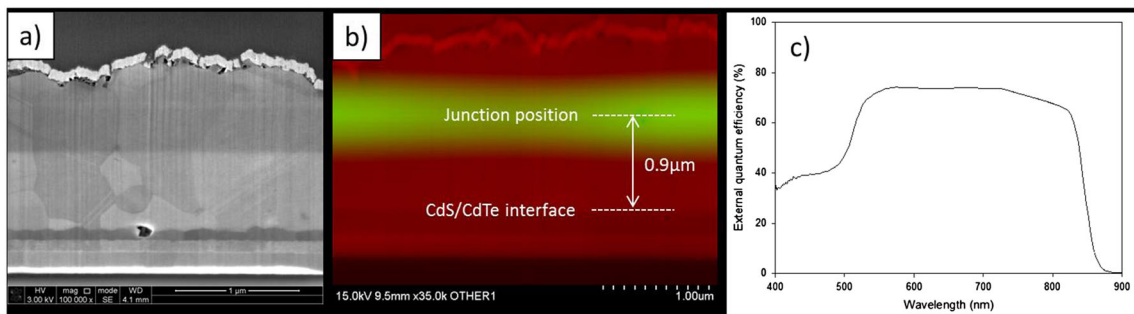


Figure 7. Analysis of sputter deposited CdTe device (a) secondary electron image showing full device structure, (b) composite image with electron beam-induced current (EBIC) signal (green) overlaid on secondary electron image (red) and (c) external quantum efficiency curve measured prior to EBIC analysis.

CdCl₂ treatment. As the CdCl₂ treatment time is extended until the device is severely overtreated, EBIC analysis shows that the junction remains fixed at the CdTe/CdS interface (Figure 6(d)) where it gives strong, narrow EBIC contrast. However, the solar cell performance is nevertheless diminished by the formation of voids at the interface induced by the overtreatment. If this voiding was not present device performance may actually be enhanced by this level of CdCl₂ treatment.

Comparison of the EBIC signal with EQE data again highlights the difficulty of interpreting junction information from EQE measurements. Typically, for a narrowed depletion region such as this one would anticipate much higher EQE performance for shorter wavelengths than for those close to the CdTe band gap, which will penetrate deeply into the layer. While there is some decrease in the long wavelength collection for the overtreated device in comparison with the optimised device, there is a far more pronounced overall decrease (~20%). Determination from this that the depletion region width had contracted would therefore be difficult.

The formation of buried homojunctions is not confined to CSS deposition, and we have observed discrepancies between EQE and EBIC analysis of other CdTe device types. Figure 7 shows a cross-sectional secondary electron image (Figure 7(a)), combined secondary electron/EBIC image (Figure 7(b)) and EQE curve for an all sputtered CdTe/CdS/ZnO/ITO device. Similar to the undertreated device, the junction is buried away from the metallurgical interface, in this case ~0.9 μm. Again, however, no evidence of this buried homojunction is evident from the EQE measurement (Figure 7(c)). For EBIC analysis, we are able to spatially image the areas of strongest collection and thus determine the junction position. While collection may appear to be zero from other regions of the CdTe layer, a small EBIC current is in fact generated from regions away from the junction. A proportion of carriers generated outside the space charge region but within a diffusion length are still collected but appear as a weak EBIC signal. As EQE is not able to distinguish between carriers generated from inside and outside the space charge region, thus shallowly buried homojunctions appear as heterojunctions. Any junction shallowly buried, that is, <1 μm, will therefore not be detectable by EQE measurement alone. Future work will focus on the development of quantitative EBIC analysis to allow direct measurement of depletion width and carrier diffusion length.

3. CONCLUSION

The FIB cross-sectioning technique effectively overcomes the limitation of the use of cleaved cross-sections for the direct study of junction phenomena in thin-film solar cells. Clean and smooth cross-sections were prepared that not only revealed surfaces displaying excellent crystallographic contrast under secondary electron imaging in the scanning electron microscope but also were ideal for

interrogation using EBIC: Interference from surface topography resulting from mechanical cleaving was absent. High-resolution imaging EBIC analysis was performed for devices with a range of CdCl₂ treatment times. Secondary electron images showed the CdS layer degraded via the Kirkendall effect, leading to the formation of void regions and TCO/CdTe weak diode regions. The electrical junction of the device was shown to be brought towards the CdS/CdTe interface from the back surface with increased CdCl₂ treatment times. For extended annealing, the junction remained at the CdTe front surface, but the quality of the junction was reduced because of the breakdown of the CdS layer. Discrepancies between junction information discernible by EBIC and by EQE measurement were highlighted, with it being demonstrated that shallowly buried homojunctions could not be identified as buried by EQE. A junction must be buried >0.9 μm from the CdS/CdTe interface before EQE measurement will yield a typical buried junction response curve.

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REFERENCES

1. Edwards PR, Galloway SA, Durose K. EBIC and luminescence mapping of CdTe/CdS solar cells. *Thin Solid Films* 2000; **372**: 284–291.
2. Galloway SA, Edwards PR, Durose K. Characterisation of thin film CdS/CdTe solar cells using electron and optical beam induced current. *Solar Energy Materials and Solar Cells* 1999; **57**: 61–74.
3. Durose K, Sadler JRE, Yates A, Szczerbakow A, IEEE. R-EBIC study of the electrical activity of grain boundaries in CdTe and Cd(S,Te). *Proceedings of the 28th IEEE Photovoltaic Specialists Conference*, IEEE, New York, 2000; 487–490.
4. Panin G, Yakimov E. REBIC-SEM characterization of compound semiconductors. *Semiconductor Science and Technology* 1992; **7**: A150–A153.
5. Durose K, Asher SE, Jaegermann W, Levi D, McCandless BE, Metzger W, Moutinho H, Paulson PD, Perkins CL, Sites JR, Teeter G, Terheggen M. Physical characterization of thin-film solar cells. *Progress in Photovoltaics* 2004; **12**: 177–217.
6. Major JD, Bowen L, Durose K. Focussed ion beam and field emission gun-scanning electron microscopy for the investigation of voiding and interface phenomena in thin-film solar cells. *Progress in Photovoltaics* 2012; **20**: 892–898.

7. Perez G, Courtade F, Benteo B, Gauffier JL, Kwang JL. Junction delineation and EBIC on FIB cross section. *Microelectronics Reliability* 1998; **38**: 907–912.
8. Inns D, Puzzer T, Aberle AG. Localisation of the $p-n$ junction in poly-silicon thin-film diodes on glass by high-resolution cross-sectional electron-beam induced current imaging. *Thin Solid Films* 2007; **515**: 3806–3809.
9. Major JD, Durose K. Study of buried junction and uniformity effects in CdTe/CdS solar cells using a combined OBIC and EQE apparatus. *Thin Solid Films* 2009; **517**: 2419–2422.
10. Major JD, Proskuryakov YY, Durose K. Impact of CdTe surface composition on doping and device performance in close space sublimation deposited CdTe solar cells. *Progress in Photovoltaics* 2013; **21**(4): 436–443.
11. Koishiyev GT, Sites JR. Effect of weak diodes on the performance of CdTe thin-film modules. *Proceedings of the 34th IEEE Photovoltaic Specialists Conference*, IEEE, Philadelphia, 2009; 79–82.
12. Edwards PR, Halliday DP, Durose K, Richter H, Bonnet D. The influence of CdCl₂ treatment and interdiffusion on grain boundary passivation in CdTe/CdS solar cells. *Proceedings of the 14th European Photovoltaic Solar Energy Conference*, WIP, Barcelona, 1997; 2083–2087.
13. Marfaing Y. Impurity doping and compensation mechanisms in CdTe. *Thin Solid Films* 2001; **387**: 123–128.
14. Proskuryakov YY, Durose K, Major JD, Al Turkestani MK, Barrioz V, Irvine SJC, Jones EW. Doping levels, trap density of states and the performance of co-doped CdTe(As,Cl) photovoltaic devices. *Solar Energy Materials and Solar Cells* 2009; **93**: 1572–1581.
15. Keeble DJ, Major JD, Ravelli L, Egger W, Durose K. Vacancy defects in CdTe thin films. *Physical Review B* 2011; **84**(17): 1–6.
16. Moutinho HR, Al-Jassim MM, Abulfotuh FA, Levi DH, Dippo PC, Dhere RG, Kazmerski LL. Studies of recrystallization of CdTe thin films after CdCl₂ treatment. *Proceedings of the 26th IEEE Photovoltaic Specialists Conference*, IEEE, Anaheim, 1997; 431–434.
17. Moutinho HR, Dhere RG, Al-Jassim MM, Mayo B, Levi DH, Kazmerski LL. Induced recrystallization of CdTe thin films deposited by close-spaced sublimation. *NCPV Photovoltaics Program Review* 1999; **462**: 517–523.
18. Cousins MA, Durose K. Grain structure of CdTe in CSS-deposited CdTe/CdS solar cells. *Thin Solid Films* 2000; **361**: 253–257.
19. Albin DS, Yan Y, Al-Jassim MM. The effect of oxygen on interface microstructure evolution in the CdS/CdTe solar cells. *Progress in Photovoltaics* 2002; **10**: 309–322.
20. Albin DS. Accelerated stress testing and diagnostic analysis of degradation in CdTe solar cells. *Proceedings of SPIE 7048, Reliability of Photovoltaic Cells, Modules, Components, and Systems*, San Diego, 2008; 1–10.
21. Taylor AA, Major JD, Kartopu G, Lamb D, Duenow J, Dhere R, Moutinho H, Irvine SJC, Durose K, Mendis BG. A comparative study of sulfur diffusion in CdS/CdTe solar cell devices. *To be published* 2014.