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Instability of phosphorous doped SiO₂ in 4H-SiC MOS capacitors at high temperatures

M. I. Idris,^{1,2} M. H. Weng,^{1,3} H.-K. Chan,¹ A. E. Murphy,³ D. T. Clark,³ R. A. R. Young,³ E. P. Ramsay,³ N. G. Wright,¹ and A. B. Horsfall¹

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In this paper, the effect of inclusion of phosphorous (at a concentration below 1%) on the high temperature characteristics (up to 300 °C) of the SiO₂/SiC interface is investigated. Capacitance–voltage measurements taken for a range of frequencies have been utilized to extract parameters including flatband voltage, threshold voltage, effective oxide charge, and interface state density. The variation of these parameters with temperature has been investigated for bias sweeps in opposing directions and a comparison made between phosphorous doped and as-grown oxides. At room temperature, the effective oxide charge for SiO₂ may be reduced by the phosphorous termination of dangling bonds at the interface. However, at high temperatures, the effective charge in the phosphorous doped oxide remains unstable and effects such as flatband voltage shift and threshold voltage shift dominate the characteristics. The instability in these characteristics was found to result from the trapped charges in the oxide ($\pm 10^{12} \text{ cm}^{-3}$) or near interface traps at the interface of the gate oxide and the semiconductor ($10^{12}–10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$). Hence, the performance enhancements observed for phosphorous doped oxides are not realised in devices operated at elevated temperatures. *Published by AIP Publishing.* [<http://dx.doi.org/10.1063/1.4969050>]

I. INTRODUCTION

In the history of high temperature electronics, the silicon technology has been used with a limited operating capability of temperatures below 150 °C.¹ The demand for electronic components that are capable of sustaining high temperature operation for markets such as automotive, aerospace, energy generation, and military has been growing rapidly. Due to the excellent material properties of silicon carbide (SiC), such as the extremely small intrinsic carrier density, the feasibility to grow a thermal oxide, and wide band gap, it has become a leading candidate for high temperature and high power electronics. A lot of effort has been made to improve the quality, performance, and reliability of silicon carbide Metal Oxide Semiconductor (MOS) structures, especially focusing on the quality of the gate oxide layer, which plays a vital role in the performance of SiC MOSFETs. However, in the recent years, a number of issues have been reported with SiC MOSFETs, especially in terms of performance and long term reliability.^{2,3} These issues have been gradually alleviated as a result of recent developments. One of the significant remaining issues with silicon carbide MOSFETs is the low channel mobility caused by Coulomb scattering and trapping that decreases the number of free carriers.^{4,5} Many researchers have been working on increasing the channel mobility of SiC MOSFET by optimizing passivation techniques using nitrogen-,^{6,7} sodium-,⁸ and phosphorous-^{9,10} rich environments. It has been shown^{6,11} that the inversion channel mobility within SiC dramatically improves when the (11 $\bar{2}$ 0) face is utilised, although this leads to a decrease in the threshold voltage, which for some applications may be

undesirable. Threshold instability is one of the important factors which disrupts the performance and reliability of SiC MOSFET. Recently, the threshold voltage instability for MOSFET annealed in POCl₃ has been investigated by using both positive and negative biases at temperatures up to 200 °C.¹² The data were described by a model based on the capture and emission properties of traps at the SiO₂/SiC interface or in the bulk oxide. It has been confirmed that the main origin of the threshold voltage instability is the oxide traps in phosphorous doped oxides.

It has been reported that incorporating P atoms into the SiO₂/SiC interface reduces the density of interface states (D_{it}) near the conduction band and increases the field effect mobility to 89 cm²/V s.¹⁰ Linked to this experimental result, a strong reduction in the interface state density was observed for samples implanted with P prior to oxidation.¹⁰ It is believed that the incorporated P atoms reduce the strain and increase the carrier density at the SiO₂/SiC interface.^{10,13} G. Liu also reported that passivation of the SiO₂/SiC interface using phosphorous results in lower D_{it} and higher field effect mobility than nitrogen passivation for MOSFETs fabricated on both the Si face and the (11 $\bar{2}$ 0) a-face of 4H-SiC.⁶ However, the mechanism responsible for D_{it} reduction by P incorporation is still not fully understood.

Atoms in group 5 of the periodic table consist of nitrogen (N), phosphorous (P), arsenic (As), antimony (Sb), and bismuth (Bi), and each has 5 electrons in the outermost shell. This electron configuration provides 4 half-filled outer orbitals that can interact with the lone pairs of other elements to form 4 covalent bonds. According to Density Functional

Theory (DFT) calculations, strong silicon-nitrogen, silicon-phosphorous, and silicon-arsenic bonds are created at the SiC/SiO₂ interface, resulting in a decrease in the density of near interface traps.¹⁴ Observations also imply that N and P atoms can not only passivate interfacial defects but may also diffuse into the SiC substrate, resulting in an increased channel mobility and reduction in threshold voltage, through the creation of shallow donors.^{6,15,16} The occurrence of counter doping of the SiC surface has been proposed, where a very thin n type layer is formed at the SiC/SiO₂ interface due to the incorporation of N or P atoms.⁶

The conductivity of the SiC surface after being exposed to post-oxidation annealing (POA) in N₂O and POCl₃ has been examined qualitatively by using scanning spreading resistance microscopy (SSRM) measurements.¹⁷ It was found that the incorporation of P-related shallow donors after POA in POCl₃ is greater than the N-shallow donors incorporation during N₂O treatment, which subsequently explains the significantly enhanced channel conductivity of the MOSFETs. The quantitative analysis of the doping at the SiO₂/SiC interface to explain the function doping effect from N and P atoms was performed using electrostatic simulations.¹⁸ The counter doping effect was assumed to arise from a thin layer of n type material in the p-well region. By varying the thickness and the doping concentration, it was identified that the counter doping reduces the electric field at the interface, alleviating the surface roughness effect, resulting in higher mobility, but resulted in instability in the threshold voltage (V_{TH}), the flatband voltage (V_{FB}), and the effective charge (N_{EFF}).

Because of the suitability of SiC for the realisation of high temperature electronic devices, the reliability and the high temperature performance of phosphorous incorporated SiO₂ in 4H-SiC are of increasing interest. However to date, very little attention has been paid to the performance of phosphorous doped oxides at high temperatures. In this paper, we have investigated the flatband, the threshold voltage, and the oxide charge shift (hysteresis) for phosphorous incorporated MOS (by characterizing bidirectional C-V curves at different frequencies between 10 kHz and 1 MHz) at temperatures up to 300 °C. All the extracted parameters were compared to an undoped thermal oxide gate dielectric sample to determine the effect of phosphorous incorporation on the oxide characteristics.

II. EXPERIMENT AND EVALUATION METHOD

In this work, two Si face, 4° off axis, and 4H-SiC wafers (4 μm epilayer thickness with $N_D = 1.44 \times 10^{17} \text{ cm}^{-3}$) with different gate dielectric fabrication processes were compared. Sample 1 was prepared with a thermal oxide gate electric MOS that has been through a conventional post

oxide annealing process.¹⁹ Sample 2 is a phosphorous doped gate oxide structure, which was annealed using a planar source of phosphorous pentoxide (P₂O₅) after thermal oxidation. This process resulted in a phosphorous concentration of below 1% in the gate dielectric. Both wafer processes are designed to be compatible with a commercial CMOS process.²⁰ Process details and the equivalent oxide thickness of the SiO₂ for both wafers are summarized in Table I.

A Keithley 4200 SCS was used to measure capacitance-voltage (C-V) characteristics at different frequencies and elevated temperatures. The measurement was swept from accumulation (+10 V) to depletion (−10 V) (reverse sweep) and vice versa (forward sweep) under positive and negative bias conditions. In this experiment, the flatband voltage (V_{FB}) was determined by calculating the flatband capacitance, C_{FB} using

$$C_{FB} = \frac{C_{ox} \cdot \epsilon_s A / L_D}{C_{ox} + \epsilon_s A / L_D}, \quad (1)$$

where ϵ_s is the permittivity of the silicon carbide (taken as equal to $9.7\epsilon_0$ ²¹), C_{ox} is the experimental oxide capacitance, and L_D is the Debye length, which can be expressed as

$$L_D = \sqrt{\frac{kT\epsilon_s}{q^2 N_D}}, \quad (2)$$

where k is the Boltzmann constant, T is the temperature, and N_D is the doping concentration. The flatband voltage is extracted directly from the capacitance-voltage characteristic.

A significant effort has been focussed on trying to improve the quality of SiC/SiO₂ by reducing the total effective oxide charge and the interface state density, because these two parameters determine the carrier channel mobility and the gate leakage current. During MOSFET operation, the density and position of charged centres in the gate oxide change, resulting in the observed stability and reliability problems. Effective oxide charge, Q_{EFF} , is used to describe the charge trapped in the bulk of the dielectric and is computed from the sum of the fixed oxide charge (Q_F), mobile ionic charge (Q_M), and oxide-trapped charge (Q_{OT}). Q_{EFF} does not vary with gate voltage, unlike interface trapped charge (Q_{IT}), and it can be assumed that the charges exist at the bulk of SiO₂

$$Q_{EFF} = Q_F + Q_M + Q_{OT}. \quad (3)$$

In order to extract Q_{EFF} , the high-frequency room-temperature capacitance–voltage characterization was performed at 1 MHz. The effective oxide charge was obtained using

TABLE I. Summary of fabrication process for both samples.

Wafer	Metal	Gate dielectric	Total effective oxide thickness (nm)	Size (μm ²)
1	Aluminium	Thermal oxide + anneal + nitride cap	33	1.12×10^5
2	Aluminium	Thermal oxide + anneal (PHOS source) + nitride cap	35.7	1.12×10^5

$$Q_{EFF} = \frac{C_{ox}(W_{MS} - V_{FB})}{A}, \quad (4)$$

where W_{MS} is the metal-semiconductor work function (the work function used for Al is 4.1 eV and the electron affinity of SiC is 3.1 eV (Ref. 22)), C_{ox} is the experimental oxide capacitance per unit area, and V_{FB} is the flatband voltage. The effective oxide charge density, N_{EFF} , can be calculated as

$$N_{EFF} = \frac{Q_{EFF}}{q}. \quad (5)$$

In SiC MOS capacitors, the inversion capacitance cannot be measured due to the low intrinsic carrier concentration and hence low generation of minority carriers.^{23,24} The turn-on region of a MOSFET correlates to the inversion region in C-V measurement data. The threshold voltage V_{TH} can be determined from the flatband voltage by

$$V_{TH} = V_{FB} \pm \left[\frac{A}{C_{ox}} \sqrt{4\epsilon_s q |N_D \Phi_B| + 2|\Phi_B|} \right], \quad (6)$$

where A is the gate area, N_D is the doping concentration, and V_{FB} is the flatband potential. Φ_B is the bulk potential calculated from

$$\Phi_B = \frac{kT}{q} \ln \left(\frac{N_D}{n_i} \right), \quad (7)$$

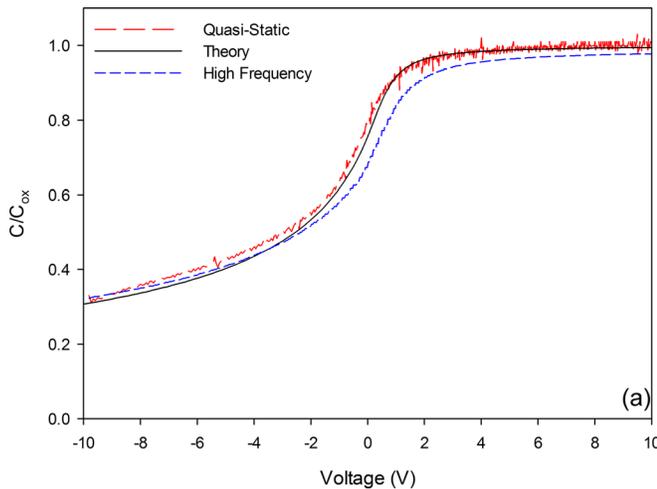
where n_i is the intrinsic carrier concentration.

However, the calculated threshold voltage V_{TH} may be slightly different from the threshold voltage V_{TH} for a MOSFET owing to the variety in methods used to extract the threshold voltage.

III. RESULTS AND DISCUSSION

A. Capacitance voltage characterization (room temperature)

The data in Figure 1 show the room temperature C-V characteristic of MOS capacitors fabricated on both wafers.



In each figure, the quasi static and high frequency (1 MHz) C-V data are plotted with a theoretical curve, which was calculated using^{25,26}

$$C_{D,theory}(\psi_s) = \frac{AqN_D \left| \exp\left(\frac{q\psi_s}{kT}\right) - 1 \right|}{\sqrt{\frac{2kTN_D}{\epsilon_{SiC}} \left\{ \exp\left(\frac{q\psi_s}{kT}\right) - \left(\frac{q\psi_s}{kT}\right) - 1 \right\}}}. \quad (8)$$

The effective oxide charge concentration, N_{EFF} , was calculated to be $-3.26 \times 10^{11} \text{ cm}^{-2}$ for the undoped oxide and $-3.03 \times 10^{11} \text{ cm}^{-2}$ for the phosphorous doped oxide. At room temperature, both samples have negative values of the order of $\sim 3 \times 10^{11} \text{ cm}^{-2}$. Phosphorous may reduce the effective oxide charge by passivating dangling bonds at the interface; however, the difference is minor in this case. Since the effective oxide charge is a sum of fixed, mobile, and trapped charge,^{22,27} further analysis is required to identify the relative contributions from the constituent components. Herein, the temperature dependence of the effective oxide charge, flatband, and threshold voltage were studied to determine the effect of phosphorous incorporation on the characteristics of the SiO₂/SiC interface.

B. Capacitance voltage characterization (elevated temperatures)

In order to investigate the polarization of the gate dielectric and temperature dependence of phosphorous incorporated oxide parameters, 1 MHz capacitance voltage characteristics were measured at temperatures up to 300 °C.

As can be observed from the data in Figure 2, the C-V data show a shift in the flatband voltage for both samples that increases monotonically with temperature. The data indicate that the shift in V_{FB} is larger for the phosphorous doped dielectric, indicating a shift in effective oxide charge and the existence of electron trapping, either at the SiO₂/SiC interface or in the bulk oxide. The effect of phosphorous incorporation on the characteristics was investigated by extracting the shift in V_{FB} , V_{TH} , and N_{EFF} arising from positive gate bias bidirectional

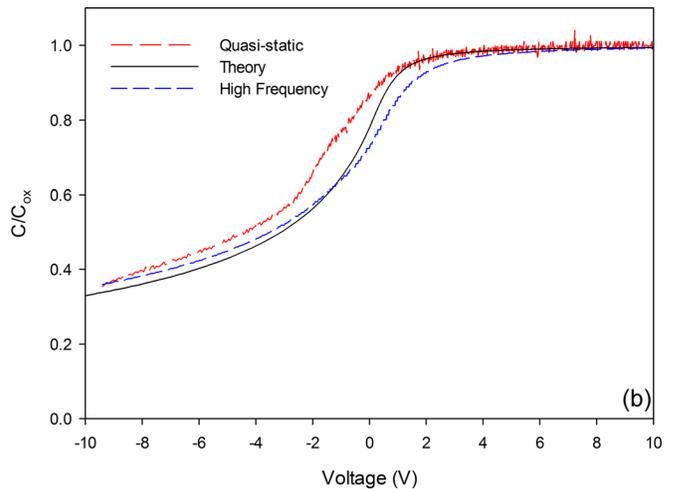


FIG. 1. Room temperature C-V characteristics of 4H-SiC MOS capacitors: (a) undoped gate dielectric; (b) phosphorous doped gate dielectric. Experimental quasi static and high frequency (1 MHz) data are plotted with a theoretical curve.

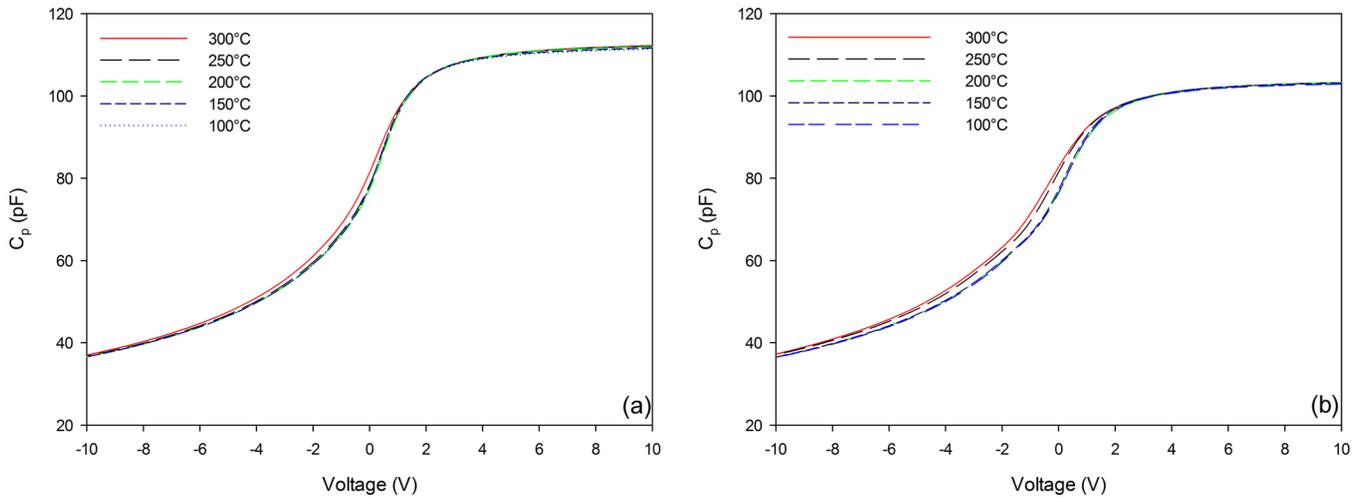


FIG. 2. 1 MHz capacitance–voltage characteristics of undoped (Figure 2(a)) and phosphorous doped devices (Figure 2(b)) measured at temperatures between 100 and 300 °C.

depletion to accumulation (forward sweep) and accumulation to depletion (reverse sweep) voltage sweeps and negative gate bias bidirectional accumulation to depletion (reverse sweep) and depletion to accumulation (forward sweep) voltage sweeps. ΔV_{FB} , ΔV_{TH} , and ΔN_{EFF} are defined as the difference in values from those obtained at room temperature; the forward sweep data of V_{FB} , V_{TH} , and N_{EFF} at room temperature are always compared to the forward sweep of V_{FB} , V_{TH} , and N_{EFF} at elevated temperature and vice versa. All the measurements were performed on fresh samples, meaning that the capacitors had not undergone any previous electrical stressing and measurements.

C. Flatband voltage, V_{FB} , instability

The data presented in Figure 3 show the change in the extracted flatband voltage, highlighting the differences arising from the direction of the voltage sweep. The data in Figure 3 show that the difference in the flatband voltage for

the phosphorous doped dielectric is more than a factor of four greater than that observed in the undoped dielectric (for both gate bias), which has only a small shift at all temperatures between room temperature and 300 °C. The shift is particularly significant for the reverse sweep during the C-V measurements. We also observed positive V_{FB} shifts in the reverse sweep data (red triangles), in close agreement with previously reported PSG oxides on Si where the observed shift in the C-V characteristics is significant; this is possibly due to the charge displacement or the buildup of polarization in the PSG doped oxide layer.²⁸ However, from the results of the flatband voltage shift from negative and positive bias measurements (accumulation to depletion and backward and depletion to accumulation and backward), where the flatband shift of sample 2 is to the positive direction regardless of the applied bias stress (bias independent), we conclude that the instability of phosphorous-doped SiO₂ is due to charge trapping or mobile charge rather than the polarization effect where the bias dependent shift is expected.

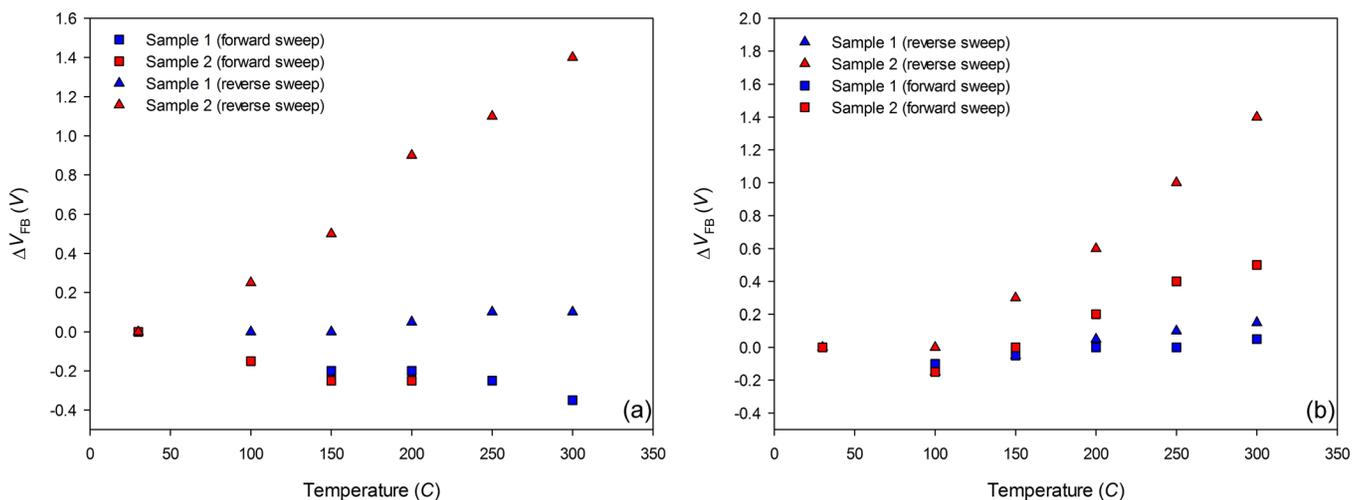


FIG. 3. Change in flatband voltage ΔV_{FB} extracted from 1 MHz C-V characteristics as a function of temperature for undoped and phosphorous doped dielectrics under negative (Figure 3(a)) and positive (Figure 3(a)) gate bias conditions. ΔV_{FB} is defined as the difference of V_{FB} at room temperature and those V_{FB} obtained at elevated temperature.

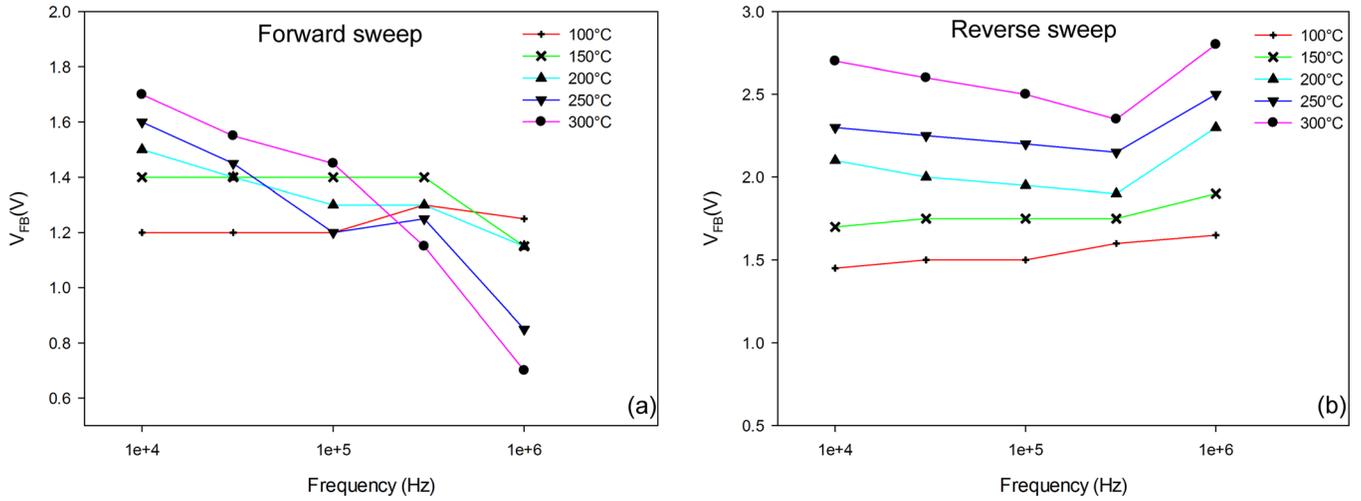


FIG. 4. Frequency dependence of V_{FB} for the phosphorous doped oxide measured for both directions. (a) Forward sweep and (b) reverse sweep.

When V_g was swept from $V_g = -10$ V to $V_g = 10$ V (forward sweep), minority carriers are attracted to the interface from the bulk of the SiC. Since the concentration of minority carriers is negligible in SiC MOS capacitors, the effect on the characteristics of the trap and de-trap processes at the SiC/SiO₂ interface is not apparent. This implies that the number of trapped charges at the interface is small, suggesting that the value of ΔV_{FB} should remain constant as the temperature changes. However, under negative bias condition, the data show that the value of ΔV_{FB} becomes negative with increasing temperature and while both samples show similar behaviour, the changes in ΔV_{FB} for the phosphorous doped dielectric are more noticeable. Meanwhile, under positive bias stress, different trends were observed. The ΔV_{FB} remains constant as the temperature increases for undoped samples, but the data show that the value of ΔV_{FB} for phosphorous doped samples becomes noticeably positive with increasing temperature.

When the gate voltage was swept from $V_g = 10$ V to $V_g = -10$ V (reverse sweep), majority carriers are accumulated at the interface. Since the majority carrier concentration is significantly higher than the minority carrier concentration

in SiC MOS capacitors, the effect of trap and de-trapping due to states at the interface is more obvious for both bias conditions, especially for the phosphorous doped SiO₂ dielectric. The larger changes in ΔV_{FB} for this sweep direction (reverse sweep) can be explained by the trapping of these additional carriers at the interface.

The data in Figure 4 show the bidirectional characteristic of V_{FB} values for the phosphorous incorporated sample measured at different frequencies. The data for the forward sweep measurement, at temperatures below 200°C, show a minor variation in V_{FB} with frequency, but as the temperature is increased above 200°C, the V_{FB} values are significantly reduced with increasing frequency. For reverse sweep measurements, the data show that the shift in V_{FB} is unaffected by frequency, but are shifted to larger V_{FB} as the temperature increased, similar to the data shown in Figure 3.

D. Threshold voltage, V_{TH} instability

The threshold voltage, V_{TH} , is the bias at which the surface potential, Φ_S , equals twice the bulk potential Φ_B and can be calculated from the C-V characteristics using

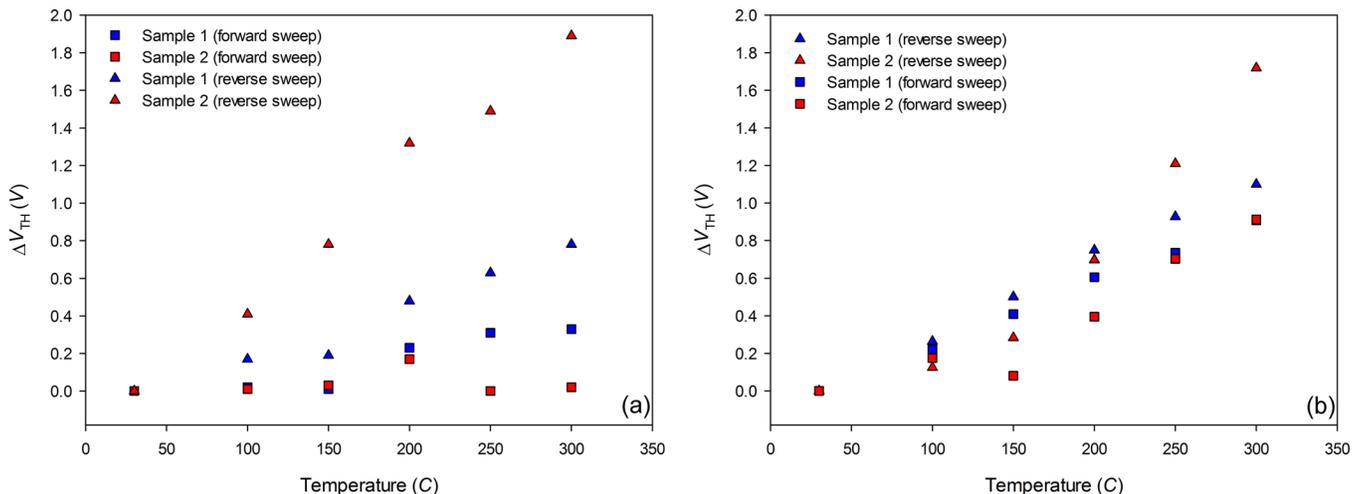


FIG. 5. Threshold voltage (V_{TH}) extracted from 1 MHz C-V characteristics as a function of temperature for the undoped (sample 1) and phosphorous doped (sample 2) dielectrics under negative (Figure 5(a)) and positive (Figure 5(a)) gate bias conditions.

Equation (6). The calculated values are shown by the data in Figure 5. Similar to the data shown in Figure 3, the effect of trapping and de-trapping processes is less significant during the forward sweep, resulting in a smaller shift in V_{TH} as the temperature increases. Furthermore, the threshold voltage shift in the device with the phosphorous doped dielectric is greater (up to 2 V shift at 300 °C) than for the undoped dielectric as the temperature increases during reverse sweep for both bias conditions.

The variation in V_{TH} with frequency and temperature was also investigated. The data in Figure 6 show the bidirectional characteristic of V_{TH} for the phosphorous incorporated sample as a function of frequency at elevated temperatures. The same trend is observed for V_{TH} as for V_{FB} , where the instability is more pronounced at 250 °C and 300 °C. The results show that V_{TH} is stable with frequency when the gate bias is swept from $V_g = 10$ V to $V_g = -10$ V. However, the observed frequency dispersion increases with temperature, similar to the trend observed for the V_{FB} data. At higher temperatures, V_{TH} values decrease because the emission of trapped charges increases as the bandgap of SiC reduces, so a lower bias is required to form an inversion region.¹² From the data, it is clear that the concentration of trapped charge is greater in the phosphorous doped dielectric than in the undoped samples. The enhanced shift in both flatband and threshold voltages is also linked to the presence of a defect arising from the incorporation of positive phosphorous in the oxide and at the SiO₂/SiC interface.^{29–32} P atoms are not mobile if they are in the form of PSG, formed during the annealing process. PSG is a polar material and the effect of polarization is more significant when it is electrically biased at high temperatures.^{9,33} Different types of voltage stress measurements are needed to investigate the characteristics of NITs.¹²

E. Total effective oxide charge density, N_{EFF} in phosphorous incorporated oxide

N_{EFF} depends on the quality of both the gate oxide and the interface. Previous studies have examined a range of approaches to reduce N_{EFF} because it is one of the dominant

factors in the suppression of channel mobility and reduces the quality of oxide based passivation layers.²² In this study, bidirectional 1 MHz C-V characteristics at elevated temperatures were used to compare the temperature dependence of N_{EFF} in the phosphorous incorporated and undoped oxides. N_{EFF} was determined using Equation (5), with a work function difference between the aluminium contact and the SiC of 1.0 eV.²⁵ Figure 7 depicts the dependence of N_{EFF} at elevated temperatures extracted from sweeps forward and reverse for both dielectrics under negative (Figure 7(a)) and positive (Figure 7(a)) gate bias conditions. For the undoped oxide, the variation in the effective oxide charge density shows a minor variation with temperature, with values between -2 and $-4 \times 10^{11} \text{ cm}^{-2}$ in both directions regardless of the applied bias stress. In contrast, under a negative bias condition, the data for the forward sweep on the phosphorous doped dielectric show N_{EFF} monotonically decreasing from $-2.4 \times 10^{11} \text{ cm}^{-2}$ to $-6.4 \times 10^{10} \text{ cm}^{-2}$ with increasing temperature up to 250 °C, before changing polarity to $4.07 \times 10^9 \text{ cm}^{-2}$ at 300 °C, but the N_{EFF} increases slowly with increasing temperatures under positive bias condition. In the reverse sweep, significantly different characteristics were observed (both bias conditions). The N_{EFF} increases slowly from room temperature to 100 °C, followed by an abrupt increase above 100 °C. This behaviour may be attributed to the concentration of mobile charge in the phosphorous incorporated oxide, which is distinct from the chemically bonded P atoms that lead to the observed increase in N_{EFF} .

This instability in N_{EFF} has two potential origins: charge trapped in the bulk of the dielectric, which is described using an effective charge density (N_{EFF}), and charge trapped in interface states, described using the interface state density (D_{it}). The data in Figure 7 show that the effective charge density in the phosphorous doped dielectric shifts significantly in comparison to the undoped dielectric. From these data, it appears that traps in the oxide generated during the phosphorous doping process result in the electrical instability through the capture and emission of electrons and holes at the SiO₂/SiC interface or in the oxide.¹²

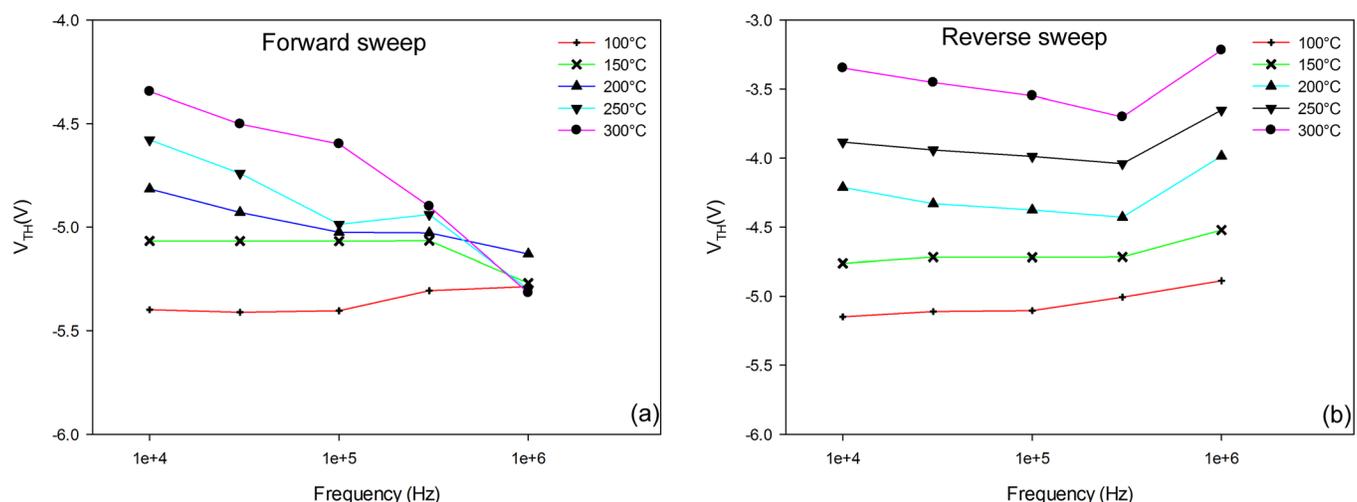


FIG. 6. Frequency dependence of V_{TH} for sample 2 measured for both directions. Forward sweep (a) and reverse sweep (b).

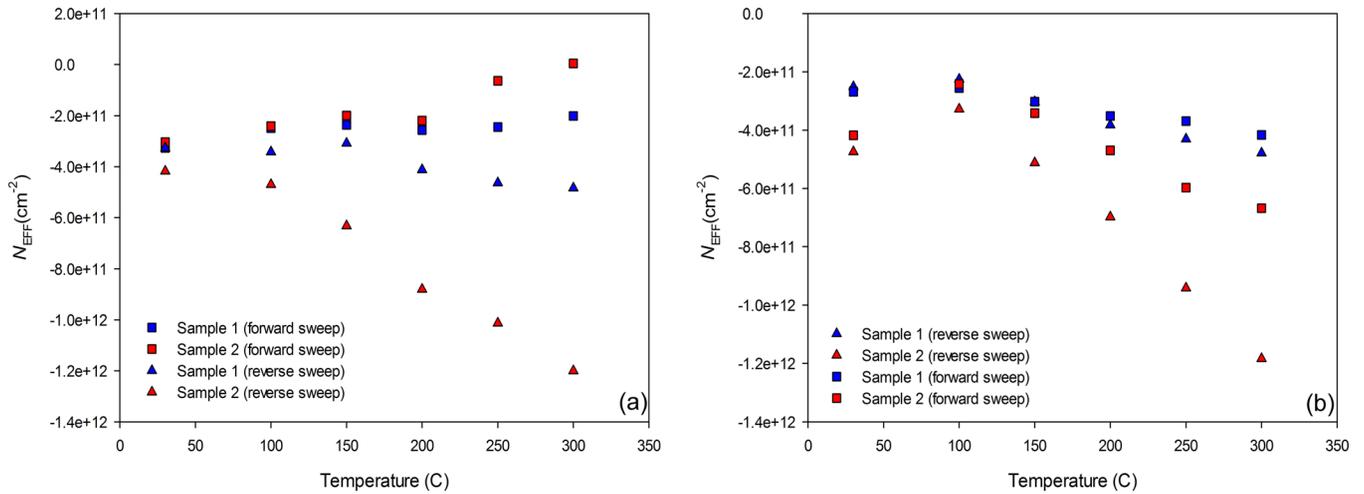


FIG. 7. Variation in the effective oxide charge density in samples 1 and 2 under negative (a) and positive (b) gate bias conditions.

F. Bias Temperature Stress (BTS)

In order to investigate the presence of mobile charge in these two samples, positive and negative bias temperature stress (BTS) has been performed according to the method stated in Ref. 26. Initially, the C-V measurements at room temperature are taken as reference (before stress) for both samples. Then, the samples are heated to 200 °C and a gate bias to produce an oxide field of around 10 MV/cm is applied for 5 min for the charge to drift to oxide interface. (In our case, the thickness of oxides is around 36 nm, so 3.6 V was applied.) The samples are then cooled to room temperature under bias, and the C-V measurements are performed. For the negative bias temperature stress (NBTS), the procedure is then repeated with the opposite bias polarity. It is important to keep the oxide field around 1 MV/cm causes mobile charge to drift and to prevent any charge injection from happening. The flatband voltage shift can be used to determine the mobile charge. Fresh samples were used for each test.

The data in Figure 8 show the C-V characteristics before and after positive bias temperature stress for both undoped and

dielectric (Figure 8(a)) and phosphorous doped dielectric (Figure 8(b)). The undoped samples and phosphorus doped samples indicates the V_{FB} shift (different before and after PBTS) of 0.35 V (mobile charge density of $2.16 \times 10^{11} \text{ cm}^{-2}$) and 1.15 V (mobile charge density of $6.55 \times 10^{11} \text{ cm}^{-2}$), respectively, while almost no hysteresis for forward and reverse sweeps for both samples before and after PBTS. These results show that the amount of mobile charge in phosphorus doped samples is significantly higher than the counterpart probably due to the mobile ion gettering capability of phosphorous.^{34,35} Positive BTS results obtained here also can be explained by the electrons trapping at the oxide and interface when the positive stress has been applied at 200 °C before C-V measurements have been performed. As mentioned before, a lot of electrons are trapped at the interface when the positive bias was applied to the gate for 5 minutes and causes the flatband voltage to shift to the positive direction.^{36,37}

The results for negative bias temperature stress (NBTS) are shown in Figure 9 for both samples. The C-V characteristics of the undoped sample are very stable; there is no

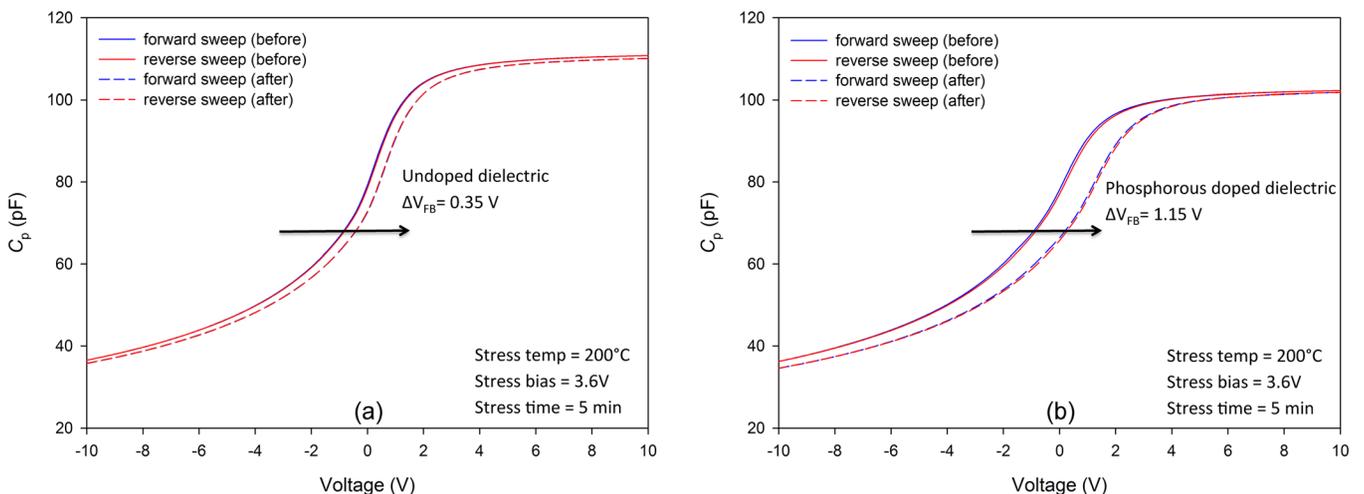


FIG. 8. C-V curves illustrating the effect of mobile charge motion for undoped (a) and phosphorous doped dielectric (b) measured before (solid lines) and after (dash lines) PBTS.

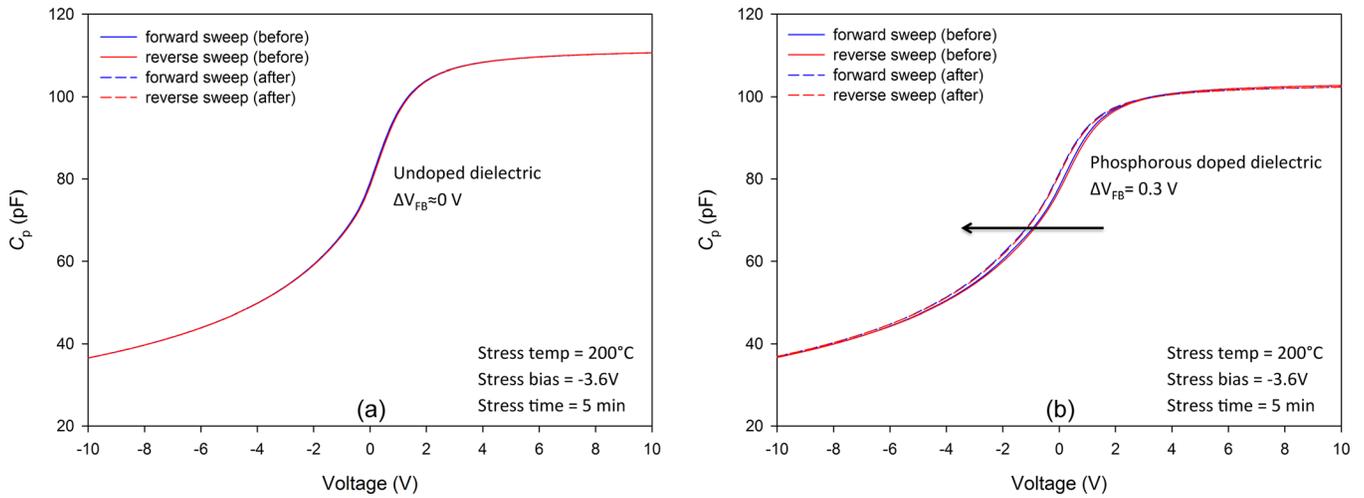


FIG. 9. C-V curves illustrating the effect of mobile charge motion for undoped (Figure 9(a)) and phosphorous doped dielectric (Figure 9(b)) measured before (solid lines) and after (dash lines) NBTS.

hysteresis for forward and reverse sweeps before and after stress, indicating the non-existence of mobile charges in the dielectric. In contrast, there is a small flatband voltage shift 0.3 V (mobile charge density of $1.72 \times 10^{11} \text{ cm}^{-2}$) in the negative direction, which is observed for the phosphorous doped samples. When the negative bias is applied to the gate for 5 minutes at 200°C , the minority carrier (holes) attracted to the interface and gets trapped. However, since holes are minority carriers, the flatband voltage shift after the stress is less compared to the shift caused by majority carriers. The trends obtained from BTS have shown that the mobile charge and trap in the oxide or interface have caused the instability to the phosphorous doped samples.^{38,39} These features for electron traps are consistent with the results obtained in Secs. III C and III D and agree with the observations published elsewhere.^{36,37}

G. Interface trap density, D_{it}

Until now, the origin of interface traps remains unclear. According to previous reports in the literature interface traps can be associated with (1) carbon or silicon clusters at the SiC/SiO₂ interface, (2) intrinsic defects formed in the bulk of gate dielectric, and (3) interfacial defects at the SiC/SiO₂ interface. Reports also correlate the presence of a carbon defect in the bulk SiC as being responsible for the low quality of gate oxide and increased value of D_{it} .⁴⁰ By incorporating phosphorous, the carbon vacancy in the gate oxide can be replaced by P or P=O, resulting in a stable silica matrix.⁴¹ Interface state density is known to play an important role in the inversion layer mobility and hence the characteristics of the MOSFET. The density of interface traps at SiC/SiO₂ is higher than Si/SiO₂ and this is often considered to be the primary reason for low mobility.⁴² Many researchers reported that mobility can be increased by reducing D_{it} ,^{7,9,43} however, the relation between D_{it} and mobility is still not fully understood.⁴² The data in Figure 10 show the D_{it} extracted for both samples using the $C-\psi_s$ technique from room temperature quasi-static C-V measurements.⁴⁴ It is worth noting that the value of D_{it} is high in comparison to previously

published data because the $C-\psi_s$ technique can accurately determine the contribution of fast states, which are not accurately reflected in the more commonly used Terman or High-Low methods.^{9,17} The voltage was swept from depletion to accumulation at a rate of 0.1 V/s. Significant reduction can be observed in the value of D_{it} at $E_c-E = 0.2 \text{ eV}$ (close to the conduction band) for the phosphorous doped oxide in comparison to the undoped dielectric (sample 1). However, the D_{it} values for sample 2 decrease more slowly as the energy from the conduction band edge increases in comparison to the undoped oxide. Near the conduction band, in the range where E_c-E is between 0.2 and 0.28 eV, the D_{it} of the phosphorous incorporated dielectric is lower; however, once $E_c-E > 0.3 \text{ eV}$, the D_{it} of the undoped sample is lower and decreases more rapidly with energy. This is due to the effect of D_{it} reduction in phosphorous incorporated oxide, which is not significant for Si face 4H SiC epilayers, and the level of phosphorous incorporated into the oxide is insufficient to form PSG in these samples.⁴⁵ However, the results are comparable with previously published reports, which show a

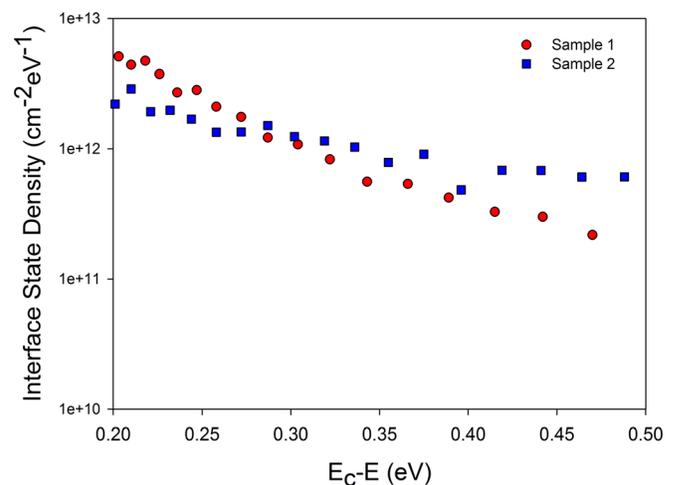


FIG. 10. Comparison of interface state density (D_{it}) as a function of energy, extracted using the $C-\psi_s$ technique.

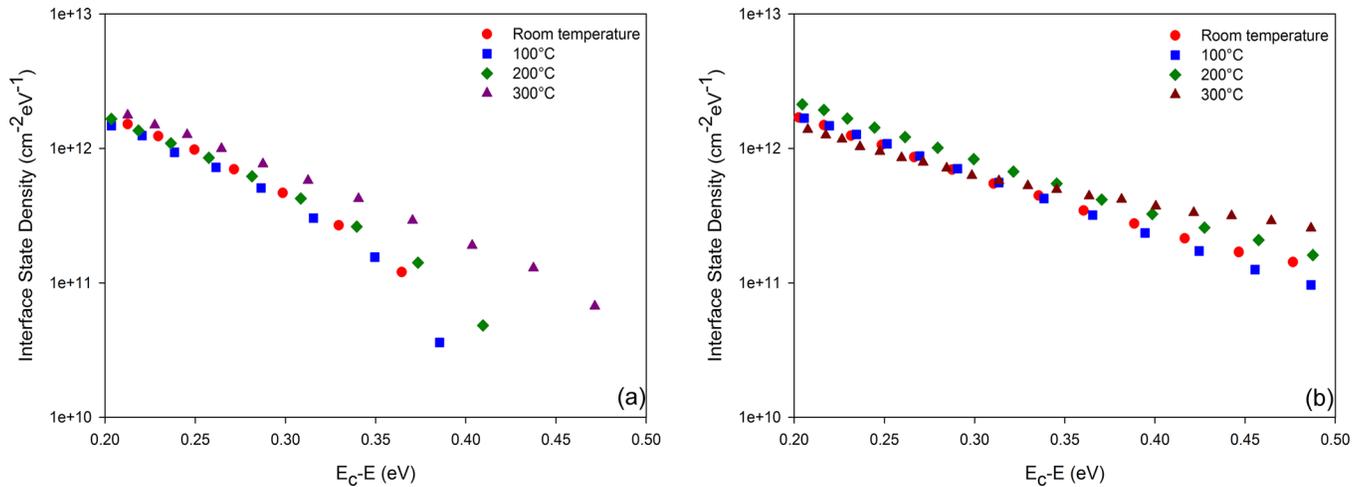


FIG. 11. Interface state density (D_{it}) as a function of energy at varying temperatures extracted using the Terman method for sample 1 (a) and sample 2 (b).

reduction of D_{it} to $2 \times 10^{12} \text{ cm}^{-2}$ at 0.2 eV below the conduction band.^{6,9}

Interface state density (D_{it}) as a function of the energy level within the bandgap was also extracted across the measured temperature range for both samples using the Terman method.⁴⁶ As can be seen from the data in Figure 11, the change in D_{it} close to the band edge as the temperature increases is not consistent for both samples; however, a trend at energies defined by $E_c - E > 0.3 \text{ eV}$ can be observed. The extracted D_{it} for both dielectrics reduces with increasing temperature across the measured energy range. This suggests that the interface state density, D_{it} , has the temperature dependence and therefore is electrically active at elevated temperatures.⁴⁷ At high temperatures, the oscillation of the atoms around their equilibrium position results in the replacement of the sharply defined energy level for the capture or emission of carriers with a probability density at the specific energy. This results in an increase in the occupancy of traps with carriers that have a sufficiently high energy to enable a capture/emission process.⁴⁸ These results can also be explained by correlating the existence of slow and fast interface states that have different time constants that only begin to interact with semiconductor carriers at high temperatures,⁴⁹ which is in agreement with the observation of the SiO_2/SiC interface annealed in nitrogen rich environments.⁵⁰

IV. CONCLUSIONS

We have shown that the incorporation of phosphorous at the SiO_2/SiC interface results in a reduction in the interface state density near the conduction band, and an increase in the instability of V_{FB} , V_{TH} , and N_{EFF} at high temperatures. To date, there are limited reports concerning the stability of phosphorous doped SiO_2 in 4H-SiC at elevated temperatures. In this paper, the effect of phosphorous incorporation in the gate dielectric was extracted from bidirectional C-V measurements at temperatures up to 300 °C. Although the effective oxide charge (N_{EFF}) in phosphorous doped SiO_2 has been slightly reduced, the instability at high temperatures is a concern. The results from other parameters (V_{FB} and V_{TH}) also showed instability depending on the gate bias,

frequency, and temperature. In the forward sweep, both samples provide stable V_{FB} and V_{TH} values even at high temperatures. Meanwhile, in the reverse sweep, due to charge trapping, V_{FB} and V_{TH} shifts increase with temperature. The D_{it} of both samples was compared, and it was found that phosphorous-doped oxides (sample 2) have slightly lower D_{it} than undoped oxides near the conduction band.

In this case, the effect of mobile ions and charge traps at high temperatures should not be neglected. This could cause electron and hole trapping to occur in the gate dielectric and at the SiC interface. The implementation of phosphorous incorporated oxide in SiC is encouraging to improve the channel mobility. However, the stability and reliability aspects are always essential to be taken into consideration of device performance. Therefore, it is important to improve the stability of phosphorous incorporated devices not only at room temperature but also at high temperatures so that the advantageous effect of phosphorous incorporation is not reduced. We have shown that although the inclusion of phosphorous with a concentration below 1% in the silicon dioxide gate dielectric of MOSFET structures can be highly beneficial for room temperature performance, the instability of the resulting devices when operated at high temperatures means that this technique is not suitable for high temperature circuits.

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