An accurate method to determine the mobility of TMDCs with incomplete gate screening

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Abstract

Van der Waals layered transition metal dichalcogenides, usually exhibit high contact resistance due to the induced Schottky barriers, which occur at non-ideal metal-semiconductor contacts. These barriers usually contribute to an underestimation in the determination of mobility, when extracted by standard, two terminals methods. Furthermore, in devices based on atomically-thin materials, channels with thickness of up to a few layers cannot completely screen the applied gate bias, resulting in an incomplete potential drop over the channel; the resulting decreased field-effect causes further underestimation of the mobility. We demonstrate a method based on Kelvin probe force microscopy, which allows us to extract the accurate semiconductor mobility and eliminates the effects of contact quality and/or screening ability. Our results reveal up to a sevenfold increase in mobility in a monolayer device.

Keywords: *field effect mobility*, *KPFM*, *TMDs*, MoS_2, contact resistance

Introduction

Two dimensional materials have attracted much attention as promising candidates for the next generation of nanoelectronics. Molybdenite (MoS_2) along with other transition metal dichalcogenides (TMDCs), are of special interest to the scientific community due to their electronic properties, such as indirect to direct band gap transition, and mechanical flexibility. MoS_2 has a direct band gap of $1.8 - 2.2\ eV$[1,2], which makes it particularly suitible for optoelectronics applications in the visible range[3,4], and photovoltaics[5–8]. Its extraordinarily large surface to volume ratio makes it ideal for chemical sensing[9–14], whereas its band structure marks it as a perfect candidate for valleytronics and spintronics[15–17]. Multilayer MoS_2 has lower, indirect band-gap and can conduct larger currents, due to the higher density of states at the conduction band minimum[18,19], which makes it useful for high power electronics. Despite being at the focus of the research efforts[20–29], measuring the carrier mobility of MoS_2, along with other transport properties, is not trivial and often leads to inaccurate results due to two main reasons. First, contact resistance that stems from the Schottky barriers at the interface between most metals and low-dimensional materials, result in large potential drops over the contacts which effectively reduce the drift

velocity in the channel. Second, limited charge screening ability in some cases, as will be demonstrated in the present work, means that the actual carrier density in the channel is overestimated. Both factors contribute to underestimation of the mobility, an effect that becomes significant in the case of ultrathin devices, thinner than the Debye screening length. Assuming a charge density of $N_D = 10^{12}\ cm^{-2}$ (equivalent to $10^{18}\ cm^{-3}$)[30] and relative permittivity of[31] $\varepsilon_r = 3.9$, Debye length is calculated to be $L_D = 2.36\ nm$, which is around 3 layers of MoS_2.

Most of the reports on contact resistance in MoS_2 FETs focus on techniques of reducing it rather than on eliminating their effect on transport properties and their measurements. Reducing the contact resistance can be achieved in several ways, including using specific electrode materials which are compatible with MoS_2[20–23], advanced growth techniques for chemical vapour deposition (CVD) grown MoS_2[24], phase-engineered low-resistance contacts[25], and the use of atomically thick h-BN as a tunnelling layer[26]. In addition to material modifications, other approaches that are based on measurement methodologies can be utilised to overcome the effect of contact resistance on the estimation of intrinsic mobility. Four probe measurements were conducted on monolayer[27] and multilayer[28] MoS_2, but are limited by the fabrication processes as achieving the four probe configuration on small-scale devices is very challenging. Moreover, the resistance between the contacts and the semiconductor is not limited to the current probes, and in many cases, the voltage probes are affected as well, rendering a precise determination of conductivity possible only when the channel is in its 'open' state.

Van Der Pauw measurements can be utilised to estimate the average mobility in any arbitrary sample shape[32], but suffer from similar disadvantage to four-probe measurements with respect to the contact resistance of the voltage probes. Hall effect measurements are another way of eliminating the contact resistance influence, as was shown on a 15nm MoS_2 FET[29]. The main disadvantages of this method, are the need of special contacts configuration beyond the usual FET contacts, and the ambiguous relation between Hall and field effect mobility which is largely affected by the Hall scattering factor that cannot be precisely determined[33]. Another approach is to calculate the intrinsic mobility through its relation to the momentum scattering time measured by optical-pump terahertz-probe spectroscopy[34]. This method can produce results of up to an order of magnitude higher than previously reported values for MoS_2, but requires advanced optical measurements.

The Y-function method, which was originally developed for Si devices[35], was recently modified to include gate depended Schottky-barrier and extract the low-field carrier mobility in MoS_2 transistors[36]. This method is based on introducing a series resistance component into the drain current equation, which accounts for both contact resistances. This method, like the other reviewed methods, generates an equivalent resistance for both contacts, without the ability to separate them- disadvantage when dealing with asymmetric contact resistance in thin-layer devices[37,38], and does not account for the incomplete screening effect discussed below.

To fully account for the incomplete screening of gate potential and decouple the inherent transport measurements from the quality of contact interface, we introduce a method for the accurate determination of the field-effect mobility, which isolates the voltage-drop on the channel from that on the contacts, and allows us to examine the quality of each contact separately, and more importantly to extract the accurate semiconductors transport properties, even when poor contacts are present. We demonstrate the first

evidence of incomplete potential screening in channels, ranging from monolayers up to few-layers, where long channels in the order of several microns, show limited charge injection or uneven distribution of the injected charges through the conduction path. This causes partial screening of the applied back-gate voltage, leaving a significant level of excess potential that is directly measureable with a Kelvin probe force microscope (KPFM), and causes a large underestimation of the mobility values.

Results and Discussion

The four studied devices differ in their thickness, ranging from a monolayer to bulk crystal. Thicknesses were measured using AFM, in combination with Raman spectroscopy for thin layer flakes[39]. The peak separation is $18.06, 21.4\ and\ 23.1\ cm^{-1}$ corresponding to 1, 2 and 3 layers respectively, the thicker device was found to be 25nm thick, corresponding to 35 layers. The channel lengths ranged between $1.75 - 7.5\ \mu m$. Those measurements are provided in Fig. S1 in the supplementary data. Electrical characteristics were measured in order to determine the gate, and source-drain voltages ranges, in which the devices operate within the linear regime, for field-effect mobility calculations. These results are also available in the supplementary data, Fig. S2.

KPFM was used to measure the surface potential cross section between the source and drain electrodes, while applying a fixed source-drain bias (V_{DS}) and varying back-gate voltages. Fig. 1a shows the surface potential profiles along the channel of the MoS_2 FET, for MoS_2 bilayer device. For each V_{BG} the $V_{DS} = 0\ V$ profile was subtracted from the $V_{DS} = 7\ V$ profile, in order to eliminate the initial work-function difference between the semiconductor and the metal contact. Large potential drops are observed on both contacts and are attributed to the formation of Schottky barriers which are common in thin films MoS_2 FETs[40,41], among many other TMDCs[42–46]. The large voltage drops on the contacts reduces the overall conductance

of the device and, if not corrected for, causes an underestimation of the mobility, since the fraction of the source-drain voltage that drops over the channel is significantly smaller than one.

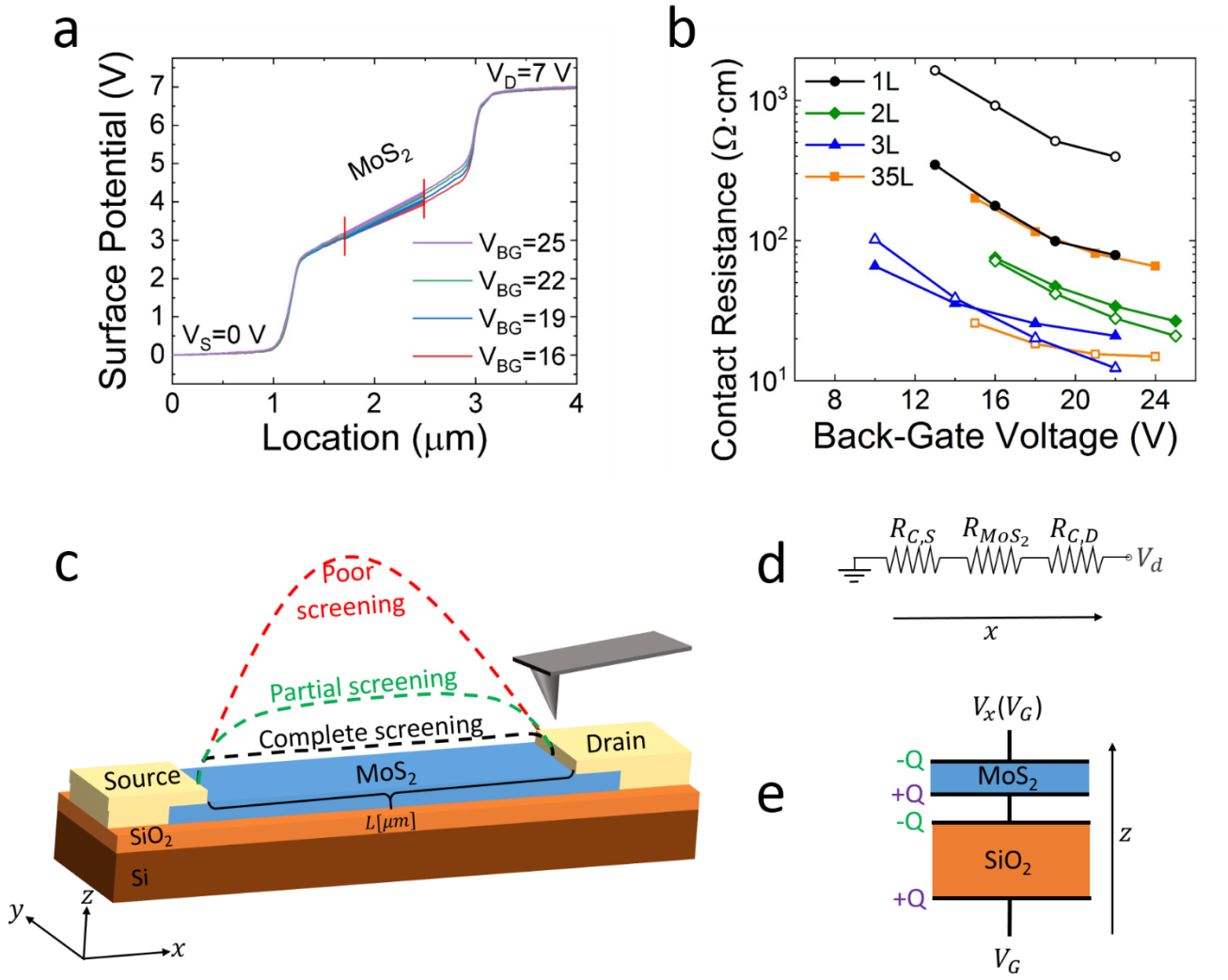

FIG. 1. (a) Surface potential measurements at different back-gate voltages with V_{BG} ranging from 16 to 25 V and a constant $V_{DS} = 7\,V$ of a bilayer MoS_2 device. The bold lines are linear fits to the potential drop over the MoS_2 film, away from the metal induced band bending which is due to Schottky barriers. (b) Calculated contact resistance for each contact individually, as a function of the back gate voltage, for the four devices. Filled markers represent the source contact, while open markers represent the drain. (c) Measurement configuration of a typical device, dashed line represents the measured surface potential profile, differ by the device screening ability. (d) An equivalent circuit diagram, with contacts resistance included as two resistors $R_{C,S}, R_{C,D}$.(e) An equivalent circuit model of the device gate-channel stack as two capacitors in series, with applied back-gate on the bottom and floating surface potential on top, defined as V_X.

The two-terminal mobility calculation relies on the device dimensions and the external applied V_{DS}, and is given by:

$$\mu = \frac{1}{C_{OX}} \cdot \frac{d\sigma}{dV_{BG}} = \frac{L}{W \cdot C_{OX} \cdot V_{DS}} \cdot \frac{dI_{DS}}{dV_{BG}} \qquad \textit{Equation.1.}$$

Where σ is the conductivity, I_{DS} is the channel current, V_G is the back-gate voltage, L and W are the device length and width, respectively, and C_{OX} is the SiO_2 capacitance per unit area, which is $3.84 \cdot 10^{-4}\ F/m^2$ assuming $90\ nm$ oxide thickness and a relative permittivity of 3.9. This equation assumes that within the linear regime of the I_{DS}-V_{BG} curve, the injection of carriers from the drain to the channel is negligible in limiting the current, and therefore, the majority of the potential drop occurs on the channel.

However, in devices where the Schottky barrier is still significant, and changes with gate bias, we must only account for the potential-drop over the MoS_2 flake away from the bent bands to achieve an accurate determination of the MoS_2 film mobility, independent of the contacts quality. The linear segment of the potential drop seen in Fig 1(a), is fitted with a linear equation. The lateral electric field along drain-to-source axis is extracted using $E(x) = d(Surface\ Potential)/dx$, which is equal to the slope of the linear fit. The conductivity can then be extracted from Ohm's law, $\sigma = J/E$, where J is the current density, and plugged into Eq. 1 to find the mobility.

The presented method for determining the mobility is profoundly different from standard two terminal estimations since the entire channel length, L, is replaced with the part of the channel that is unaffected by the band bending at the Schottky barriers, ΔL, and the applied V_{DS} is substituted with a fraction, ΔV, that corresponds to that segment of the channel. This manipulation isolates the measurement of the material quality from the effects induced by the contacts. By way of demonstration, the standard two terminal estimation leads to a mobility of $\mu = 4.1\ \frac{cm^2}{V \cdot s}$ on the bilayer device, while our method yields a corrected value of $\mu = 10.8\ \frac{cm^2}{V \cdot s}$, with the difference between the two values attributed to the contribution from the contact resistance.

Using the voltage drop on the metal-semiconductors contact (V_C) and the measured current (I_{DS}), the contact resistance (R_C) can be extracted using: $R_C = V_C/I$. The contact resistance for each of the contacts (source – S, and drain – D) was calculated as a function of the back gate voltage, and is shown for each for the four devices in Fig. 1(b).

The figure shows that the contact resistance reduces with an increase in the gate bias for all devices. This could be due to either a gate controlled Schottky diode, where the gate bias changes the work function of the semiconductor and thus, the Schottky-barrier height, or due to a reduction in the Schottky barrier width, which increases the tunnelling efficiency across the junction. For the thinner devices, up to a trilayer, there is a monotonous trend of reduced contact resistance with device thickness, while for bulk there is a moderate increase in the contact resistance. This dependency was explained by S.-L. Li *et al.*[47], who distinguished between two transport regimes – a 2D regime with a resistance deep (or trough) at 5 layers, and a 3D regime for thicker materials. The resistance in the 2D regime is mainly governed by the expansion of the band-gap[2,48] which changes the Schottky barrier height, through a change in the work function. Whereas in the 3D regime, the band gap is constant, and inactive layers with a very low concentration of free charge carriers, which are present at the bottom of the device closer to the gate[19,49,50], become the dominant effect that hinders the gating in bottom gated devices[51].

Eq. 1 is derived from the basic FET drain current in the linear regime $I_D = \mu \cdot Q \cdot \frac{W}{L} V_{DS}$, where $Q = C_{tot} \cdot (V_{BG} - V_{th})$ is the gate induced charge within the channel. This equation relies on an implicit assumption that the channel fully screens the potential that reaches the semiconductor. However, in devices that are thinner than the Debye screening length, it is reasonable to assume that some of the gate potential will not be screened by the channel, and will fringe at the top modifying the surface potential. By modelling the device as two capacitors in series as shown schematically in Fig.1(e), we can describe the change in surface potential using

$$Q = C_{tot} \cdot (V_{BG} - V_{th}) = \frac{V_{BG} - V_{th} - V_X}{C_{OX}^{-1} + C_{MoS_2}^{-1}} \approx C_{OX}(V_{BG} - V_{th} - V_X). \quad \textit{Equation.2.}$$

Where V_X is the modified surface potential. The approximation on the right-hand side is justified by the two orders of magnitude difference in thickness between the gate oxide and the channel thickness which renders $C_{MoS_2}^{-1}$ negligible compare to C_{OX}^{-1}. When V_X is in the order of the applied gate bias, Eq. 2 must be used as a correction to Eq.1, which means that the differential $d\sigma/dV_{BG}$ must be corrected accordingly to account for decrease in induced charge carriers in the channel, which is a source for further underestimation of the mobility.

When a positive gate voltage is applied to the channel, electrons are injected through the contacts to screen the applied potential, shifting the Fermi level towards the conduction band. Since exfoliated MoS_2 is naturally n-doped, due to abundant sulphur vacancies[52–57], its Fermi level is initially close to the conduction band, and can only shift up to a few tenth of electron-volts before being pinned by the high density of states in the conduction band[18,19]. This means that when the measured surface potential is larger than a few tenth of electron-volts, with a positive gate bias compared to the surface potential at $V_{BG} = 0\ V$, the measured excess surface potential is the unscreened gate voltage.

To determine whether V_X is negligible in the calculation of mobility, the surface potential was measured on four devices. A short channel $1.75\ \mu m$ bilayer device, and long channel ($L > 5.65\ \mu m$) monolayer, trilayer and bulk devices, with the back gate biased between 10 and 25 V, and both the source and drain electrodes grounded.

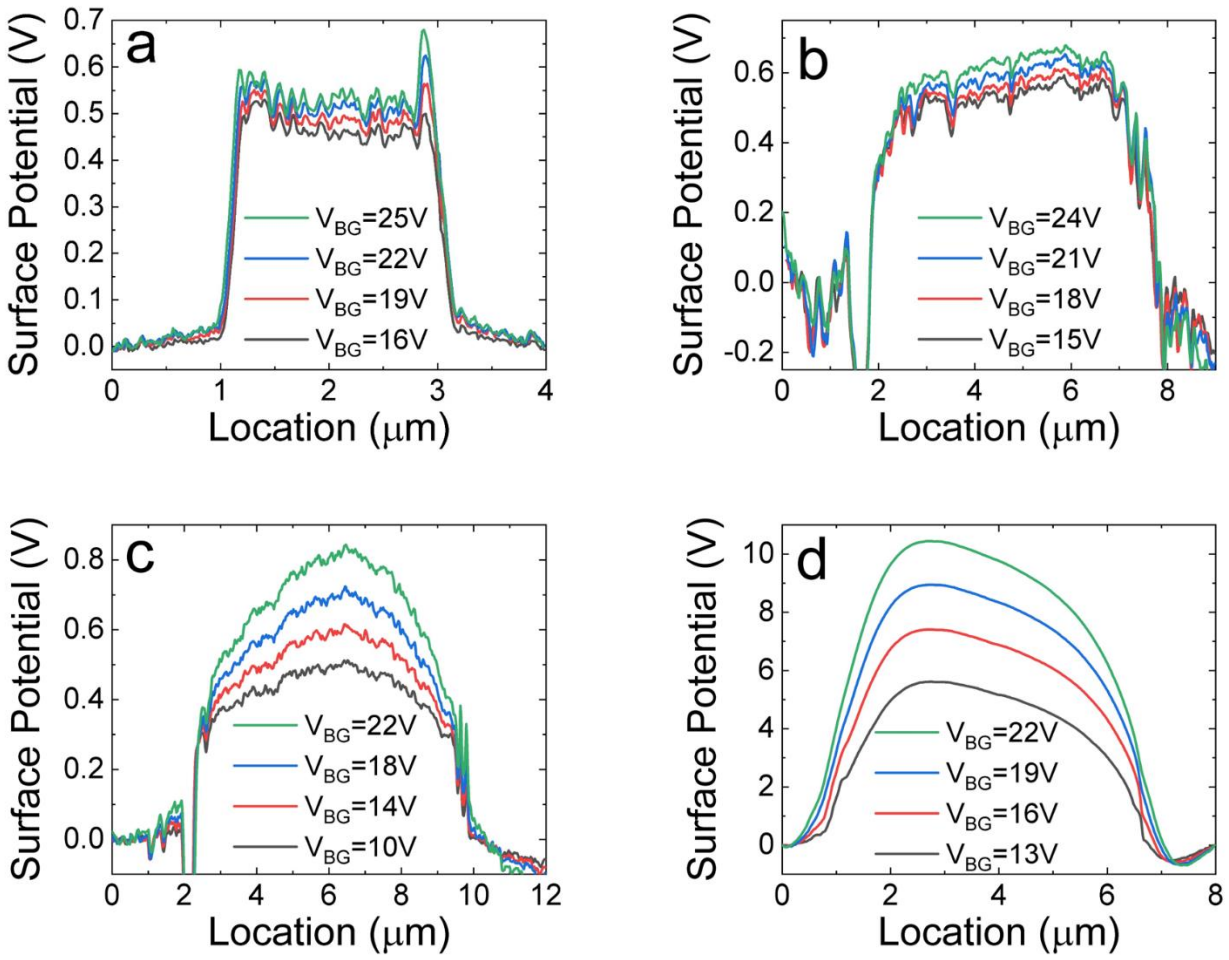

FIG. 2. Surface potential measurements at varying positive V_G, while $V_S = V_D = 0\,V$. (a) Bilayer short channel device – complete screening. (b) Multilayer (35 layers) long device – complete screening. (c) trilayer long device – incomplete screening. (d) Monolayer long device – very poor screening.

The cross-sectional surface potential traces in Fig. 2(a) and (b) show that for the short channel bilayer device and long channel bulk device, the change in V_X is in the order of a few tens of milielectron volts for high gate voltages which is consistent with the expected shift of the Fermi level, indicating that these devices fully screen the applied back-gate voltage, rendering the contribution of V_X negligible for the determination of mobility.

In contrast, for the case of longer channels and thinner devices, this assumption no longer holds. V_X values in panels (c) and (d) are in the order of a few hundreds of millivolts to a few volts, respectively, showing that these channel partly screen the gate potential. It is therefore evident that both the channel thickness and its length strongly influence its ability to fully screen the back-gate voltage, and thus for thin devices of up to few layers, with channels longer than $5\mu m$, V_X must be accounted for in the calculation of mobility.

To explain the shape of V_X in Fig. 2(c) and (d), we must consider the electrostatics of the device along the current transport (source-channel-drain) direction, termed here the x-axis, and along the capacitive stack (gate-dielectric-channel) direction, termed here the z axis. Fig. 3 shows a finite element simulation in the x-z plane of a short ($3\mu m$) and a long ($6\mu m$) channel devices, where the source (S) and drain (D)

electrodes are grounded, the gate potential is set to +10V and the top boundary is set to a floating potential to emulate the configuration of a device.

Below the source and drain electrodes and in their immediate vicinity, the electrode potentials V_S and V_D form a constraint on the residual surface potential, setting it to zero. In contrast, away from the electrodes the residual potential increases and reaches a maximal value over the center of the channel. It is therefore clear that the strong dependence of V_X on the distance from the contact dictates that longer channels will result in a less effective screening of the gate bias. Panel (c) of Fig. 3 shows a comparison of the surface potential V_X for the short (red) and long (blue) channel devices, 2 nm thick, at a distance of 10nm over the channel.

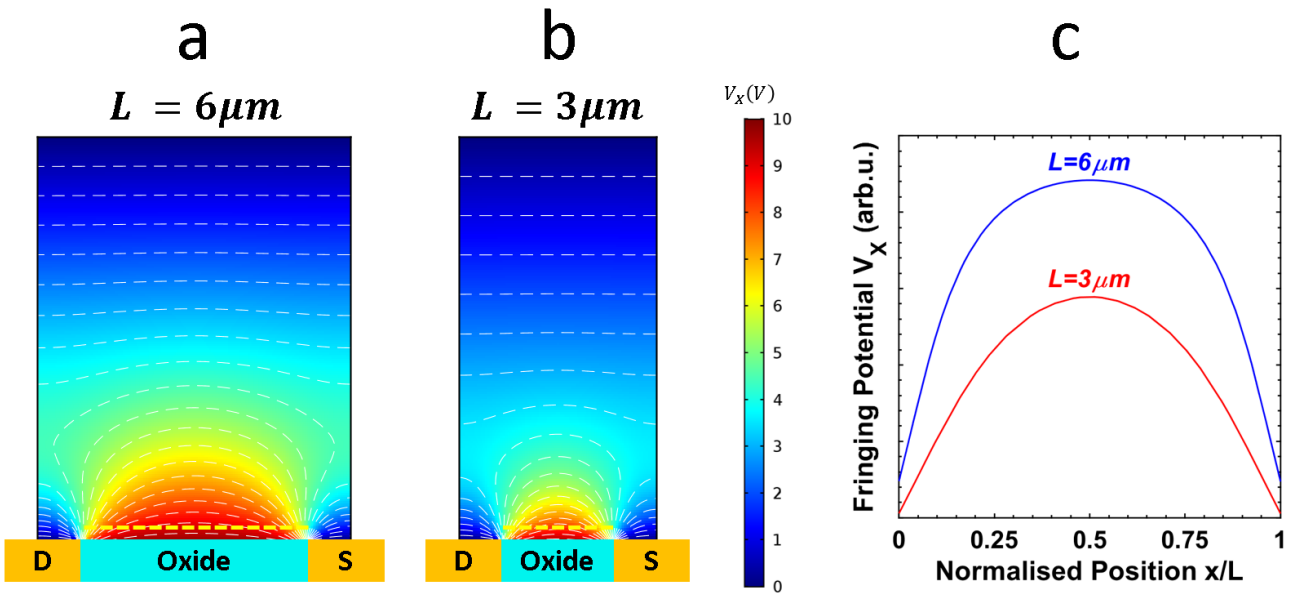

FIG. 3. A finite element electrostatic simulation of 2 nm thick devices (a) a short channel ($L = 3\mu m$) and (b) a long channel ($L = 6\mu m$) device. (c) A cross-sectional surface potential at a distance of 10nm over the channel for the short (red) and long (blue) channel devices.

To account for the incomplete screening, a second correction must be added to the mobility calculation. In the cases shown in Fig. 2(c) and (d), where the surface potential changes along the channel, we can describe the semiconductor as a series of resistive 'slices', with local resistivity of $\rho(x)$, width of W and a 'slice' length of dx. The local resistance is then $R_x = \rho(x) \cdot dx/W$. The equivalent circuit resistance, $\langle R \rangle$, which is calculated by integrating over the channel length, yields terms for the equivalent resistivity ($\langle \rho \rangle$), and equivalent conductivity ($\langle \sigma \rangle$), which can be used to correct the calculation for mobility, which now takes the form:

$$\mu_n = \frac{1}{C_{OX}} \cdot \frac{d\langle\sigma\rangle}{dV_{BG}} \cdot \left[\frac{d}{dV_{BG}}\left(\left[\frac{1}{L}\int_{x=0}^{L} \frac{dx}{V_{BG}-V_X-V_{th}}\right]^{-1}\right)\right]^{-1} \equiv \frac{1}{\beta \cdot C_{OX}} \cdot \frac{d\langle\sigma\rangle}{dV_{BG}} \quad \textit{Equation.3.}$$

Appendix B of the supplementary information contains the full derivation of Eq. 3. The entire correction is contained in the new term β which is calculated numerically from the raw data. β can be regarded as the spatial-mean fraction of the applied gate potential that induces charge accumulation in the channel. $\beta = 1$ is the ideal case where all of the applied gate bias is screened by the channel, whereas when $\beta < 1$, the channel can be viewed as subjected to a spatially uniform gate bias of βV_{BG}.

By plotting the term $\left[\frac{1}{L}\int_{x=0}^{L}\frac{dx}{V_{BG}-V_X-V_{th}}\right]^{-1}$, denoted as the effective gate bias in Fig. S4 of the supplementary , as a function of the gate bias, we can estimate β as the slope of the fitted line. For the trilayer device, the correction factor is found to be $\beta_{3L} = 0.98$, which indicate a minor correction for the estimation of mobility. In contrast, for the monolayer device, the correction factor is found to be $\beta_{1L} = 0.53$, which indicates that a significant part (47%) of the applied gate bias remains unscreened and that a significant correction is required for calculating the mobility in the monolayer case.

As expected, applying the modified mobility equation (Eq.3) to the long-channel trilayer device leads only to a minor increase in the value of the mobility compare to the value obtained by correcting for contact resistance alone, whereas applying it to the long-channel monolayer device yields a significant increase in the calculated mobility. All the results are summarised in Table 1.

Calculation method	Mobility $\frac{cm^2}{V\cdot s}$			
	Monolayer $L = 5.65\ \mu m$	Bilayer $L = 1.75\ \mu m$	Trilayer $L = 7.5\ \mu m$	35 Layers $L = 6.25\ \mu m$
Uncorrected two terminal Field-effect Mobility	2.52	4.17	5.06	7.82
Contact resistance corrected Field-effect Mobility	9.54	10.77	23.47	26.07
Partial gating corrected Field-effect Mobility	17.88	-	24.04	-

Table 1. Mobility values obtained for each sample using the three different calculation methods. The third calculation is only demonstrated for the samples described in Fig. 2 (c) and (d), which showed incomplete screening of V_{BG}.

Conclusions

In summary, we have developed a methodology for accurately measuring the mobility of layered and ultrathin semiconductors by eliminating the effects of contact resistance and incomplete gate potential screening. The method was demonstrated on MoS_2 devices varying in thicknesses and channel lengths. Our method can be used for calculating the inherent field-effect mobility of semiconductors and independently measure the resistance of Schottky contacts. Crucially, we have shown that partial screening of the back-gate voltage is inherent to the electrostatics of thin semiconductors, and therefore affects the calculation of mobility in any field-effect method, with the most significant effects manifesting in very thin channels with lengths of over a few microns.

The methods presented here clearly demonstrate that the source of reduced observed mobilities in mono- to trilayer TMDCs are the formation of highly resistive contacts and overestimated accumulation of charges in thin channels. Our research is therefore instrumental in helping to focus the scientific efforts in improving contact formation and measurement accuracy.

Materials and Methods

Monolayer MoS_2 flakes were mechanically exfoliated by the Scotch Tape method, initially developed for graphene[58], from commercially available MoS_2 bulk crystals (*Structure Probe, Inc.*). Following exfoliation, the flakes were mechanically transferred onto a highly doped, p-type Si substrate bearing 90 nm of thermally grown SiO_2. The flakes chosen for device fabrication were identified by their colour contrast in an optical microscope following procedures that were previously reported[59]. The contacts were patterned onto the flakes using a standard electron beam lithography procedure followed by metallisation with Ti/Au 3/60 nm using electron beam evaporation. The devices were soaked in *N*-Methyl-2-pyrrolidone (NMP) at 80 ºC for 60 min before lift-off, and then wire-bonded onto a chip carrier. Four devices were produced in this way, differing by their thickness and length: a relatively short bilayer with $1.75\ \mu m$ channel, and three longer devices – monolayer, trilayer and multilayer, with channel lengths of $5.65\ \mu m$, $7.5\ \mu m$ and $6.25\ \mu m$, respectively. Electrical measurements were conducted using a semiconductor parameter analyser (*B1500A, Agilent Technologies*). Amplitude modulation atomic force microscopy (AM-AFM) coupled with KPFM measurements were performed in dual frequency mode configuration, using Dimension Edge, Bruker Inc. All measurements were performed inside an N_2 glove box (with water content <1.5ppm).

Acknowledgments

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Supporting Information

Including: AFM mapping and Raman spectroscopy of monolayer to multilayer MoS_2 sheets.MoS_2 based transistors devices characteristics. Surface potential mapping of all devices *in operando, via* KPFM, as well as complete mathematical derivation of Equation 3. This material is available free of charge via the Internet at http://pubs.acs.org.

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