Graphical Abstract

3D Structures for Silicon Carbide Transistors utilizing Al_2O_3 as a gate dielectric

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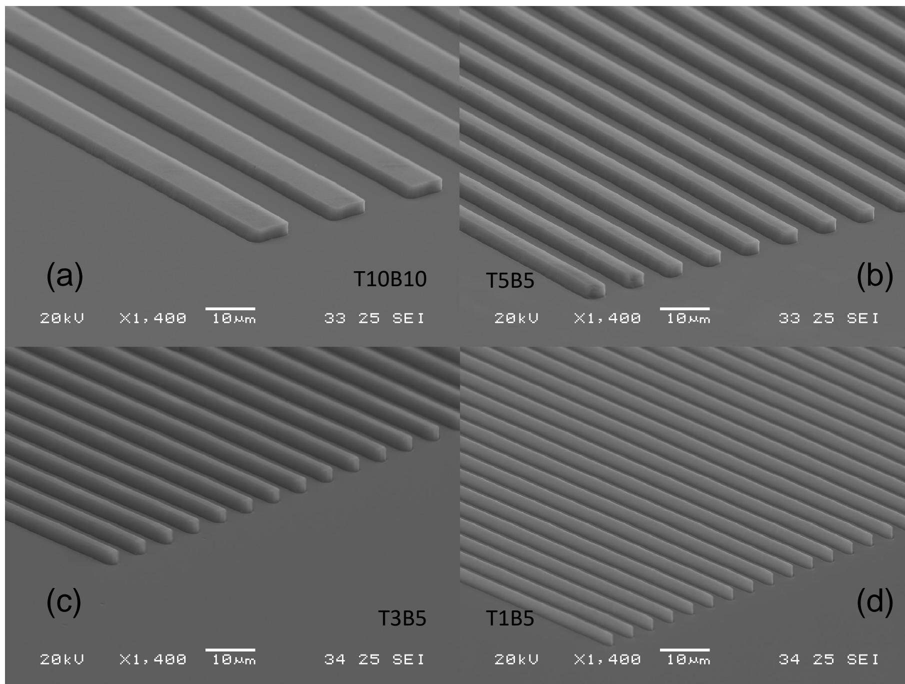

Highlights

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- For the first time, the characteristics of 3D structures formed in silicon carbide for the realisation of ultra-high performance nanoscale transistors, based on the FinFET topology is investigated.
- C-V characteristics show evidence of a second flatband voltage, located at a higher bias than that seen for purely planar devices.
- Two distinct peaks in the conductance – voltage characteristics are observed, centered at the flatband voltages, where the peak located at high bias correlates with the behaviour of the sidewall area.

3D Structures for Silicon Carbide Transistors utilizing Al_2O_3 as a gate dielectric

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ABSTRACT

This paper reports on the first investigation of the characteristics of 3D structures formed in silicon carbide for the realisation of ultra-high performance nanoscale transistors, based on the FINFET topology. Capacitance – voltage characteristics show evidence of a second flatband voltage, located at a higher bias than that seen for purely planar devices. Two distinct peaks in the conductance – voltage characteristics are observed, centered at the flatband voltages, where the amplitude of the high voltage peak correlates with the sidewall area. This suggests that the chemical behaviour of the sidewalls differ from those of the (0001) wafer surface. The breakdown electric field of the dielectric film grown on the 3D structure is in excess of 3 $MVcm^{-1}$. It is demonstrated that 3D transistors (FINFETs) do not utilise the gate voltage range where the abnormal characteristics exist and so this work reports for the first time the possibility of high performance nanoscale transistors in silicon carbide that can operate at high temperatures.

1. Introduction

The move to nanoscale transistors has been the key enabler in the realisation of high performance electronic systems. In order to facilitate the continued reduction in physical dimension of devices to the nanometer scale, 3-D structures, in the form of FINFETs [1] are an area of active research in silicon technology in order to minimise short channel effects. These 3-D structures are often formed by etching features in the surface of the semiconductor to form devices (that include the sidewalls) which result in higher levels of gate control and hence enhanced performance. However, silicon technology cannot function in environments where the temperature exceeds 175 °C, as commonly found in a wide range of industrial applications. In these environments, 4H-SiC has become the most suitable candidate for next generation electronic devices for deployment in extreme environments [2, 3] because of the chemical stability of the carbon – silicon bond. The hexagonal crystal structure of silicon carbide results in significantly different surface chemistry of the sidewalls in comparison to the planar (0001) surface – a situation that does not occur in silicon technology. Hence, the realisation of nanoscale 3-D transistors in silicon carbide is a greater challenge than in silicon because of the influence of the chemistry of the sidewall.

The demand for high performance, miniaturised resilient electronic circuits operating in environments where the temperatures exceed 300 °C has grown significantly in the last few years, with SiC offering solutions due to its superior electrical properties [4, 5, 6]. At present 4H-SiC devices with gate lengths in excess of 1 μm have been used to demonstrate simple circuits in automation, aerospace and home appliances [7]. The challenge of maintaining the electrostatic integrity of a short channel MOSFET at high temperatures has limited the aggressive scaling of silicon carbide devices, however the enhanced control of the 3D gate structure in a FINFET could mitigate this, leading to significant potential enhancements in performance for high temperature logic circuits.

For the multi – μm scale MOSFETs being researched at the present time, one of the main technological concerns in 4H-SiC technology is that of electrically active defects at the SiO_2/SiC interface, leading to a high density of interface states (D_{it}) near the conduction band edge, resulting in low effective inversion channel mobility [8, 9]. This appears

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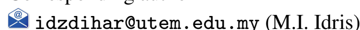
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to reduce capability of 4H-SiC MOSFETs, which means that the performance is below that predicted theoretically. The effective mobility is reduced by Coulombic scattering by trapped charges [10], interface states and fixed oxide charges, which decreases the number of free carriers in the channel [11]. The reported [12, 13, 14] channel mobility in 4H-SiC MOSFETs has increased due to the development of post-oxidation annealing techniques using nitrogen [15] and phosphorous [16], which act to passivate defects at the SiO_2/SiC interface. However, the extracted mobility characteristics are still significantly lower than the technical capability of the material, so further improvements are still required to realise the true potential of the technology.

In power device technology an attractive approach to increase the channel mobility is to use a vertical trench MOSFET structure which utilizes the sidewall of the trench, typically the $(11\bar{2}0)$ face, to enhance the drain current and improve gate control [17, 15]. The vertical trench power MOSFET structure produces good device performance with high channel density and low resistance. It is well known that different surface orientations of 4H-SiC have anisotropic electrical properties and show differing oxidation rates and surface roughness values. An enhanced drain current has been demonstrated by the use of a 3-D gate structure power MOSFET owing to the anisotropic mobility properties of 4H-SiC on different planes. This indicates that the development of 3-D structures offers a route to high performance nano – scale devices that are capable of operating in high temperature environments, because 3-D gate MOSFETs have better control of short channel effects [18, 19].

The inability to control the threshold voltage in FINFET structures in a manner similar to that of a planar MOSFET is a critical challenge in the realisation of nanoscale transistors in materials such as silicon carbide. Hence, a systematic study is required to identify the effect of the sidewall surface on the device characteristics, which is vital if this technology is to be used for nanoscale devices. One of the challenges in fabricating FINFET structures is the etching process to realise the 3-D gate structure which might cause damage to the surface and result in a high interface state density [20]. In this study, for the first time, the characteristics of 3D structures formed in silicon carbide for the realisation of ultra-high performance nanoscale transistors, based on the FinFET topology is investigated. 3-D MOS capacitors have been fabricated on 4H-SiC, alongside planar (etched) and planar (non-etched) structures, as shown in Figure 1, to investigate the effect of the 3-D gate structure on the characteristics of the gate capacitor (the critical part of a MOSFET device). As the surface area of 3-D MOS capacitors is larger in comparison to the conventional planar capacitor on the same footprint, it is expected that 3-D MOS capacitors will give higher capacitance compared to the planar capacitor. The planar capacitors on etched and non-etched surfaces act as a reference to understand the characteristics of the trench bottom and top surface of the finger that comprise the 3-D MOS capacitors. 3-D MOS capacitors with different sidewall planes were also investigated, by rotating the angle of the etched fingers on the wafer surface in multiples of 15° with respect to $(11\bar{2}0)$.

2. Device fabrication

A schematic cross-section of the MOS capacitor with 3-D gate structure is shown in Figure 1. The height of the gate structures were 1.3 μm and the width of the top finger, T was varied between 10 and 1 μm whilst the bottom trench, B is fixed at 5 and 10 μm.

4° off-axis 4H-SiC samples with a 10.6 μm thick epitaxial layer with a nitrogen concentration of 6×10^{15} cm^{-3} were used as the starting material. A SF_6 and O_2 plasma with power of 200 W at a pressure of 30 mTorr was used to etch trenches of depth of 1.3 μm in a reactive ion etching (RIE) process. After the removal of metal mask (Titanium/

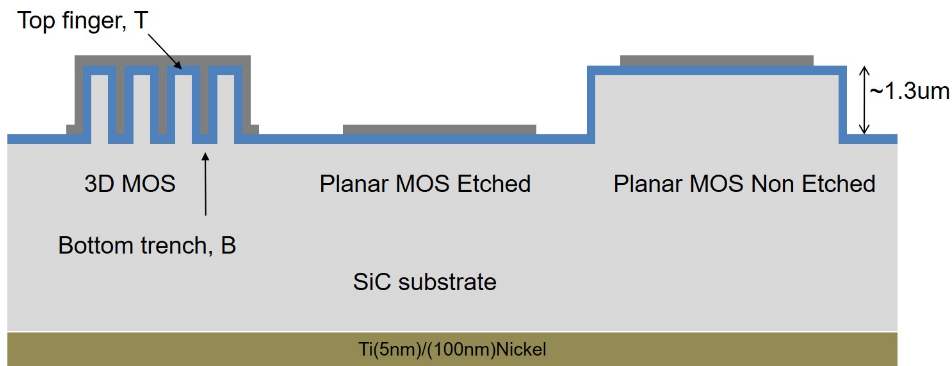

Figure 1: Schematic illustration of the cross-section of 3-D gate structure MOS capacitor.

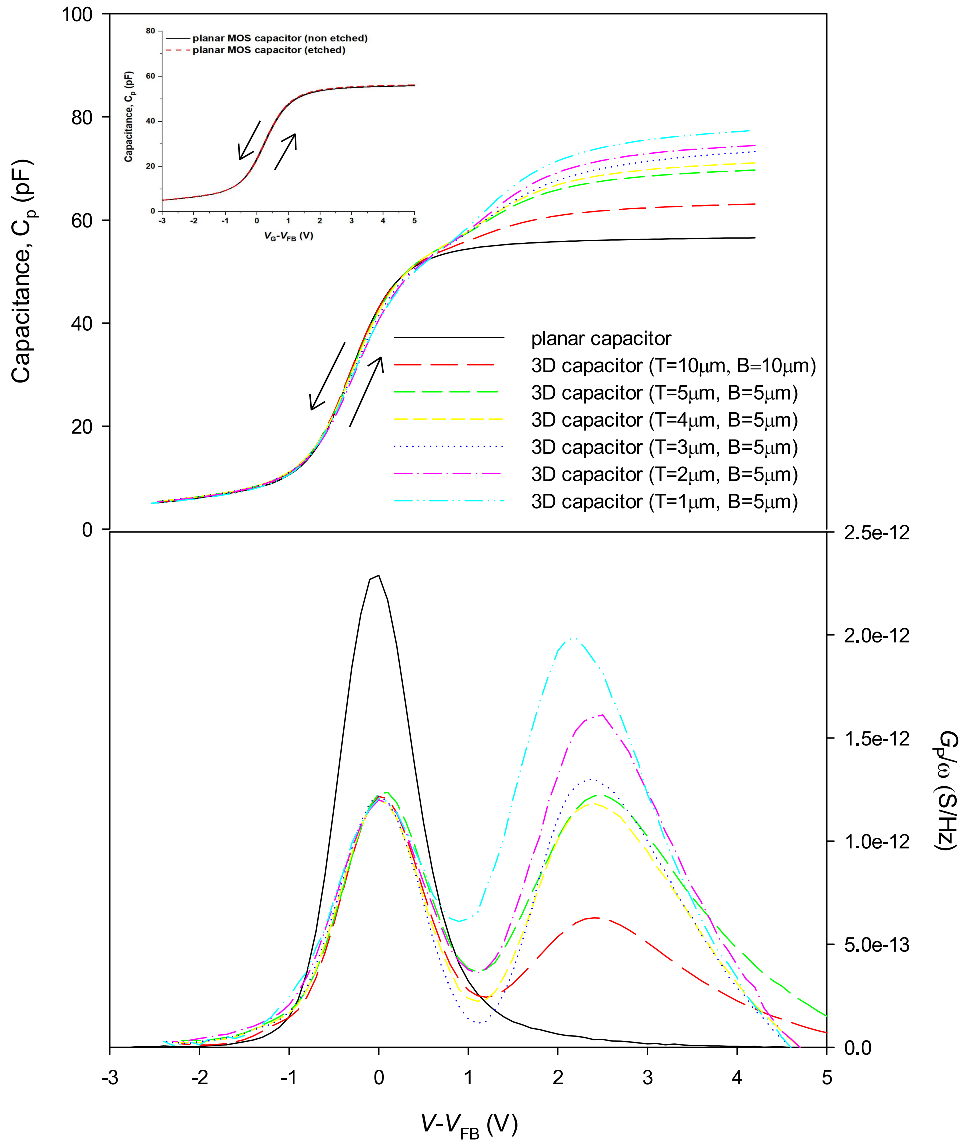

Figure 2: 1 MHz capacitance – voltage and conductance – voltage characteristics of 3D MOS capacitors at room temperature. (Inset: The comparison of C-V characteristics of etched and non etched MOS capacitor).

Nickel), the surface was recovered using a sacrificial oxidation process, followed by BHF dip to remove any process related damage prior to the dielectric deposition. 40 nm of Al_2O_3 was deposited by ALD at 300° using using trimethylaluminum (TMA) and H_2O as precursors. A Ti (5 nm)/ Ni (100 nm) stack was deposited on backside of the wafer and annealed for 200 s at 1050°C in forming gas using an RTP process. Aluminium was deposited using PVD to act as the gate metal and patterned to give contacts with dimensions of 200 μm × 200 μm.

3. Results and discussion

The data in Figure 2 show the capacitance – voltage and conductance – voltage characteristics of the 3-D MOS capacitor structures with different sidewall areas when were applied from the accumulation to deep-depletion region.

Almost no hysteresis was observed for both planar and 3D MOS capacitor at the room temperature (Data are not shown here). The data is plotted as a function of gate overdrive ($V_G - V_{FB}$) based on the flatband voltage extracted for the planar structures. In the legend, T refers to the width of the finger and B the width of the trench in μm. The capacitance data show an enhancement in the accumulation capacitance, which increases with the sidewall area. The increase in the capacitance as a function of the capacitor surface area is shown by the data in Figure 3, with a 43% enhancement observed. The linear relation between the accumulation capacitance and the surface area of the capacitor indicates that the ALD process used for the growth of the Al_2O_3 is conformal, with identical film thicknesses on the sidewalls and (0001) planes. This is in contrast to what is typically observed with thermally grown SiO_2 on SiC, which is significantly thicker on the sidewalls, resulting in a reduction in the capacitance increase with the formation of a 3D structure [17, 18]. The capacitance data in the figure also show what appears to be a second MOS depletion characteristic located at $V_G - V_{FB} \approx 2$ V due to the vertical or sidewall capacitance. Using standard analysis, the dopant concentration related to the two regions can be extracted – giving 6.0×10^{15} cm^{-3} for the lower voltage (at around $V_G - V_{FB} = 0$ V), which we relate to the (0001) surface and 1.0×10^{18} cm^{-3} for the higher voltage section ($V_G - V_{FB} \approx 2$ V). The dopant concentration of the lower voltage data matches the dopant concentration in the epilayer used to fabricate the devices, whilst the higher voltage dopant concentration is significantly higher, as reported previously for SiO_2 based dielectrics on SiC [21]. The doping mechanism on different crystal orientations is complicated and the doping efficiency is known to change as a result of the existence of surface steps (which in this case arise from the intentional off-angle of the substrate). One hypothesis for this discrepancy is the difference in the surface stoichiometry of the sidewall in comparison to the planar surface (Si or C coverage) and desorption of impurity atoms during processing may result in the high effective dopant concentration. However, analysis of the doping profile for 3D MOS capacitor using conventional analysis may have an intrinsic limitation as the planar portion of the capacitor is under accumulation whilst the sidewall capacitors are depleted and this can potentially influence the

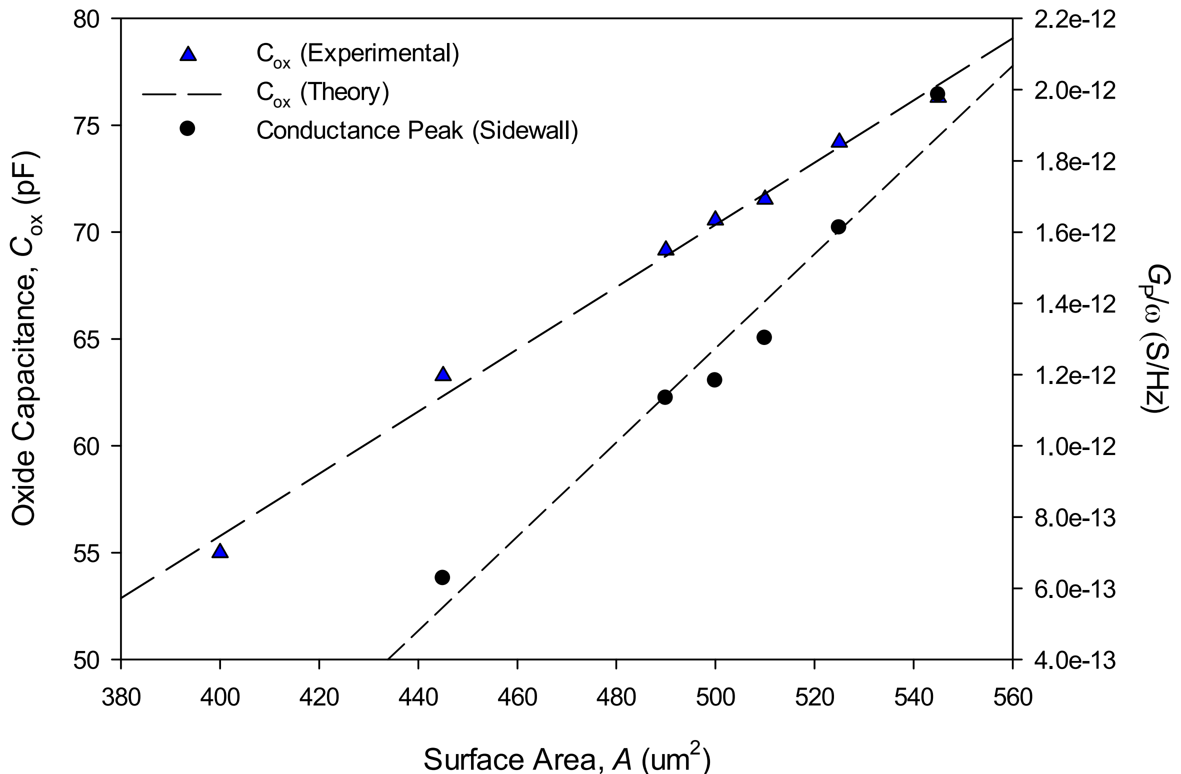

Figure 3: Variation in capacitance and conductance with sidewall surface area. The dielectric constant for the gate dielectric of the Al_2O_3 is approximately 7.2.

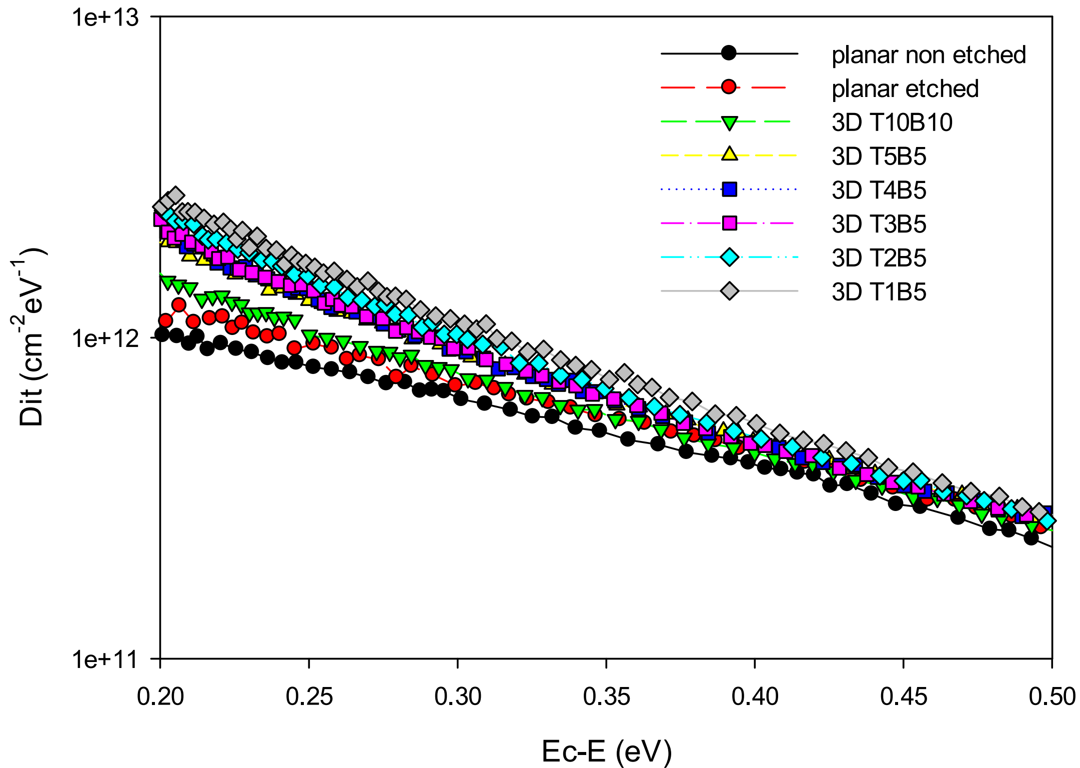

Figure 4: The distribution of interface state density as a function of energy within the bandgap, extracted using the $C-\psi$ technique for 3D MOS capacitors with different sizes. Planar capacitors of etched and non-etched were also included in the figure as a reference

extracted dopant concentration for the high voltage data.

The data in Figure 2 also shows the variation in peak conductance for the capacitors. The planar devices show a single conductance peak, located at the flatband voltage that is fully symmetric, suggesting that the dielectric / SiC interface is of high quality. The 3D structures that showed evidence of the second capacitor in the characteristics also show a second conductance peak that is located at $(V_G - V_{FB}) \approx 2.5$ V. The influence of the sidewall angle on the additional capacitance and conductance characteristics observed in the data from Figure 2 was also studied in this work. However, there is no significant difference observed in terms of either the accumulation capacitance or the height of the conductance peak with changes in the angle. One possible explanation for the lack of a significant difference in the characteristics is related to the tilt angle of the trench sidewalls from the actual crystal plane since the 3-D MOS capacitors were fabricated on a commercial 4° off wafer. Reduction of the offcut angle may yield a greater level of clarity in this regard, however the data presented here is relevant to the realisation of devices on commercially available production grade wafers. For the data reported here, for one 3-D structure, the data includes contributions from two planes of $(11\bar{2}0)$ and $(\bar{1}\bar{1}20)$ on the same structure. It was reported that the mobility of $(\bar{1}\bar{1}20)$ is only half of $(11\bar{2}0)$, which is the opposite plane [22]. The magnitude of the second peak height scales with the surface area of the sidewalls, as shown by the data in Figure 3. The different heights of the peaks in the conductance – voltage characteristics are related to the capacitance of the traps at the SiC/SiO_2 interface and the trap generation / recombination time constant. The conductance, G_P, normalised by the angular frequency of the exciting voltage can be expressed as

$$\frac{G_P}{\omega} = \frac{C_{it}}{2\omega\tau_p} \ln\left[1 + \left(\omega\tau_p\right)^2\right] \quad (1)$$

where C_{it} is the capacitance of the interface traps and τ_p the lifetime of the trapping state.

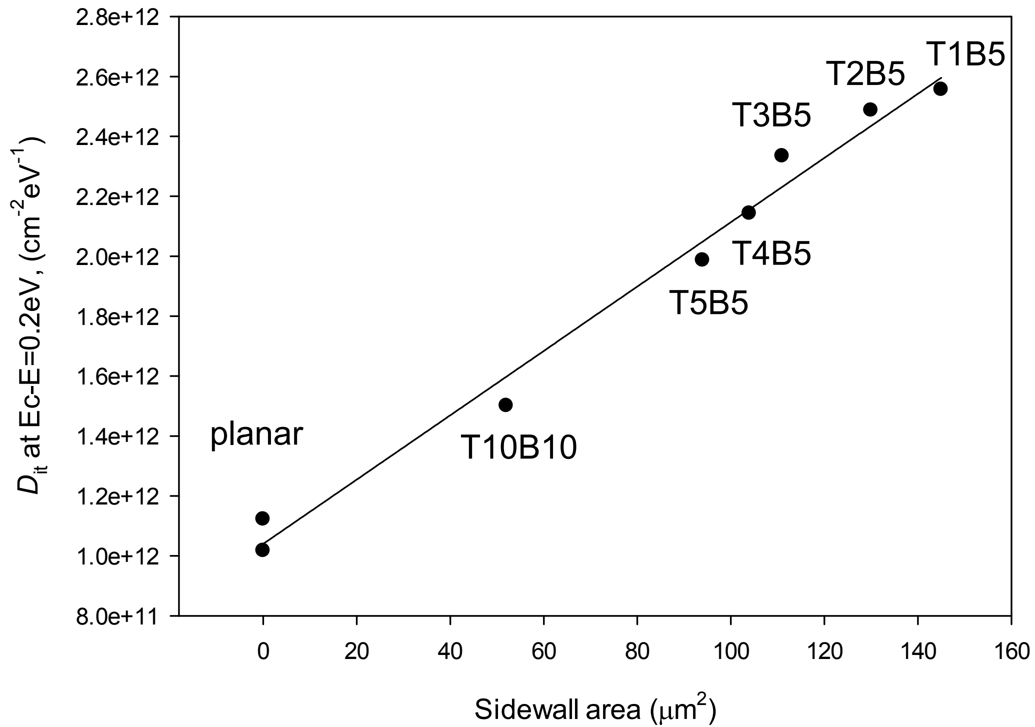

Figure 5: Interface state density of 3-D MOS capacitors near conduction band, $E_c - E$=0.2 eV as a function of sidewall area, extracted using $C - \psi$ technique.

In order to identify the influence of C_{it} on the peak height, the distribution of interface state density as a function of energy for the 3D capacitor structures with different sidewall areas is shown by the data in Figure 4. The interface state density was extracted from quasi static capacitance measurements using the $C - \psi$ technique, which accurately reports the concentration of slow traps at the dielectric interface [23]. The unetched planar capacitors that were fabricated alongside the 3D structures show the expected exponential dependence of D_{it} with energy, with a value of 1×10^{12} cm^2eV^{-1} at $(E_C - E) = 0.2$ eV, which is comparable to data published in the literature for a range of dielectrics on 4H-SiC [16, 23, 24, 25]. The etched planar MOS capacitors exhibit a slight increase in the interface state density near the conduction band [21]. As can be seen from the data in the figure, the value of D_{it} close to the conduction band increased with the sidewall area in 3D MOS capacitor. The legend for each capacitor describes the width of the finger (T value) and the width of the trench (B value). The data in Figure 5 show a linear relation between the area of the sidewall and the interface state density that has been extracted from the $C - \psi$ technique close to the conduction band. The two data points at zero sidewall area relate to the unetched surface (lower point) and the etched surface (upper point) confirming that the additional surface roughness does not play a significant role in the interface state density values reported. The data show a factor of 3 increment in D_{it} for the T1B5 structure in comparison to the T5B5, which correlates with the increase in conductance peak height seen in Figure 2. Hence we ascribe the difference in the conductance peak height with changes in the capacitance arising from trapping states at the SiC/SiO_2 interface, rather than changes in the recombination / generation lifetime.

These results are in good agreement with those published for FINFET structures in other materials, including silicon and InGaAs [26, 27] where the interface state density at the sidewall is high in comparison to that at the top surface. In silicon FinFET technology, the surface damage and sidewall profile have became issues with the electrical characteristics. In order to improve the surface of the trench structure on the sidewall, previous reports in the literature state that hydrogen annealing is effective in reducing surface roughness and hence improve the electrical characteristics such as gate leakage, subthreshold slope and drain-induced barrier lowering in SiC [28].

The origin of the higher flatband voltage for the sidewall component of the characteristics can be described by the difference in the polar nature of the two different surfaces. The observed shift in the flatband voltage for the two

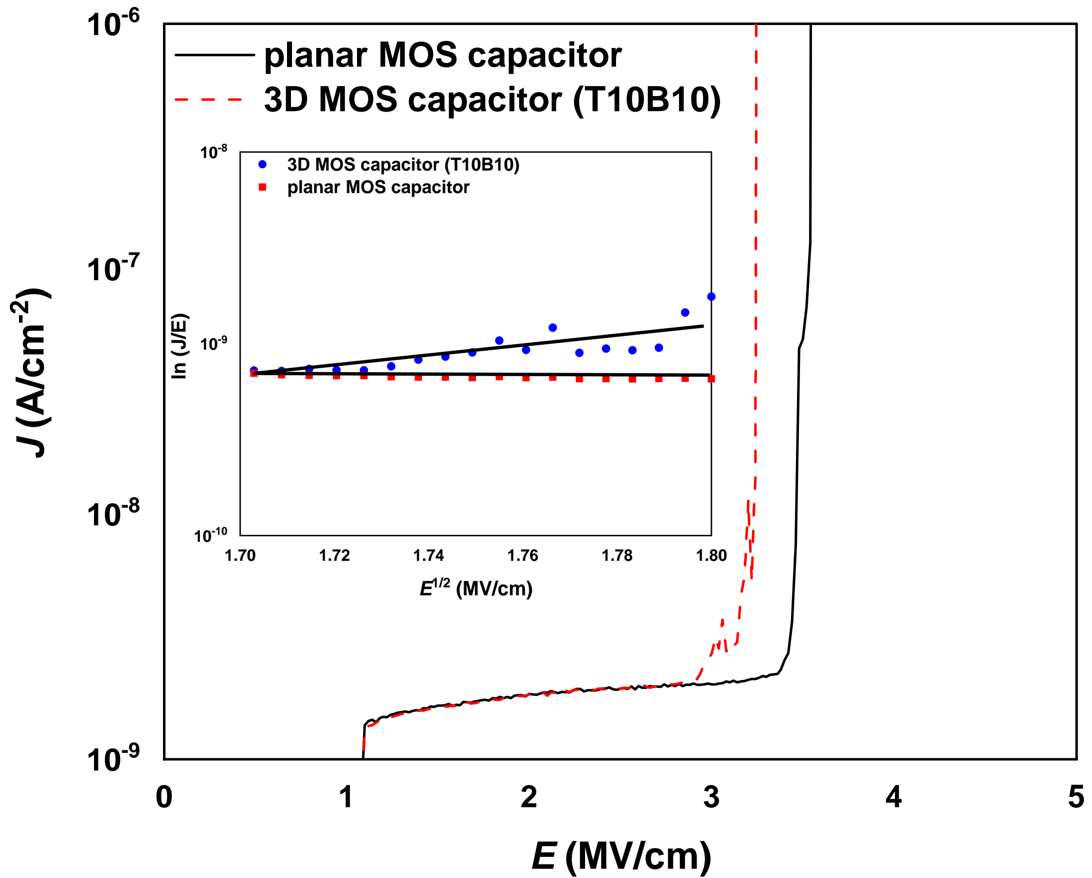

Figure 6: Leakage current density through the Al_2O_3 film, for both planar and 3D structures. (Inset: Data are presented as a Frenkel–Poole plot showing the dependence of the leakage current density divided by the oxide electric field versus the square root of electric field. The linear slopes imply Frenkel–Poole emission in the Al_2O_3).

conductance peaks cannot be explained by the observed shift in the position of the Fermi level that arises from the different dopant concentrations extracted from the capacitance – voltage characteristics. The Fermi level will rise by 0.125 V, which is an order of magnitude lower than the 2 V shift observed in the conductance data. The effect of different crystallographic surfaces on the characteristics of polar semiconductors has been described previously [29] and we relate the increased voltage to the higher density of unsatisfied chemical bonds that are formed on the sidewall of the 3D structure.

The existence of the non-ideal features in the positive capacitance and conductance characteristics of the 3D structures will not degrade the behaviour of the transistor when operated in a circuit. When operating in the on-state, the bias on the capacitor is such that the surface of the semiconductor is inverted, forming the conductive channel. For the data presented here, this equates to the application of a negative bias where the characteristics of the 3D structure are identical to those of the planar devices.

The data in Figure 6 show the leakage current density through the Al_2O_3/SiC junction. The data show the expected Poole–Frenkel behaviour for electric fields between 1 and 3 $MVcm^{-1}$ and critical electric fields of 3.4 $MVcm^{-1}$ for the planar and 3.2 $MVcm^{-1}$ for the 3D structures. These values are comparable to the 4 to 5 $MVcm^{-1}$ reported in the literature for amorphous Al_2O_3 on Si [30], which indicates that the high temperature annealing does not result in the formation of an underlying SiO_2 layer. From the analysis of the leakage current ln (J/E) vs $E^{1/2}$, the Frenkel-Poole

mechanism match with the experimental data at low electric field. As can be seen in the inset in Figure 6, the linear slopes at low electric field imply Frenkel- Poole emission [30, 31, 32]. The breakdown field for the 3D structure is lower than for the planar device, suggesting that the inclusion of the sidewall reduces the oxide quality but the conduction band offset is unchanged, indicating that the sidewalls do not have a significantly higher surface charge density than the planar (0001) surface. This supports the hypothesis that the increase in D_{it} for the 3D structures is related to the high density of unsatisfied chemical bonds at the surface of the sidewall. However, the breakdown field for both the planar and 3D structures remains above 3 $MVcm^{-1}$, which is sufficient to form an inversion layer and hence operate the transistor.

4. Conclusion

The data show that 3-D gate structures (FIN MOS) capacitors, a key component of nanoscale MOSFETs, hold the promise of achieving high capacitance densities on the same footprint area, with a demonstrated enhancement of 43%. The enhancement of the accumulation capacitance is linearly dependent on the sidewall area of the capacitor. The capacitance–voltage characteristics for the 3D structures show evidence of a second depletion behaviour at a higher flatband voltage than those observed in a purely planar device and this second flatband voltage is identical to the location of a second peak in the G/ω–V characteristics. The chemistry of any unterminated chemical bonds on the sidewall is different to that of the planar (0001) surface and this results in the observed second flatband voltage in both the C–V and G/ω–V characteristics, as well as the observed increase in the interface state density, D_{it}. This work shows that the 3D structure is highly promising for the fabrication of high temperature logic devices for extreme environments.

CRediT authorship contribution statement

M. Idzdihar Idris: Investigation, Data curation, Writing - Original draft preparation. **Alton B. Horsfall:** Writing - Review and Editing, Supervision.

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