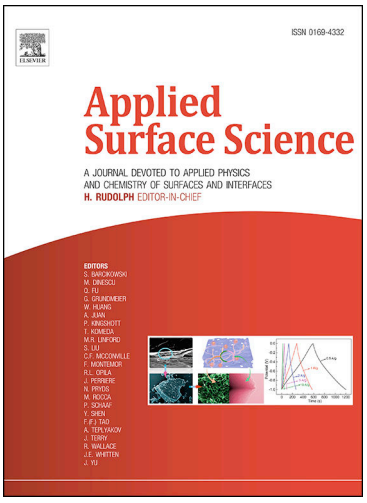
Journal Pre-proofs



Fully controllable silicon nanowire fabricated using optical lithography and orientation dependent oxidation

Sami Ramadan, Leon Bowen, Sinziana Popescu, Chen Fu, Kelvin K. Kwa, Anthony O'Neill

PII: S0169-4332(20)31273-3
DOI: https://doi.org/10.1016/j.apsusc.2020.146516
Reference: APSUSC 146516

To appear in: *Applied Surface Science*

Received Date: 18 February 2020
Revised Date: 22 April 2020
Accepted Date: 26 April 2020

Please cite this article as: S. Ramadan, L. Bowen, S. Popescu, C. Fu, K.K. Kwa, A. O'Neill, Fully controllable silicon nanowire fabricated using optical lithography and orientation dependent oxidation, *Applied Surface Science* (2020), doi: https://doi.org/10.1016/j.apsusc.2020.146516

Fully controllable silicon nanowire fabricated using optical lithography and orientation dependent oxidation

Sami Ramadan,[a,b] Leon Bowen,[c] Sinziana Popescu,[a,d] Chen Fu,[a,e] Kelvin K. Kwa,[a] Anthony O'Neill*[a]

[a]*School of Electrical, Electronic and Computer Engineering, Newcastle University, Newcastle upon Tyne NE1 7RU, United Kingdom. E-mail: anthony.oneill@ncl.ac.uk*

[b]*Department of Materials, Imperial College London, London, SW7 2AZ, United Kingdom*

[c]*Department of Physics, Durham University, Durham DH1 3LE, United Kingdom*

[d]*School of Life & Health Sciences, Aston University, Birmingham, B4 7ET, United Kingdom*

[e]*University College of Physics and Optoelectronic Engineering, Shenzhen University, Shenzhen, 518060, China*

ABSTRACT

Silicon nanowires (SiNWs) exhibit unique electrical, thermal, and optical properties compared to bulk silicon which make them suitable for various device applications. To realize nanowires in real applications, large-scale and low-cost fabrication method is required. Here, we demonstrate a simple, low-cost fabrication process to produce silicon nanowires (SiNWs) with full controllability of size and length. The nanowires are fabricated using optical lithography and orientation dependent oxidation. Highly uniform single crystalline nanowires with thicknesses down to 10 nm, lengths up to 3 cm and aspect ratios up to approximately 300,000 are formed with high yield. The technology is further simplified to fabricate more complex structure such as metal-oxide-semiconductor field-effect-transistors (MOSFETs) by means of the selective etching of silicon without the need for extra steps. This method is distinct from other top-down techniques, where the formation of nanowires at low-cost, using simple processing steps, with high controllability and reproducibility is major challenge. This controllable and CMOS-compatible technology can

offer a practical route to fabricate nanostructures with tuneable properties that can be the key for many device applications including nanoelectronics, thermoelectric and biosensing.

1. INTRODUCTION

Silicon nanowires are considered for use as a building block in a wide range of applications including in the fields of electronics[1-3], photonics[3-7], energy[8-10], health care[11-16] and biology[13, 17-24]. The integration of silicon nanowire into functional devices for future applications requires low-cost, scalable, robust, reproducible and simple fabrication technology. Moreover, nanowire-based technology requires high precision in device definition, surface quality and density. The ability to control the crystal surface and orientation of fabricated devices can also be crucial in many applications, including energy and electronic devices.

Bottom-up methods can produce high quality nanowires with controlled diameter [25-28]. However, there are still a number of issues associated with this approach such as the alignment of nanowire, the incorporation of metal impurities during nanowire growth, and the integration of the nanowire into conventional CMOS technology[29]. Top down methods such as optical and electron beam lithography have dominated the area of IC manufacturing for decades. Their applications for achieving nanometre array structures with high control of doping, position and feature sizes are still superior. However, further scaling using these techniques requires either additional tools or conditions, such as in Extreme UV (EUV), or slow and expensive ones such as electron beam lithography (EBL).

Among many developed fabrication methods, the indirect top-down methods that use optical lithography have attracted lots of attention due to their cost-effective [30-33]. Some of the techniques that use anisotropic wet etching together with thermal oxidation and optical lithography[34, 35] promise scalable and low-cost fabrication of nanowire and show potential success in biosensing application[36]. Such techniques use dielectric film such as silicon

nitride to act as a mask during thermal oxidation of silicon. However, these processes have controllability and reproducibility issues. Reproducibility largely depends on the properties of nitride film and its resistance to thermal oxidation. Although, there are some attempts to improve the reproducibility and controllability, the issue of controlling the final structure due to the local oxidation of silicon (LOCOS) process[37]. In addition, the number of steps involved results in the increased complexity of these methods. In this paper, we show that silicon nanowires can be fabricated without the need of such complex processing. This technology overcomes the major challenges, associated with other indirect top-down methods[34, 35], such as issues of using silicon nitride mask during thermal oxidation and the formation of LOCOS structure. Improvements in process controllability, reproducibility and simplicity compared to other technologies are achieved by utilizing orientation-dependent oxidation which eliminates the need to use silicon nitride masks during thermal oxidation and the complexity associated with this, such as the selection of nitride film that has high resistance to thermal oxidation and high selective etching over silicon dioxide. Consequently, the bird's beak effect produced during sidewall oxidation, which affects the controllability of the shape of the nanowires is eliminated.

The principle of this fabrication method is based on the fact that the thermal oxidation rate and anisotropic wet etching change with the crystal orientation of the silicon surface. It has been well documented that the oxidation rate of silicon at temperatures between 750-1000 °C is orientation-dependent, where the rate at the silicon (111) surface is higher than that at the silicon (100) surface[38-40]. It is also well known that Si(111) acts as an etch stop in alkaline solutions. Our fabrication process combines these two characteristics of silicon to produce silicon nanowires. We show that our method can produce nanowires with lengths up to centimeter scale and simultaneously thickness down to sub-10 nm. We have further simplified the process to form nanowires via selective etching, which can then be integrated

into MOSFET structures without additional process steps. Although many methods have been reported in the last decade to fabricate sub-50 nm nanostructures with no need to use high resolution techniques, this technique is simple and offers high tunability of the nanostructure, in addition to the ability to form a complete MOSFETs structure with no need to use additional steps. This enables such structures to be readily used in the creation of More Than Moore mixed technology platform.

2. RESULTS AND DISCUSSION

2.1 Orientation-dependent oxidation of silicon

The role of the orientation-dependent oxidation of silicon is an important factor in the formation of the nanowires. The oxidation of silicon at temperatures between 750-1000 °C depends on the density of silicon atoms on the planes[38, 41]. As the (111) plane has a higher density of available bonds compared with the (100) plane, the oxide grows faster at the (111) face[41]. Although, orientation-dependent oxidation has been well studied theoretically and experimentally, it is the first time a silicon nanostructure is fabricated using this technique.

The oxidation kinetics of silicon is generally described by a linear-parabolic rate law. In the linear rate law, the growth is reaction-controlled, where the reaction occurs at the boundary between the silicon and the oxide, and the oxide growth follows a linear relationship with time. In the parabolic rate law, growth is diffusion-limited and the growth follows the square root of the oxidizing time. The general expression of oxidation behaviour in silicon is given by([38], p.374):

$$x^2 + Ax = B(t + \tau) \qquad (1)$$

where x is oxide thickness at a given oxidising time (t), the linear rate law represents the oxidation for a short duration and is generally given by([38], p.374):

$$x = \frac{B}{A}(t + \tau) \qquad (2)$$

Here, B/A is the linear rate constant, and τ is the initial oxidation time where the oxidation behaviour does not follow a certain growth law. The linear rate for Si(111) is larger than that for Si(100), and the typical oxidation rate between these two orientations is given by:

$$(\frac{B}{A})_{(111)} = 1.6 * (\frac{B}{A})_{(100)} \qquad (3)$$

The parabolic rate law represents the oxidation for long duration and is generally given by:

$$x^2 = B(t + \tau) \qquad (4)$$

where B is the parabolic constant. The linear constant (B/A) is proportional to the chemical reaction rate of oxidation, which depends on the density of Si-Si bonds available for reaction, so is different for Si(111) and Si(100) surfaces. However, the parabolic constant (B) is primarily dependent on the diffusivity of oxygen through the growing oxide layer. Therefore, as the oxide thickness increases, the ratio of oxide growth for Si(111) and Si(100) approaches 1.

In order to calculate the oxidation thickness ratio between the Si(100) and Si(111) surfaces, process simulation using TCAD Sentaurus is performed on SOI substrate. The top silicon layer is patterned and etched in such a way that the top surface of Si(100) forms an angle of 54.7° with the sidewall Si(111). Thermal oxidation is performed at 950 °C for 20 min (**Fig.** 1(a)). The oxidation thickness ratio between Si(100) and Si(111) is 1.42, and the oxidation rate is reduced at the concave corner between BOX/Si where the ratio is 1.12. This reduction could be explained due to a reduction in oxidant species at the corner due to viscous stress. The oxide layer at the top silicon surface is then completely etched using both the anisotropic and isotropic wet etching of oxide. The etched thickness is 10% greater than that on the top

surface to represent the real process. The remaining thickness of the oxide at the sidewall is 5 nm, which is enough to act as a mask during the second wet etching process. The oxide at the bottom corner also remains.

In our experiments, the oxide thickness ratios between Si(100) and the sidewall plane are approximately determined (**Fig.** 1(c)). Silicon samples are oxidised at a temperature of 950 °C and for various times. The oxidation was performed to obtain a thickness in the linear region in the reaction-controlled regime where oxidation is orientation-dependent. In these experiments, silicon substrates with etched structures were oxidised at various temperatures to grow oxide on <100> with different thicknesses from 14 nm to 30 nm. The thickness of oxide on Si (100) is determined using the profiler. Buffered oxide etch (BOE) is used to etch an amount of oxide equivalent to the thickness on Si (100). To determine the ratio of oxide on (111) to (100), the samples are etched in BOE followed by TMAH etching to form the nanowires. Failures in forming the nanowires indicate that there is no oxide at the sidewall or the oxide at the sidewall is not sufficient to act as a mask.

By fitting the experimental data of oxide thicknesses at Si(100) and Si(111) in Fig. 1(c), we determined the oxide ratio from the slope as:

$$t_{<111>} = 1.41 * t_{<100>} \qquad (5)$$

The oxide thickness on Si(111) and Si(100) is further confirmed using FIB. **Fig.** 1(d) is the result of oxidation at 950 °C for 40 mins. The oxide thicknesses on the Si(111) (region B) and Si(100) (region A) are measured to be 38 nm and 25 nm respectively with ratio of 1.46. The oxide thickness at the concave corner (region C) is 32 nm with oxide ratio of 1.23 between C/A. The oxidation at the concave corner can be enhanced by reducing the stress using higher oxidation temperature. Further experiments are required to optimize the oxidation process.

147 During the BOE etching of oxide at the Si(100), the same thickness of oxide at the sidewall is
148 also etched, However, due to the variation in oxidation rate between the silicon at the
149 sidewall and at the concave corner, the excessive oxide etching process can result in
150 completely etching the oxide at the sharp edge. This can result in nanowire with a convex
151 shape at the bottom. This can be avoided by using the anisotropic etching of silicon dioxide
152 using RIE. The RIE process requires high etch selectivity of SiO_2 over silicon to ensure that
153 the silicon underneath is not etched during the process. Fluorocarbon gases such as C_2F_4
154 mixed with hydrogen, CHF_3 mixed with hydrogen or $C_5HF_7/O_2/Ar$ have been reported to give
155 high selective etching of SiO_2 over Si[42]. These gases can be used to etch the silicon dioxide
156 layer. However, in our experiment, BOE was sufficient to prove the concept.

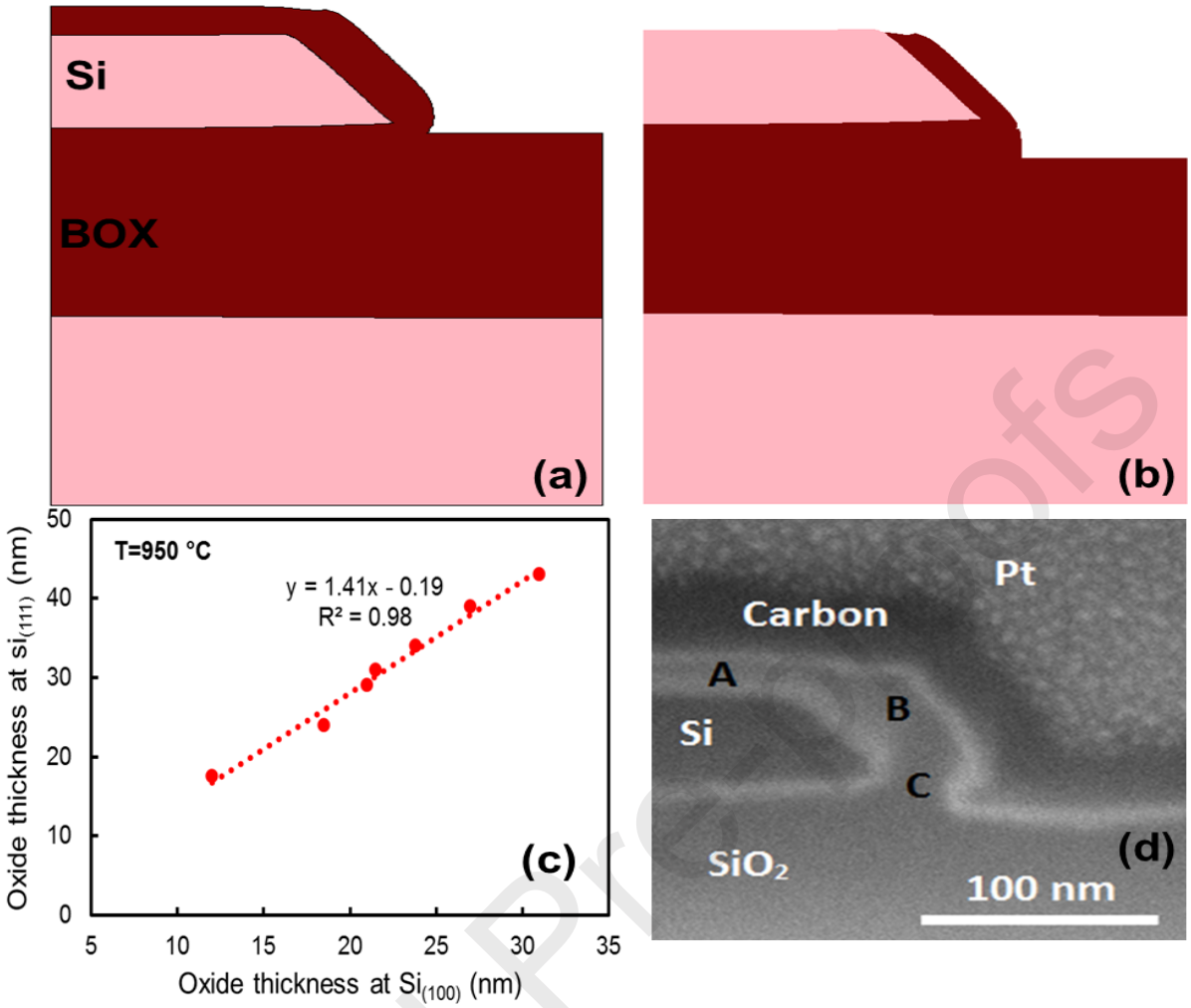


Fig. 1. Orientation-dependent oxidation of silicon structure. (a,b) 2D simulation of oxidation of silicon structure. (a) Oxidation at 950 °C for 20 mins. (b) The structure after the removal of oxide at the Si(100). (c) Experimental results of oxide thickness at Si(111) and Si(100) at oxidation temperature of 950 °C. (d) FIB cross-section of oxidised sample at 950 °C for 40 mins showing oxidation at different regions.

2.2 Fabrication of silicon nanowire using orientation-dependent oxidation

A novel method of fabrication of silicon nanowires using optical lithography has been developed. The novelty of this technique is based on the orientation-based etching and oxidation of silicon. This method can be used to fabricate nanowires on Si or SOI substrates. **Fig.** 2 shows an overview of the fabrication process of SiNWs on SOI(100) substrate. A 25%wt Tetramethylammonium hydroxide (TMAH) solution with 10% IPA added at 63 °C is utilized to form the 1st side of the NWs at the (111) plane. TMAH etchant etches single crystalline silicon at different rates for different crystalline orientations; for example where

171 the etch rates in the Si(100) and Si(110) directions are much faster than in the Si(111)
172 direction. Due to the anisotropic characteristics of TMAH etching, the etch stops at the (111)
173 plane and produces an angle of 54.7° with the <100> plane (**Fig.** 2(a)). The IPA is added to
174 the solution to improve the smoothness of the sidewall. A buffered oxide etch (BOE) is used
175 to remove any oxide on the silicon surface. The substrate is oxidised at 950 °C where
176 oxidation occurs on both Si(100) and Si(111) surfaces (**Fig.** 2(b)). The grown thickness on
177 (100) is measured to be about 21 nm. As the oxidation rate at the Si(111) is higher than at the
178 Si(100), the thickness grown on the Si(111) is higher compared with the Si(100). The
179 approximate oxide thickness on <111> is about 28 nm. The silicon oxide layer grown on
180 <100> is etched using BOE. The etch rate of silicon dioxide in the BHF solution is 1.25
181 nm/Sec. The etching time should be controlled to keep sufficient oxide at the <111> plane to
182 act as a mask during the second anisotropic etching step (**Fig.** 2(c)). The exposed silicon on
183 the Si(100) is then etched using 25%wt TMAH solution with 10% IPA added at 63 °C (**Fig.**
184 2(d)).

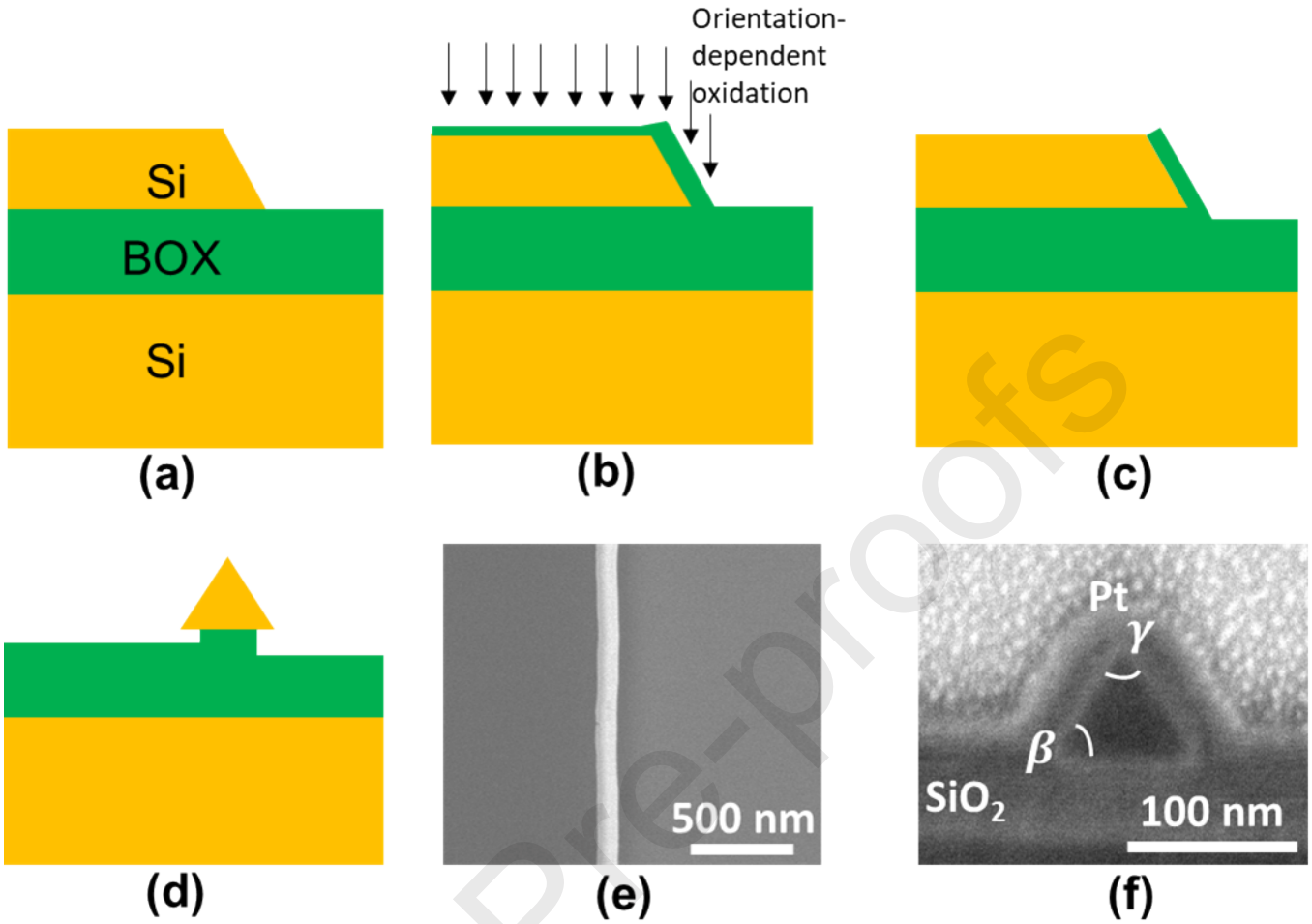


Fig. 2. Silicon nanowire fabrication process. (a-d) Schematics of the nanowire fabrication process on SOI(100). (a) First anisotropic wet etching of silicon. (b) Orientation-dependent oxidation of silicon. (c) BOE Etching of silicon dioxide at the Si(100). (d) Second anisotropic etching of silicon and sidewall oxide removal. (e) SEM top view of the nanowire. (f) Cross-section of the nanowire obtained by focus ion beam (FIB).

Fig. 2(e,f) shows representative SEM images of SiNWs fabricated using this process. The cross-section of the nanowire (**Fig.** 2(f)) is obtained using a focused ion-beam (FIB). As shown, the process produces NWs with triangular shape. The height of the nanowire (h) is measured to be 54 nm. The sidewall angle (β) between (111) and (100) is measured to be approximately β≈ 54° and β≈ 51° at the left and right edges of the triangle respectively. The measured angle (γ) between the two intersection (111) planes is γ≈ 75°. The theoretical values of (β) and (γ) are 54.7° and 70.6° respectively. The slight deviation in the angle could be because that Si(111) was not completely exposed during the TMAH etching as a result of etching time and misalignment. The variation in thermal oxidation rate at the corners could

also lead to this small deviation in the angle. The width of the triangle is given by $w = \frac{2h}{\tan\beta}$ and measured to be 84 nm. The quality of sidewall of the nanowires can be controlled by the wet etching process. Atomically smooth sidewall surfaces can be achieved by utilizing TMAH with high concentration where the etch rate at Si(111) is very slow [37, 43-45]. The etch profile strongly depends on several factors, including impurities in the etchant, temperature, concentration and defects in the silicon crystal. The orientation, shape and surface quality of the nanowires make this technology suitable for sensing applications. It has been reported that Si(111) orientation has high chemical stability and is the preferable orientation for surface functionalization [46], whereas the triangular cross-section of the nanowire has been reported to obtain the highest chemical response compared to other shapes [47]. Therefore, such nanowires can be configured as field-effect-transistors (FETs) to be used for label-free and selective detection of biomolecules.

2.3 Controllability of the size of the nanowires

The fabrication process can be used to produce triangular silicon nanowire of any length and size. The nanowire can be formed in a controllable manner with high uniformity. The length of nanowire can be controlled by changing the length of the photomask layer prior to the anisotropic wet etching step. We fabricated an ultralong nanowire with a high aspect ratio of approximately 300,000:1. **Fig.** 3(a) shows the analysis of 18 SEM scans along a nanowire with 3 cm in length. The analysis was performed at different positions along the substrate. The AFM profile in **Fig.** 3(c) represents a segment on the NWs with a thickness of 103 nm and length of 50 μm. The variations in width and thickness were 5% and 2% respectively. This high uniformity in structure is generally difficult to obtain using bottom-up methods [48]. We further measured the electrical resistivity of 22 positions along the nanowire length using four-probe measurements. The measured value of electrical resistivity was 8.04 X 10^{-}

^{3}±5.33 X 10^{-4} Ω.cm with variation in resistivity of 6.6% along the nanowire. The fabrication of this kind of highly uniform nanowire is suitable for a different range of applications, including biosensors and nanoelectronics [48-52]. Long nanowires allow building a large number of FET transistors into an individual silicon nanowire which can improve the integration of electronic circuits and device performance [48-52]. Moreover, the high electrical and structural uniformity of the nanowire devices make them ideal for DNA sequencing where the high uniformity level between devices are required [48]. Integration of ultralong NWs devices into flexible substrates can provide the opportunity to extend the applications of nanowires [48-52]. The thickness of the nanowire can be simply controlled by the duration of time the samples are placed in the etchant during the second etching step. TMAH and KOH can be employed to control the size of the nanowire. However, due to its non-zero etching of oxide and long etching time, using KOH could cause a failure in the process. In this method, we used 25 wt% TMAH at 63 °C, to reduce the size of the nanowire. This method can be used to form nanowire of any size. In this work the smallest height was obtained of 10 nm as shown in the SEM and AFM images in **Fig.** 4(a) and 4(b) respectively.

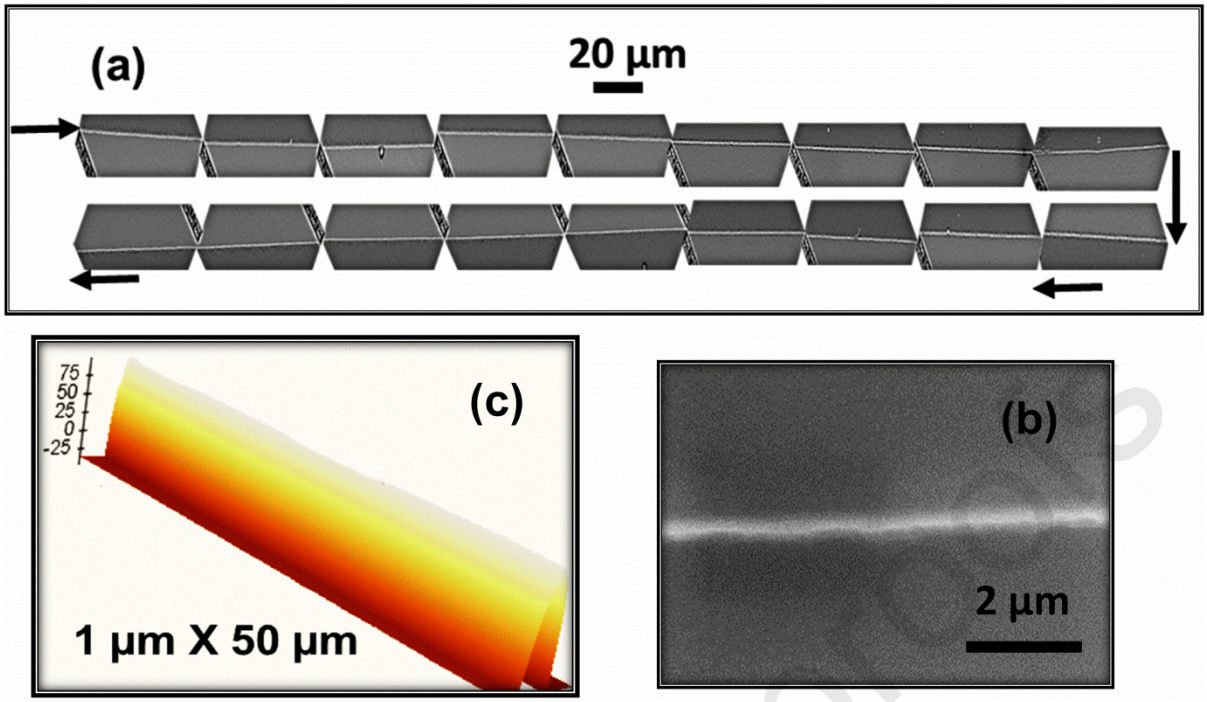


Fig. 3. Ultralong SiNWs. (a) Series of 18 SEM images of a 3 cm long SiNW, each segment being 63 µm long. (b) Top view SEM image of a segment of nanowire at higher magnification. (c) AFM profile of a NWs segment.

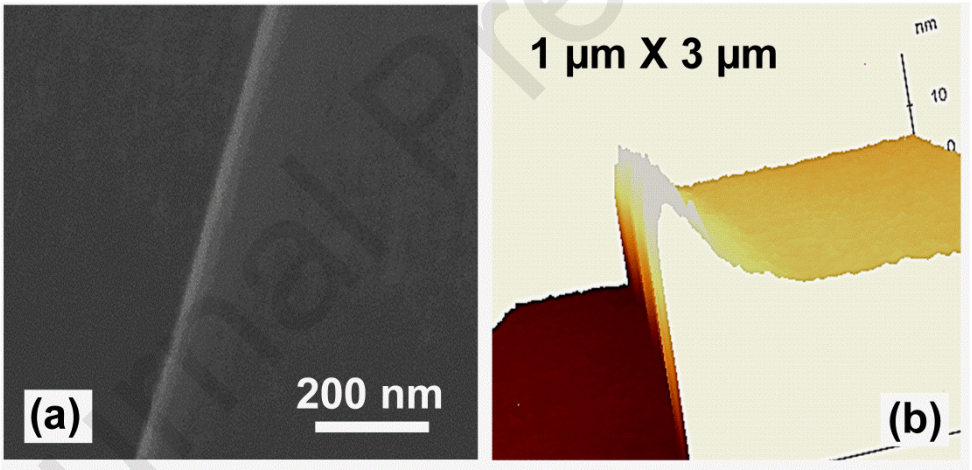


Fig. 4. 10 nm SiNW. (a) SEM top view of the nanowire. (b) AFM image of the nanowire (h≈10 nm)

2.4 Formation of nanowires by means of selective etching

The selective etching of nanowire is based on the principle that the etching rate of heavily doped silicon in anisotropic wet etching is much slower than a lightly doped one. Palik et al. have reported that heavily doped n- and p-type silicon act as etch stops in alkaline etchants of silicon [53]. They have reported a drastic reduction in etch rates of phosphorous-doped

silicon with a concentration of about 5 X $10^{20}cm^{-3}$. According to H. Seidel et al., the etch rate of boron-doped silicon in an alkaline etchant of silicon with a concentration larger than 2 X 10^{19} cm^{-3} becomes dopant-dependent [54]. The etch rate has been reported to be inversely proportional to the fourth power of boron concentration.

Therefore, if thin layers of undoped and heavily doped regions are etched using anisotropic wet etchants such as KOH or TMAH, the undoped region can be completely etched before the heavily doped region is attacked by the etchant.

In several devices such as the NW MOSFET used in electronic devices, undoped nanowire is connected to heavily doped source and drain regions. The fabrication of these types of structures using indirect top-down methods requires an additional lithography step to protect the source and drain during nanowire formation. The fabrication of nanowires via selective etching can allow the formation of nanowire with its source and drain using a single fabrication step. In our method, this can be achieved by adjusting the second anisotropic wet etching step of silicon.

In order to fabricate NWs using this principle, a thick oxide layer of about 130 nm is grown on Si to act as a doping mask, and standard lithography and BOE etching are performed to open a window through the oxide. The SOD is applied through the open window followed by diffusion at 1050 °C in pure N_2 to obtain a boron doping level of 9.8 X 10^{19} cm^{-3}. The glass and oxide layers are removed using BOE. **Fig.** 5(a) shows a schematic structure of the two regions. A layer of oxide is then patterned to define the undoped NW device region. This followed by TMAH etching at 63 °C (**Fig.** 5(b)). Thermal oxidation is performed to protect the sidewall oxide (**Fig.** 5(c)), followed by a carefully selected etching time in BOE to remove the oxide on the (100) surface (**Fig.** 5(d)). The nanowires are then formed by etching selectively the undoped region (**Fig.** 5(e)). **Fig.** 5(f) shows an AFM image of p++ region/p

SiNWs after 1 min etching in TMAH at 63 °C. The heavily doped boron region acts as an etch stop. The thickness of the heavily doped region is measured to be about 100 nm while the thickness of the nanowire is 85 nm. The relative etch rate of heavily doped (9.8 X 10^{19} cm^{-3}) to lightly doped (1 X 10^{15} cm^{-3}) is measured to be 0.023. It is expected that the etch rate ratio can be further reduced by increasing the doping level in the doped region. The thickness of the nanowire and the doped region can be controlled by adjusting the time the samples are placed in the etchant. This principle can be used to fabricate nanowire MOSFET (p++ S/D and channel) in a single step with no need for an extra lithography step. This process is suitable for p-type silicon as the etch rate for n-type silicon, is not significantly influenced by doping concentration.

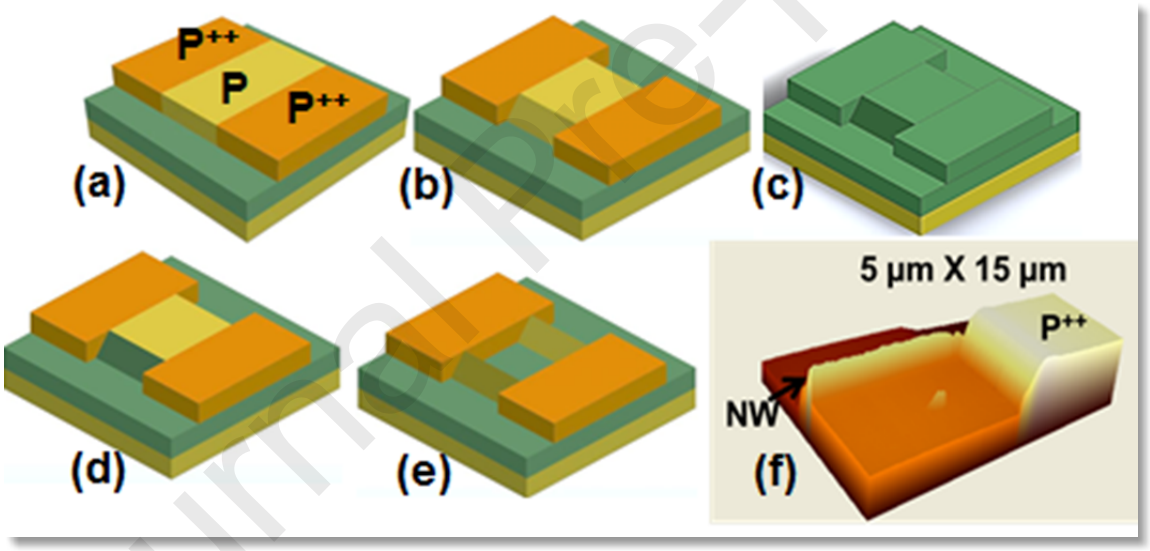


Fig. 5. Schematics of the fabrication process steps of nanowire formation by means of selective etching. (a) Selective doping of SOI substrate. (b) First anisotropic wet etching of silicon. (c) Thermal oxidation of silicon. (d) BOE Etching of silicon at the Si(100). (e) Second anisotropic etching of silicon and sidewall oxide removal. (f) AFM image of an undoped NW with heavily doped silicon structure.

2.5 Electrical characterization

A series of electrical measurements were performed to determine the properties of the nanowires, including effective resistivity, carrier concentration and specific contact resistance. Four-probe measurements were performed to eliminate the effect of contact

resistance and to measure the resistance of the nanowires. Electrical current was applied between the two outer probes, while the voltage drop between the inner probes was measured. **Fig.** 6(a) shows an SEM image of the four-probe on the single silicon nanowire with Ti/Al contacts. Ti/Al was used as a contact to the nanowire because it can form ohmic contacts to n-type doped silicon. The nanowire channel outside the contact area is protected by thermally grown oxide layer to reduce the effect of interface traps. The SEM image of the top view of the nanowire at higher magnification is shown in **Fig.** 6(b). The SOI substrate was doped with an n-type to a level of 8 X 10^{18} cm^{-3} prior to nanowire formation using the spin-on-dopants method. The nanowire resistance R_{NW} and effective nanowire resistivity ρ_{eff} are extracted from $R_{NW} = \frac{I_{14}}{V_{23}} = \rho_{eff}\frac{l_1}{A}$, where l_1 is the distance between the two inner probes (2,3) and A is the cross-section of the nanowire. Representative results for two- and four-probe I-V curves of nanowires devices with a cross-section of 7.5 X 10^3 nm^2 are shown in **Fig.** 6(c). The cross-section of the nanowire was measured using AFM (**Fig.** 6(d)), where the increase in nanowire width due to the effect of the AFM tip radius is calculated based on the technique reported in previous work. For nanowires with a length of 17 μm, the average measured electrical resistivity was 0.0076 Ωcm. Effective carrier concentration was calculated based on the measured electrical resistivity. The carrier density in silicon nanowire was 6.8 X 10^{18} cm^{-3}. This value is slightly lower than the one measured for the SOI substrate. The reduction in carrier concentration could be attributed to interface traps at the Si/SiO_2. The total resistance was measured using a two probe measurement set-up and is given by $R_T = \frac{V_{14}}{I_{14}}$. The contact resistance was then measured using the equation $R_T = 2R_C + \rho_{eff}\frac{l_2}{A}$, where l_2 is the distance between the outer probes (1,4). The average value of contact resistance was about (36 ± 3) kΩ. The contact resistance contributes to about 7 % of the total resistance, and can be further reduced by using large contact pads or by increase doping level. The contact

resistance value was used to extract the transfer length (L_T), which is an important parameter that defines the distance that most current flows into or out from the contact. L_T is calculated from $R_C = \frac{\rho_{eff} L_T}{A} \coth\left(L/L_T\right)$, where L is the contact length. The average value of L_T is 1.9 µm. The specific contact resistivity was calculated by generalizing the nanowire transmission model in circular cross-section to an arbitrary cross-section. Because $L_T < L$, the specific contact resistivity is calculated using $\rho_C = P_I L_T R_C$, where P_i is the perimeter of the nanowire. The extracted value of $\rho_C = 1.9\ X\ 10^{-4}$ Ωcm^2. Values of specific contact resistivity smaller than 10^{-6} Ω.cm^2 are required for low contact resistance. This can be achieved by increasing the doping level of the nanowire and careful annealing of the devices.

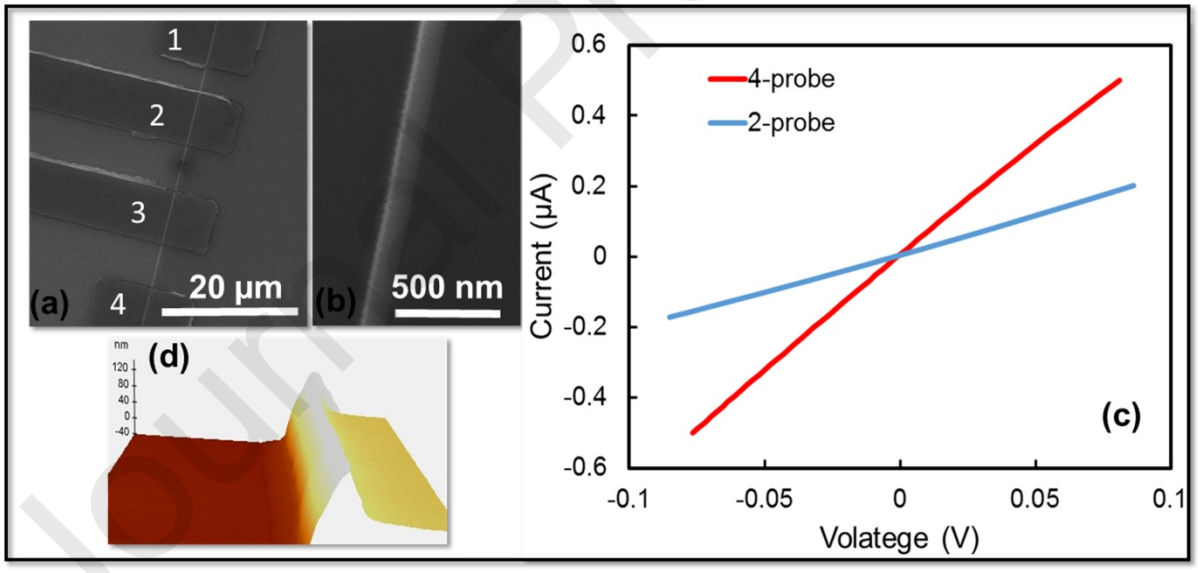


Fig. 6. Measured electrical characteristics of silicon nanowire with thickness of 103 nm. (a) SEM image of 4-probe contacts on the nanowire. (b) Top view of SEM image on the nanowire. (c) 2- and 4-probe IV measurements results. (d) AFM image showing the NW profile.

Furthermore, 50 arrays of nanowires were integrated into field-effect-transistors, each of which consisted of 5 nanowires. Electrical measurements were performed to determine the characteristics of the transistors. Fig. 7 shows the transfer characteristics of 15 FET devices

with back gate. The devices were selected from different zones of the wafer. An SEM representative image of the device is shown in the inset in **Fig.** 7. The length and thickness of each nanowire are 10 μm and 100 nm respectively. The nanowires were lightly doped with boron while the source and drain were heavily doped with phosphorous to form ohmic contacts to Al/Ti contacts. The channel of the NWs was passivated with 20 nm Al_2O_3 deposited by means of atomic layer deposition (ALD). In these measurements, the back gate was swept from -2 V to 10 V and a constant voltage of 0.4 V between source and drain was applied. The increase in current with increasing positive gate voltage for all devices indicates that the devices exhibit n-type characteristics. The devices are normally-off at negative gate bias and the inversion channel is formed at positive voltages higher than the threshold (n-channel enhancement MOSFET). The variation in electrical current could be mainly attributed to the variation in nanowire geometry and defects induced during fabrication and doping processes. The key parameters of NW FETs, including threshold voltage and peak transconductance, are extracted. Standard deviation values of 4.2 ± 0.5 V and 13.2 ± 2.45 μS/μm were found for threshold and peak transconductance respectively. The average value of subthreshold swing and I_{on}/I_{off} ratio were calculated to be 750-900 mV/dec and 10^4-10^5 respectively. The devices exhibit a large value of subthreshold swing which is much higher than the ideal value of ≈ 60 mV/dec at room temperature. Subthreshold swing measures the ability of gate voltage to control the surface potential of the nanowire channel and is given by

$$S = \frac{\partial V_{GS}}{\partial \psi_S}\frac{\partial \psi_S}{\partial log_{10} I_D} = 2.3\frac{KT}{q}\left(1 + \frac{(C_{it} + C_d)}{C_{ox}}\right) \qquad (6)$$

where $\frac{KT}{q}$ is the thermal voltage of $\approx 26\, mV$, C_d, C_{ox} and C_{it} are depletion layer, gate oxide and interface capacitances respectively. Due to thick buried oxide layer (145 nm), the gate oxide capacitance is very small which results in a weak control of gate voltage over channel surface potential. The interface traps could be another reason for the high S. The trap density

of ALD Al_2O_3 on silicon is an order of magnitude higher than the high-quality thermal oxide [55, 56]. The interface traps can be reduced by using high quality thermal oxide or inserting a thin layer of thermally grown oxide between NWs and Al_2O_3 [57]. Subthreshold swing can also be largely reduced by controlling the NWs channel using gate-all-around (GAA) with thin gate oxide. Numerical simulations using carrier transport models such as modified drift-diffusion or Monte Carlo are useful tool for modelling the transport characteristics of nanowire devices and study the influence of different conditions such as the nonuniform distribution of electrostatic potential inside nanowire channel due to corner effect on mobility, and effects such as interface traps, doping, dimension, and gate oxide on the performance of NWFETs characteristics[58, 59]. Such modelling could support the identification of the most optimum conditions of nanowires to be implemented in the next CMOS technology and biosensing platforms[24, 60].

The small device-to-device variability in addition to the good electrical properties of the transistors suggest that these devices are suitable for sensing applications; in particularly for label-free, sensitive and selective detection of DNA and cancer biomarkers where highly uniform electrical properties are required.

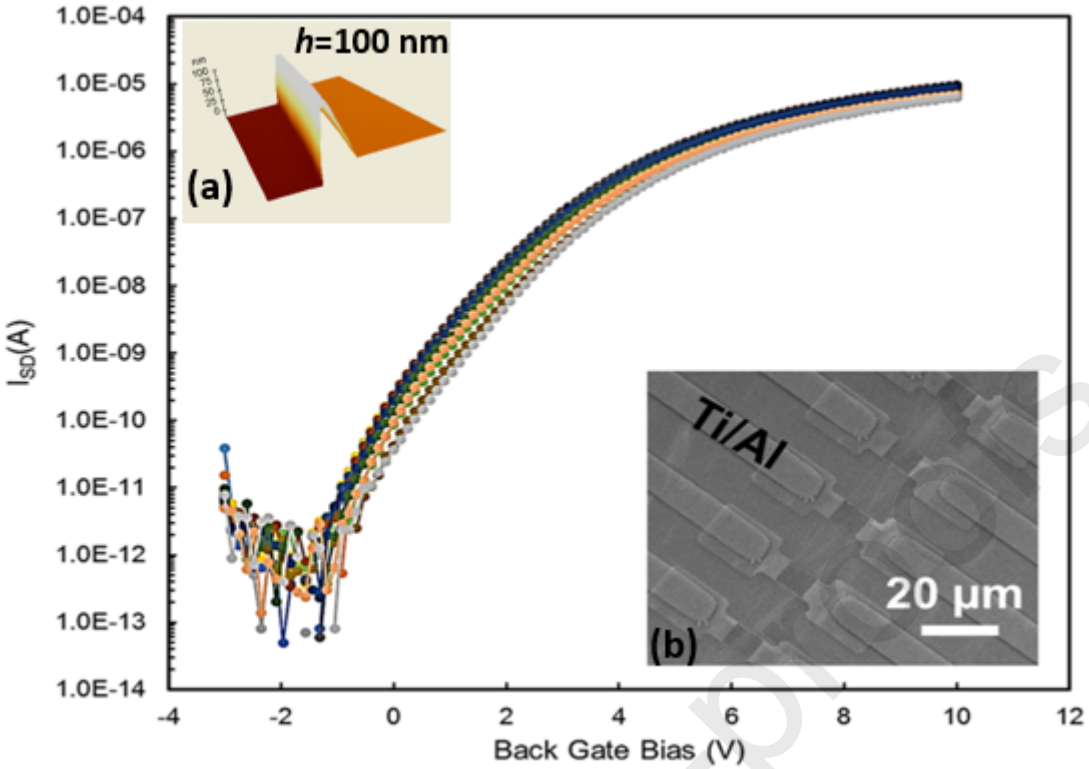


Fig. 7. The transfer characteristics of 15 FET devices with Vsd=0.4V. The devices were selected from different zones of the wafer; the length and thickness of each nanowire are 10 µm and 100 nm respectively. Inset (a): AFM image showing the NW profile. Inset (b): Top view SEM image of a SiNWs array with metal contacts.

3. CONCLUSION

We present a simple fabrication process for silicon nanowire using a top-down approach. This method advances the state-of-the-art technologies by using orientation-dependent oxidation which enables the fabrication of silicon nanowires without the need of multi-processing steps and materials that complex the fabrication process. This can reduce the fabrication cost and improve the controllability of the nanostructure. The small device-to-device variability in addition to the uniformity of the electrical properties of the devices make the nanowire suitable for DNA-sequencing applications and the ability to tune its surface roughness using etching process can make it ideal for thermoelectronic and electronic applications. Furthermore, we extended the technology to produce nanowires via selective etching to allow the formation of a nanowire with its source and drain using a single

fabrication step. By optimizing the nanowire surface roughness during fabrication, we expect the technology to be capable of producing nanowires with thermal conductivity comparable to the value of amorphous silicon without significant reductions in electrical conductivity. This would enable the nanowires to be integrated into highly efficient thermoelectric devices.

4. EXPERIMENTAL SECTION

Silicon nanowires and FETs fabrication: Silicon nanowires were fabricated from lightly doped p-type SOI(100) substrates with various device layer thicknesses and BOX thickness of 145 nm. Some SOI substrates were heavily n-type doped using the SOD process at temperatures between 950-1050 °C to obtain doping levels of 5 X 10^{18} – 8.6 X 10^{18} cm^{-3}. For FET devices, the source and drain (SD) were formed first and heavily n-type doped at a level of 8.6 X 10^{18} cm^{-3}. 20 nm silicon nitride was deposited using r.f magnetron sputtering. A lithography step was then used to define the area of nanowire formation. This was followed by a BHF etching of SiNx. A 25%wt TMAH solution with added 10% IPA at 63 °C for 2 min was utilized to etch the exposed silicon. The silicon nitride was then removed using boiling phosphoric acid. The substrate was then cleaned using Piranha and RCA before being oxidised at 950 °C for 15 min. Oxidation occurs on both <100> and <111> surfaces. The grown thickness on Si(100) was measured to be about 21 nm. Due to that the oxidation rate at the <111> is higher than that at the <100>, the thickness grown on the <111> is thicker compared with the <100>. The approximate thickness on <111> was about 28 nm. The grown silicon oxide layer on <100> was etched using BOE. The etch rate of silicon dioxide in the BHF solution was 1.25 nm/Sec. The exposed silicon on the <100> was then etched using 25%wt TMAH solution with added 10% IPA at 63 °C. The nanowires were then immersed in BHF for 10 seconds in order to remove the sidewall oxide. The nanowires with their S/D contact regions were then patterned using a lithography step to isolate the devices from one another. The isolation patterns were transferred using an RIE step in SF_6/O_2. The

photoresist was then removed by immersing the samples for 10 min in NMP, which was followed by Piranha cleaning for 10 min; then the samples were placed in a plasma Asher for 2 min in order to remove residual organic material. The samples were cleaned twice in Piranha, RCA1, and RCA2 for 5 min each at 80 °C. This was followed by dipping the samples in BHF for 3 seconds in order to remove native oxide and then the samples were placed for 1 min in plasma Asher in order to remove any residual organic layer. Some samples were placed in ALD to coat the nanowires with 20 nm AlOx, while others were placed in the furnace and annealed up to 930 °C in oxygen to obtain an oxide layer of about 15 nm. The area of contact was then patterned and defined using lithography and BHF etching. An ebeam evaporator was used to deposit 60/100 nm of Ti/Al, which was followed by a lift-off step in acetone in order to remove the photoresist. The devices were then placed in RTP and annealed in forming gas at 370 °C for 2 min to improve contact resistance and reduce interface traps.

Electrical measurements: The four-probe technique was used to measure the electrical resistivity of the nanowire. The measurements were performed in air using a Keighley 2400 probe station. An electrical current (-0.5 μA to 0.5 μA) was applied between the two outer probes. Nanowire resistance R_{NW} was measured by dividing the voltage drop between the inner probes over the electrical current. The electrical resistivity was extracted from $\rho_{eff} = R_{NW}\frac{A}{l}$.

AFM measurements: Two types of non-contact AFM tips were used to extract the nanowire profile; very sharp SSS-NCHR tips with a typical tip radius of <5 nm and an aspect ratio of 4:1 at 200 nm; and commercial ACTA tips with a typical tip radius <20 nm and aspect ratio of 1.5-3:1. The increase in nanowire width due to the convolution effect of the AFM tip was

calculated using:

$$w = w_m - 2i = \begin{cases} w_m - 2(\sqrt{R^2 - (R-h)^2} - h\cot\beta), & h_c \le R(1-\cos\beta) \\ w_m - 2(R\cos(90-\beta)) & , \ h_c > R(1-\cos\beta) \end{cases} \quad (8)$$

where w_m is the width measured by AFM. R is the tip radius, h is the height of the nanowire and β is the sidewall angle of silicon, i is the increase in width, and h_c is the critical thickness of the nanowire.

REFERENCES

1 Wang, D., Sheriff, B.A., and Heath, J.R.: 'Complementary symmetry silicon nanowire logic: power-efficient inverters with gain', Small, 2006, 2, (10), pp. 1153-1158

2 Yan, H., Choe, H.S., Nam, S., Hu, Y., Das, S., Klemic, J.F., Ellenbogen, J.C., and Lieber, C.M.: 'Programmable nanowire circuits for nanoprocessors', Nature, 2011, 470, (7333), pp. 240-244

3 Kim, J., Lee, H.-C., Kim, K.-H., Hwang, M.-S., Park, J.-S., Lee, J.M., So, J.-P., Choi, J.-H., Kwon, S.-H., Barrelet, C.J., and Park, H.-G.: 'Photon-triggered nanowire transistors', Nature Nanotechnology, 2017, advance online publication

4 Priolo, F., Gregorkiewicz, T., Galli, M., and Krauss, T.F.: 'Silicon nanostructures for photonics and photovoltaics', Nature Nanotechnology, 2014, 9, (1), pp. 19-32

5 Emre, M., Sahin, C., Mete, G., Bayram, B., Ekmel, O., Rasit, T., and Husnu Emrah, U.: 'Silicon nanowire network metal-semiconductor-metal photodetectors', Applied Physics Letters, 2013, 103, (8), pp. 083114

6 Heiss, M., Fontana, Y., Gustafsson, A., Wüst, G., Magen, C., O'Regan, D.D., Luo, J.W., Ketterer, B., Conesa-Boj, S., Kuhlmann, A.V., Houel, J., Russo-Averchi, E., Morante, J.R., Cantoni, M., Marzari, N., Arbiol, J., Zunger, A., Warburton, R.J., and Fontcuberta i Morral, A.: 'Self-assembled quantum dots in a nanowire system for quantum photonics', Nature Materials 2013, 12, (5), pp. 439-444

7 Zhou, L., Lu, Y., Fu, Y., Ma, H., and Du, C.: 'Design of a hybrid on-chip waveguide with giant backward stimulated Brillouin scattering', Optics Express, 2019, 27, (18), pp. 24953-24971

8 Tsakalakos, L., Balch, J., Fronheiser, J., Korevaar, B.A., Sulima, O., and Rand, J.: 'Silicon nanowire solar cells', Applied Physics Letters, 2007, 91, (23)

9 Boukai, A.I., Bunimovich, Y., Tahir-Kheli, J., Yu, J.-K., Goddard Iii, W.A., and Heath, J.R.: 'Silicon nanowires as efficient thermoelectric materials', Nature, 2008, 451, (7175), pp. 168-171

10 Que, R., Shao, M., Wang, S., Ma, D.D.D., and Lee, S.-T.: 'Silicon nanowires with permanent electrostatic charges for nanogenerators', Nano Letters, 2011, 11, (11), pp. 4870-4873

11 Zhang, A., and Lieber, C.M.: 'Nano-Bioelectronics', Chemical Reviews, 2016, 116, (1), pp. 215-257

12 Zhou, W., Dai, X., and Lieber, C.M.: 'Advances in nanowire bioelectronics', Reports on Progress in Physics, 2017, 80, (1)

13 Tian, B., Cohen-Karni, T., Qing, Q., Duan, X., Xie, P., and Lieber, C.M.: 'Three-dimensional, flexible nanoscale field-effect transistors as localized bioprobes', Science, 2010, 329, (5993), pp. 830-834
14 Cui, Y., Wei, Q., Park, H., and Lieber, C.M.: 'Nanowire nanosensors for highly sensitive and selective detection of biological and chemical species', Science, 2001, 293, (5533), pp. 1289-1292
15 Baraban, L., Ibarlucea, B., Baek, E., and Cuniberti, G.: 'Hybrid Silicon Nanowire Devices and Their Functional Diversity', Adv Sci (Weinh), 2019, 6, (15), pp. 1900522-1900522
16 Tran, D.P., Pham, T.T.T., Wolfrum, B., Offenhäusser, A., and Thierry, B.: 'CMOS-Compatible Silicon Nanowire Field-Effect Transistor Biosensor: Technology Development toward Commercialization', Materials, 2018, 11, (5), pp. 785
17 Qing, Q., Jiang, Z., Xu, L., Gao, R., Mai, L., and Lieber, C.M.: 'Free-standing kinked nanowire transistor probes for targeted intracellular recording in three dimensions', Nature Nanotechnology, 2014, 9, (2), pp. 142-147
18 Li, Z., Chen, Y., Li, X., Kamins, T.I., Nauka, K., and Williams, R.S.: 'Sequence-specific label-free DNA sensors based on silicon nanowires', Nano Letters, 2004, 4, (2), pp. 245-247
19 Yan, R., Park, J.H., Choi, Y., Heo, C.J., Yang, S.M., Lee, L.P., and Yang, P.: 'Nanowire-based single-cell endoscopy', Nature Nanotechnology, 2012, 7, (3), pp. 191-196
20 Chiappini, C., De Rosa, E., Martinez, J.O., Liu, X., Steele, J., Stevens, M.M., and Tasciotti, E.: 'Biodegradable silicon nanoneedles delivering nucleic acids intracellularly induce localized in vivo neovascularization', Nature Materials 2015, 14, (5), pp. 532-539
21 Tian, B., Liu, J., Dvir, T., Jin, L., Tsui, J.H., Qing, Q., Suo, Z., Langer, R., Kohane, D.S., and Lieber, C.M.: 'Macroporous nanowire nanoelectronic scaffolds for synthetic tissues', Nature Materials 2012, 11, (11), pp. 986-994
22 M Nuzaihan, M.N., Hashim, U., Md Arshad, M.K., Rahim Ruslinda, A., Rahman, S.F.A., Fathil, M.F.M., and Ismail, M.H.: 'Top-Down Nanofabrication and Characterization of 20 nm Silicon Nanowires for Biosensing Applications', PLoS One, 2016, 11, (3), pp. e0152318-e0152318
23 Jayakumar, G., Asadollahi, A., Hellström, P.E., Garidis, K., and Östling, M.: 'Silicon nanowires integrated with CMOS circuits for biosensing application', Solid-State Electronics, 2014, 98, pp. 26-31
24 Mirsian, S., Khodadadian, A., Hedayati, M., Manzour-ol-Ajdad, A., Kalantarinejad, R., and Heitzinger, C.: 'A new method for selective functionalization of silicon nanowire sensors and Bayesian inversion for its parameters', Biosensors and Bioelectronics, 2019, 142, pp. 111527
25 Morales, A.M., and Lieber, C.M.: 'A laser ablation method for the synthesis of crystalline semiconductor nanowires', Science, 1998, 279, (5348), pp. 208-211
26 Holmes, J.D., Johnston, K.P., Doty, R.C., and Korgel, B.A.: 'Control of thickness and orientation of solution-grown silicon nanowires', Science, 2000, 287, (5457), pp. 1471-1473
27 Barth, S., Hernandez-Ramirez, F., Holmes, J.D., and Romano-Rodriguez, A.: 'Synthesis and applications of one-dimensional semiconductors', Progress in Materials Science, 2010, 55, (6), pp. 563-627
28 Panciera, F., Chou, Y.C., Reuter, M.C., Zakharov, D., Stach, E.A., Hofmann, S., and Ross, F.M.: 'Synthesis of nanostructures in nanowires using sequential catalyst reactions', Nature Materials 2015, 14, (8), pp. 820-825
29 Hobbs, R.G., Petkov, N., and Holmes, J.D.: 'Semiconductor nanowire fabrication by bottom-up and top-down paradigms', Chemistry of Materials, 2012, 24, (11), pp. 1975-1991
30 Stern, E., Klemic, J.F., Routenberg, D.A., Wyrembak, P.N., Turner-Evans, D.B., Hamilton, A.D., LaVan, D.A., Fahmy, T.M., and Reed, M.A.: 'Label-free immunodetection with CMOS-compatible semiconducting nanowires', Nature, 2007, 445, (7127), pp. 519-522
31 Gao, Z., Agarwal, A., Trigg, A.D., Singh, N., Fang, C., Tung, C.-H., Fan, Y., Buddharaju, K.D., and Kong, J.: 'Silicon nanowire arrays for label-free detection of DNA', Analytical Chemistry, 2007, 79, (9), pp. 3291-3297

32 Hakim, M.M.A., Lombardini, M., Sun, K., Giustiniano, F., Roach, P.L., Davies, D.E., Howarth, P.H., de Planque, M.R.R., Morgan, H., and Ashburn, P.: 'Thin Film Polycrystalline Silicon Nanowire Biosensors', Nano Letters, 2012, 12, (4), pp. 1868-1872
33 Zhou, K., Zhao, Z., Pan, L., and Wang, Z.: 'Silicon nanowire pH sensors fabricated with CMOS compatible sidewall mask technology', Sensors and Actuators B: Chemical, 2019, 279, pp. 111-121
34 Chen, S., Bomer, J.G., Van der Wiel, W.G., Carlen, E.T., and Van Den Berg, A.: 'Top-down fabrication of sub-30 nm monocrystalline silicon nanowires using conventional microfabrication', ACS Nano, 2009, 3, (11), pp. 3485-3492
35 Za'Bah, N.F., Kwa, K.S.K., Bowen, L., Mendis, B., and O'Neill, A.: 'Top-down fabrication of single crystal silicon nanowire using optical lithography', Journal of Applied Physics, 2012, 112, (2)
36 Chen, S., Bomer, J.G., Carlen, E.T., and van den Berg, A.: 'Al2O3/Silicon NanoISFET with Near Ideal Nernstian Response', Nano Letters, 2011, 11, (6), pp. 2334-2341
37 Ramadan, S., Kwa, K., King, P., and O'Neill, A.: 'Reliable fabrication of sub-10 nm silicon nanowires by optical lithography', Nanotechnology, 2016, 27, (42)
38 S.M.Sze: 'Semiconductor devices physics and technology' (Wiley, 2001, 2nd edn. 2001)
39 Massoud, H.Z.: 'Thermal oxidation of silicon in dry oxygen accurate determination of the kinetic rate constants', Journal of the Electrochemical Society, 1985, 132, (7), pp. 1745-1753
40 Massoud, H.Z., and Plummer, J.D.: 'Analytical relationship for the oxidation of silicon in dry oxygen in the thin-film regime', Journal of Applied Physics, 1987, 62, (8), pp. 3416-3423
41 Lewis, E.A., and Irene, E.A.: 'The Effect of surface orientation on silicon oxidation kinetics', Journal of the Electrochemical Society, 1987, 134, (9), pp. 2332-2339
42 Miyawaki, Y., Kondo, Y., Sekine, M., Ishikawa, K., Hayashi, T., Takeda, K., Kondo, H., Yamazaki, A., Ito, A., Matsumoto, H., and Hori, M.: 'Highly selective etching of SiO2 over Si3N 4 and Si in capacitively coupled plasma employing C 5HF7 gas', Japanese Journal of Applied Physics, 2013, 52, (1)
43 Seidel, H., Csepregi, L., Heuberger, A., and Baumgörtel, H.: 'Anisotropic etching of crystalline silicon in alkaline solutions: I. Orientation dependence and behavior of passivation layers', Journal of the Electrochemical Society, 1990, 137, (11), pp. 3612-3626
44 Islam, M., Chen, Y., Wang, S.Y., and Williams, R.: 'Nanowire device with (111) vertical sidewalls and method of fabrication', in Editor (Ed.)^(Eds.): 'Book Nanowire device with (111) vertical sidewalls and method of fabrication' (US 2006/0006463 A1, 2006, edn.), pp.
45 Ahn, M., Heilmann, R.K., and Schattenburg, M.L.: 'Fabrication of ultrahigh aspect ratio freestanding gratings on silicon-on-insulator wafers', Journal of Vacuum Science and Technology B: Microelectronics and Nanometer Structures, 2007, 25, (6), pp. 2593-2597
46 Bunimovich, Y.L., Ge, G., Beverly, K.C., Ries, R.S., Hood, L., and Heath, J.R.: 'Electrochemically programmed, spatially selective biofunctionalization of silicon wires', Langmuir, 2004, 20, (24), pp. 10630-10638
47 Khodadadian, A., Hosseini, K., Manzour-ol-Ajdad, A., Hedayati, M., Kalantarinejad, R., and Heitzinger, C.: 'Optimal design of nanowire field-effect troponin sensors', Computers in Biology and Medicine, 2017, 87, pp. 46-56
48 Park Ii, W., Zheng, G., Jiang, X., Tian, B., and Lieber, C.M.: 'Controlled synthesis of millimeter-long silicon nanowires with uniform electronic properties', Nano Letters, 2008, 8, (9), pp. 3004-3009
49 Zhang, B.C., Wang, H., He, L., Zheng, C.J., Jie, J.S., Lifshitz, Y., Lee, S.T., and Zhang, X.H.: 'Centimeter-long single-crystalline Si nanowires', Nano Letters, 2017, 17, (12), pp. 7323-7329
50 Yeon, J., Lee, Y.J., Yoo, D.E., Yoo, K.J., Kim, J.S., Lee, J., Lee, J.O., Choi, S.J., Yoon, G.W., Lee, D.W., Lee, G.S., Hwang, H.C., and Yoon, J.B.: 'High throughput ultralong (20 cm) nanowire fabrication using a wafer-scale nanograting template', Nano Letters, 2013, 13, (9), pp. 3978-3984
51 Pyun, Y.B., Lee, D.H., Yi, J.S., Kim, Y.J., Jang, J.I., and Park, W.I.: 'Lateral assembly of millimetre-long silicon nanowires for multiple device integration', Journal of Ceramic Processing Research, 2009, 10, (4), pp. 521-525

52 Seo, M.H., Yoo, J.Y., Choi, S.Y., Lee, J.S., Choi, K.W., Jeong, C.K., Lee, K.J., and Yoon, J.B.: 'Versatile transfer of an ultralong and seamless nanowire array crystallized at high temperature for use in high-performance flexible devices', ACS Nano, 2017, 11, (2), pp. 1520-1529
53 Palik, E.D., Gray, H.F., and Greene, R.F.: 'Study of the etch-stop mechanism in silicon', Journal of the Electrochemical Society, 1982, 129, (9), pp. 2051-2059
54 Seidel, H., Csepregi, L., Heuberger, A., and Baumgärtel, H.: 'Anisotropic etching of crystalline silicon in alkaline solutions II. influence of dopants', Journal of the Electrochemical Society, 1990, 137, (11), pp. 3626-3632
55 Garnett, E.C., Tseng, Y.-C., Khanal, D.R., Wu, J., Bokor, J., and Yang, P.: 'Dopant profiling and surface analysis of silicon nanowires using capacitance–voltage measurements', Nature Nanotechnology, 2009, 4, pp. 311
56 Wang, J., Mottaghian, S.S., and Baroughi, M.F.: 'Passivation Properties of Atomic-Layer-Deposited Hafnium and Aluminum Oxides on Si Surfaces', IEEE Transactions on Electron Devices, 2012, 59, (2), pp. 342-348
57 Urresti, J., Arith, F., Olsen, S., Wright, N., and O'Neill, A.: 'Design and Analysis of High Mobility Enhancement-Mode 4H-SiC MOSFETs Using a Thin-SiO2/Al2O3 Gate-Stack', IEEE Transactions on Electron Devices, 2019, 66, (4), pp. 1710-1716
58 Khodadadian, A., Taghizadeh, L., and Heitzinger, C.: 'Three-dimensional optimal multi-level Monte–Carlo approximation of the stochastic drift–diffusion–Poisson system in nanoscale devices', Journal of Computational Electronics, 2018, 17, (1), pp. 76-89
59 Khodadadian, A., and Heitzinger, C.: 'Basis adaptation for the stochastic nonlinear Poisson–Boltzmann equation', Journal of Computational Electronics, 2016, 15, (4), pp. 1393-1406
60 Khodadadian, A., Stadlbauer, B., and Heitzinger, C.: 'Bayesian inversion for nanowire field-effect sensors', Journal of Computational Electronics, 2020, 19, (1), pp. 147-159