

Article

Increased Mobility in 4H-SiC MOSFETs by Means of Hydrogen Annealing

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Abstract: Enhancement-mode 4H-SiC MOSFETs utilising an aluminium oxide (Al₂O₃) dielectric without the requirement for an underlying silicon oxide (SiO₂) layer have been shown to have a field effect mobility of 150 cm²V⁻¹s⁻¹ and a subthreshold swing of 160 mV/dec. The fabricated devices utilised a forming gas (3% H₂ in N₂) anneal immediately prior to the deposition of the Al₂O₃ by Atomic Layer Deposition (ALD). A comparison MOSFET using an identical Al₂O₃ deposition process with a 0.7 nm SiO₂ layer had a field effect mobility of approximately 20 cm²V⁻¹s⁻¹. The hydrogen annealed device had a lower density of interface traps (D_{it}), a lower subthreshold swing, and a significantly reduced hysteresis in the transconductance data than the thin SiO₂ sample. This finding solves the issue of inconsistency of device performance using thin film gate dielectric as an interfacial layer by offering a simple and controllable process.

Keywords: high- κ ; 4H-SiC MOSFET; high mobility; surface reconstruction; surface treatment; trap density



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1. Introduction

The physical-chemical properties of 4H silicon carbide (SiC) are superlative in comparison to conventional semiconductors, such as silicon, gallium nitride or gallium arsenide. However, in comparison to what is seen in the bulk, the carrier mobility in metal oxide semiconductor field effect transistors is substantially lower. This mobility suppression is related to the quality of the interface between the dielectric and the semiconductor substrate with the SiC/SiO₂ interface having much lower quality than that found in silicon based CMOS. Electrically active defects located close to this interface result in poor electron mobilities in nMOS devices that are typically below 20 cm²V⁻¹s⁻¹ [1]. Often, the gate dielectric is fabricated using a high temperature dry oxidation process; however, this is known to increase the density of ON1/ON2 defects in the region of the device where the channel forms [2].

A range of post-oxidation processes have been demonstrated to increase mobility, often using nitrogen [3,4], phosphorous [5] or boron-containing species [6]. This technique offers an improvement in the channel mobility to approximately 180 cm²V⁻¹s⁻¹ [7]. However, this can be accompanied by a decrease in the threshold voltage, V_{TH} and a significant degradation in the high temperature stability of the dielectric [8,9]. An alternative approach as a replacement for thermally grown SiO₂ is to use high- κ materials as dielectrics, notably Al₂O₃. Results in the literature report channel mobilities of 300 cm²V⁻¹s⁻¹ for 4H-SiC MOSFETs employing an Al₂O₃ layer as a gate dielectric with SiO₂ as an interfacial layer [10,11]. The data suggest that an interfacial layer with a thickness of over 2 nm degrades the quality of the SiC-SiO₂ interface, resulting in a lower channel mobility. Arith et al. [12] reported that an underlying silicon dioxide layer with a thickness of 0.7 nm resulted in an intrinsic mobility of 125 cm²V⁻¹s⁻¹, in comparison to a 29 nm SiO₂ layer, which had a mobility

of $7 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$. Devices with the thin oxide layer also had a significantly improved sub-threshold slope (130 mV/dec in comparison to 550 mV/dec). Peak field effect mobility of $106 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ using a gate dielectric of thin nitrided SiO_2 and Al_2O_3 was reported by Lichtenwalner et al. [13]. Hydrogen plasma treatment was found to be effective at decreasing the interface state density at the Al_2O_3 -SiC interface [14,15], resulting in a peak field effect of mobility of $57 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ with a density of interface traps of 1.7×10^{12} at $E_C - E = 0.2 \text{ eV}$ using the $C-\psi$ technique.

Nevertheless, one issue with short oxidation times is the inability to produce a uniform thin layer. We have previously reported that post-oxide annealing at 1050°C in forming gas significantly improved the stability of the flatband voltage and reduced the interface state density. However, the leakage current and oxide breakdown of the Al_2O_3 degraded due to crystallization of the film [16].

Here we report SiC MOSFETs using an Al_2O_3 dielectric without the inclusion of an underlying SiO_2 layer that demonstrate a peak field effect mobility of $150 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$. The high peak mobility can be attributed to the inclusion of a forming gas anneal performed immediately prior to the atomic layer deposition of the dielectric. We attribute this increase in channel mobility to the electrically charged defects at the SiC surface being passivated.

2. Materials and Methods

4H-SiC, with an epilayer approximately $1 \mu\text{m}$ thick with an Aluminium concentration of $2 \times 10^{15} \text{ cm}^{-3}$ (4° off-axis, Si-face, and an n^+ (substrate)/ p^+/p^- wafer supplied by Cree or Wolfspeed) were used as a starting material for the fabrication of the MOSFETs. Multiple nitrogen implantations with a cumulative dose of $9.8 \times 10^{14} \text{ cm}^{-2}$ were used to form the source and drain regions at room temperature. A carbon capping procedure was used to anneal the implants in an Argon environment at 1700°C for 10 min [16]. The carbon cap was removed in a low energy oxygen plasma. After surface cleaning in buffered HF (hydrofluoric acid), the ohmic contacts for the source and drain implants were formed by depositing titanium (5 nm) and nickel (100 nm) metal films. These contacts were then annealed at 1050°C in forming gas, (3% H_2 in N_2) to form nickel silicide [17,18]. Trimethylaluminum (TMA) and water (H_2O) were used to produce a layer of Al_2O_3 with a thickness of 40 nm by performing atomic layer deposition at 200°C in a chamber pressure of 600 mTorr. The Al_2O_3 layer was etched to create the source and drain contacts. Then, tungsten was physically vapor-deposited to form the gate contacts, which were then shaped using a lift-off technique. The thickness of all materials was also confirmed using Atomic Force Microscopy (AFM). The alignment process of each step in the fabrication of 4H-SiC MOSFET was performed using Karl Suss MJB-3 mask aligner with a maximum resolution of $1 \mu\text{m}$. Figure 1 shows the summarized process used in the fabrication of 4H-SiC MOSFET and an image of the final 4H-SiC MOSFET taken under an optical microscope.

To provide a direct comparison of the transistor performance, control samples with a traditional SiO_2 layer under the Al_2O_3 layer were also fabricated. Based on the process reported previously [11], after Ohmic contact formation, a thin oxide layer was grown at 600°C in dry oxygen for 3 min using a Rapid Thermal Process. This resulted in an oxide layer thickness of 0.7 nm, which was confirmed by X-Ray Photoelectron Spectroscopy using monochromatic $\text{Al K}\alpha$. The thickness of thin film SiO_2 was estimated by areal ratio with a binding energy of 102.9 eV (SiO_2 peak) [19]. To prevent inadvertent SiO_2 formation at the SiC/ Al_2O_3 interface, neither post-oxide annealing nor post-metalization annealing were carried out after Al_2O_3 deposition. The manufactured MOSFETs have $100 \mu\text{m}$ in width and channel lengths (L) ranging from 2 to $20 \mu\text{m}$.

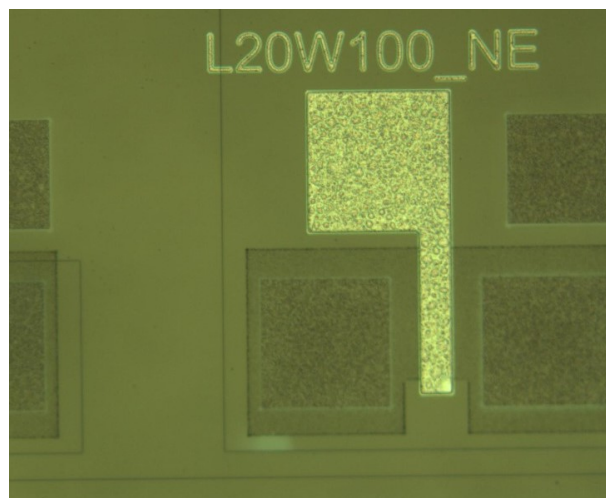
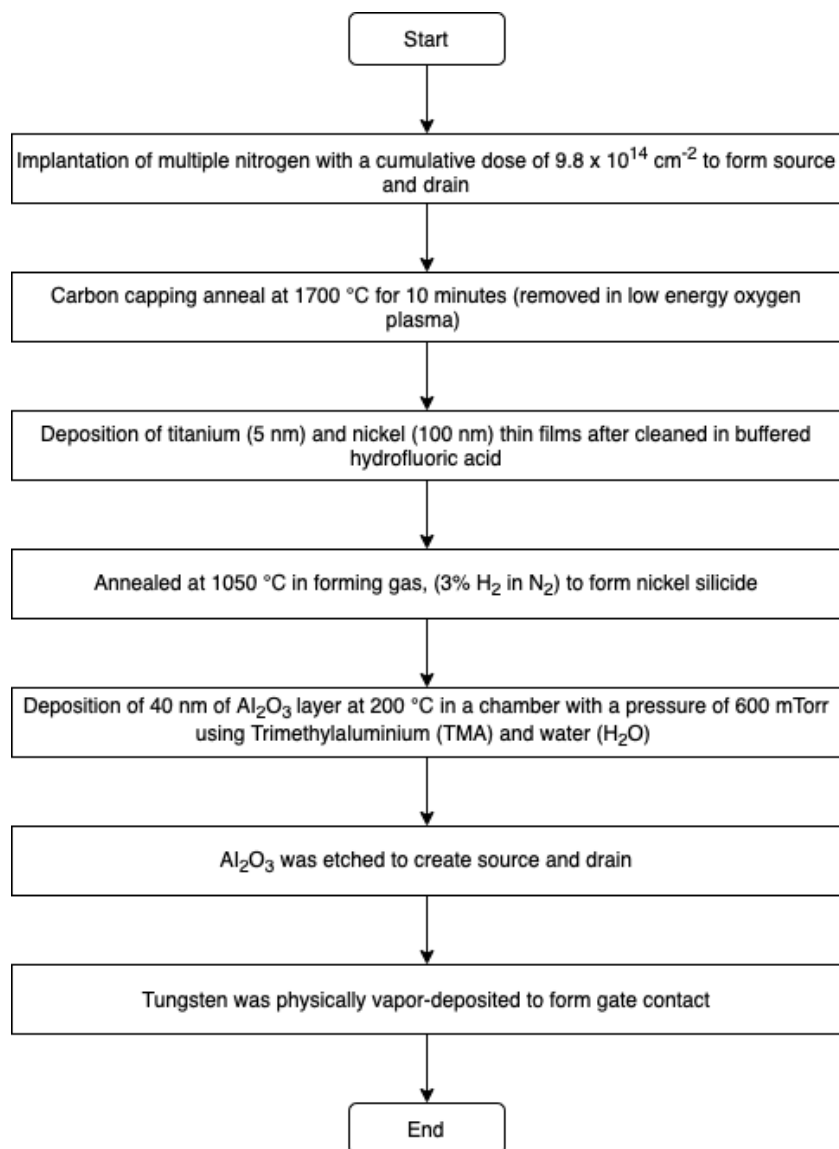


Figure 1. Summary of the important steps for the fabrication process of 4H-SiC MOSFET and image of the final 4H-SiC MOSFET with Gate Length, L and Gate Width, W of 20 μm and 100 μm taken under an optical microscope.

Capacitance–voltage (C – V), quasi-static and current–voltage (I – V) characteristics of MOS capacitors and MOSFETs were performed using a Keithley 4200 semiconductor device parameter analyzer in conjunction with a Cascade Microtech probing station (Model Summit 12,000 BAP) supported on an active air anti-vibration table at room temperature under dark conditions. The density of interface traps (D_{it}) for the MOS capacitor was extracted by using the C – ψ method, which is the most accurate method to estimate the density of interface states, derived from quasi-static capacitance–voltage (C – V) measurements. The interface state density extracted using C – ψ_s is calculated using the difference between the low frequency (quasi-static) data, where all traps can respond and $C_{D,theory}$ ($C_{it} = 0$) as given below:

$$D_{it} = \frac{(C_D + C_{it})_{QS} - (C_D + C_{it})_{theory}}{Ae^2} \quad (1)$$

$(C_D + C_{it})_{QS}$ is $C_D + C_{it}$ extracted from quasi-static measurements, and $(C_D)_{theory}$ is obtained from theoretical calculation of semiconductor capacitance.

3. Results

The results in Figure 2 depict the drain current (I_D) as a function of gate voltage (V_{GS}) for both MOSFETs obtained at room temperature with $V_{DS} = 100$ mV. The threshold voltages, V_{TH} of 2.5 V and 5.5 V were obtained for the samples annealed in forming gas and thin oxide, respectively. Plots of I_D vs. V_{GS} are shown in the subthreshold area, where $10^{-10} > I_D > 10^{-9}$. These were used to determine the values for the subthreshold slope, S . Samples annealed in forming gas show excellent subthreshold slope of 160 mV/dec, in comparison to a thin oxide sample with 500 mV/dec. The hysteresis in the drain current in the subthreshold region when swept forward and backward is negligible for the forming gas sample, in comparison to that obtained for the thin oxide samples. The origin of the negligible hysteresis in the subthreshold region is related to the reduced density of interface traps at the SiC/Al₂O₃ as a result of the H passivation [20]. The hysteresis under strong inversion for both samples is due to defects in the bulk of the Al₂O₃ gate dielectric as the same gate dielectric is present in both devices. In 4H-SiC MOSFETs, the interface state density is the main problem that deteriorates the channel mobility and causes the instability of the flatband voltage. The huge difference between both devices is in the preparation of the dielectric materials that greatly impact the device performance, such as field effect mobility, threshold voltage, and subthreshold slope. From the data in Figure 2, it was found that incorporating a new step prior to the deposition of dielectric material can reduce the interface state density, thus increasing channel mobility.

The data in Figure 3 show a typical $I_D - V_{DS}$ characteristic at $V_G - V_{TH} = 3$ to $V_G - V_{TH} = 6$ V for the forming gas annealed sample and $V_G - V_{TH} = 7$ V for the device with the thin oxide layer. The forming gas sample exhibits a six-fold enhancement in drain current at $V_G - V_{TH} = 4$ V than that observed in the thin oxide sample operating with a gate bias of $V_G - V_{TH} = 7$ V. The data in Figure 4 show that the forming gas annealing process reduces the interface state density by a factor of three for energies between 0.2 and 0.5 eV below the conduction band edge, by means of hydrogen atom termination of Si and C atoms dangling bonds [21]. The density of interface states was extracted using the C – ψ technique at room temperature. This technique allows the detection of very fast states, resulting in a more accurate D_{it} profile in comparison to both the High-Low and Terman methods [21]. The D_{it} at $E_C - E = 0.2$ eV is below $1 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$, which is the lowest value reported for measurements on SiC using the C – ψ technique [22].

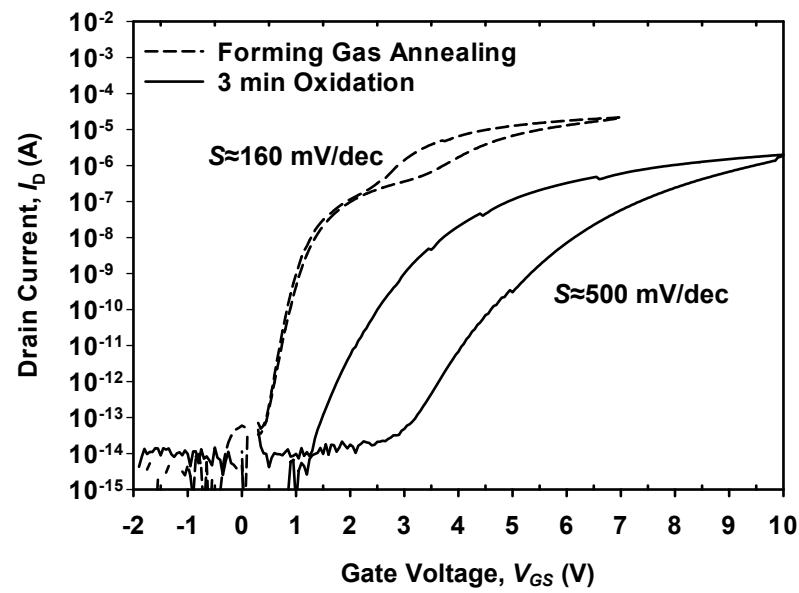


Figure 2. Semi-Log $I_D - V_G$ characteristics with $V_{DS} = 100$ mV for MOSFETs with Gate Length, L and Gate Width, W of $20\ \mu\text{m}$ and $100\ \mu\text{m}$, respectively.

The field effect mobility for both MOSFET architectures is displayed in the data in Figure 5. The field effect mobility, μ_{EFF} , of carriers in a MOSFET channel can be defined as:

$$\mu_{\text{EFF}} = \frac{L}{WC_{\text{OX}}V_{DS}} \left(\frac{dI_{DS}}{dV_{GS}} \right) \quad (2)$$

where I_{DS} , V_{DS} , and V_{GS} are the drain current, drain voltage and gate voltage respectively. The MOSFET transconductance is defined as:

$$g_m = \frac{dI_{DS}}{dV_{GS}} \quad (3)$$

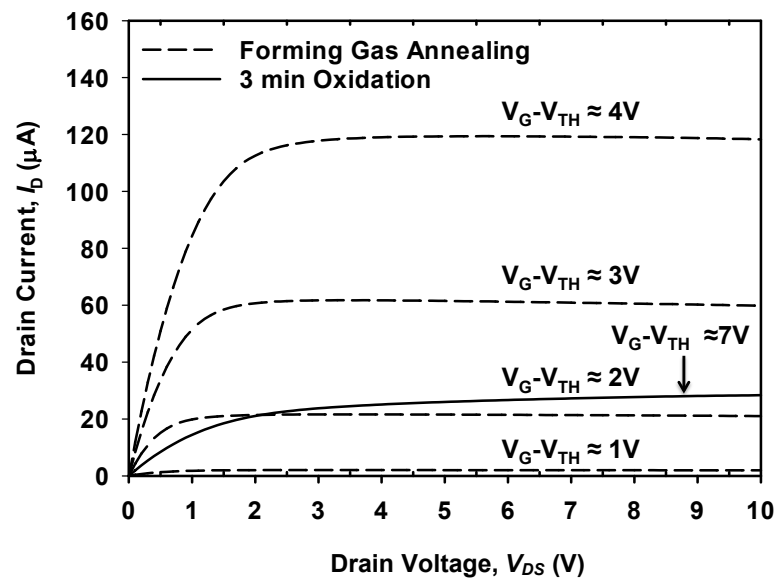


Figure 3. $I_D - V_{DS}$ characteristics with $V_G - V_{TH} = 3$ to 6 V for MOSFETs with gate length, L , and gate width, W , of $20\ \mu\text{m}$ and $100\ \mu\text{m}$, respectively.

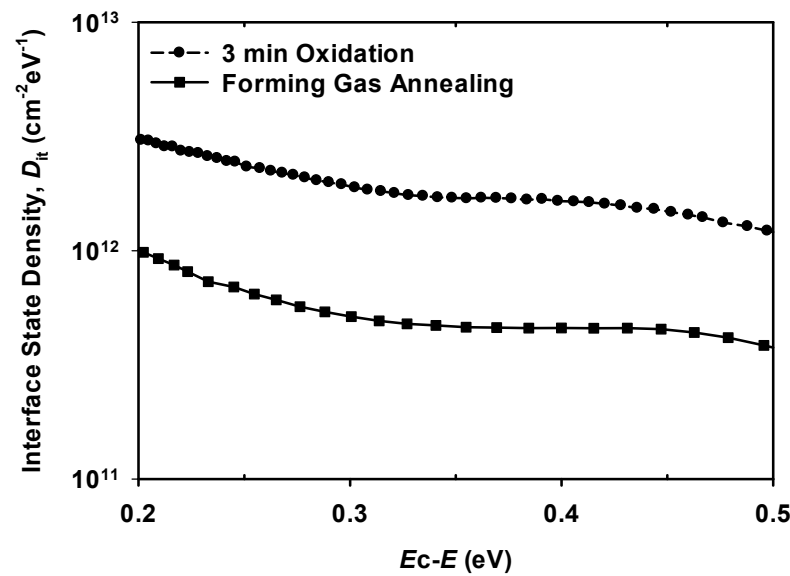


Figure 4. Interface state density, D_{it} , as a function of energy for n-type MOS capacitor at room temperature extracted using the $C-\psi$ technique. E_C is conduction band edge, E is interface state energy, and $E_C - E$ is the energy position or energy range in the band gap.

The forming gas sample exhibits a massive improvement in the field effect mobility, with a peak field effect mobility of $150 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, while retaining a positive threshold voltage of 2.5 V. The thin oxide sample, in comparison, exhibits a maximal field effect mobility of around $20 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$. The improvement in the field effect mobility may be linked to the suppression of carbon cluster (ON1/ON2 defects) formation in the near-interface region during the hydrogen passivation process [23]. It has also been shown that hydrogen passivation lessens stress relaxation and Coulombic scattering at the SiC–dielectric contact [24,25]. Our findings are in strong accord with those of Okuda et al. [26], who found that H_2 annealing at temperatures over 750°C increases the carrier lifetime in p-type 4H-SiC epi-layers. It is also believed that hydrogen etching of the SiC surface occurred during the forming gas annealing, resulting in the reconstruction of the SiC surface suitable prior to Al_2O_3 deposition [27,28].

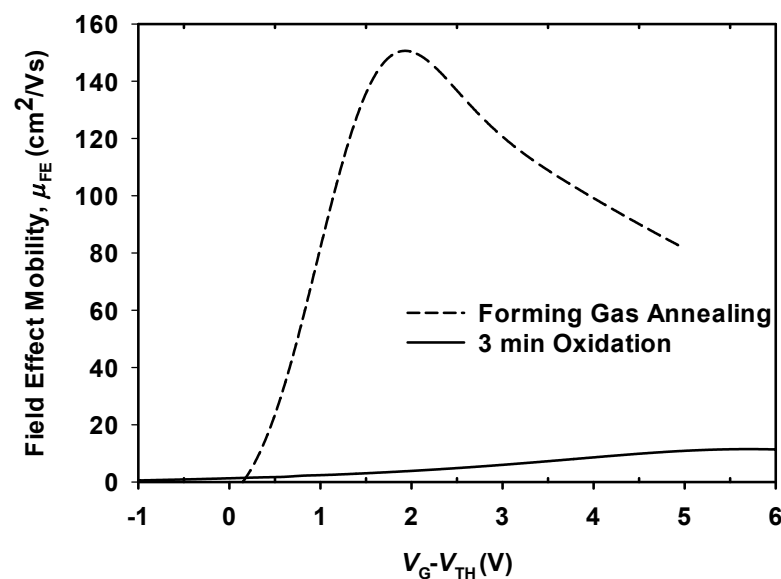


Figure 5. Field effect mobility for n-channel 4H-SiC MOSFET fabricated using Al_2O_3 with a gate length $L = 20 \mu\text{m}$ and gate width $W = 100 \mu\text{m}$. The same figure also displays the field effect mobility for MOSFETs with thin oxide.

The mobility is limited by several scattering mechanisms, including Coulomb scattering, phonon scattering, surface roughness scattering, and bulk mobility scattering that are pertinent to MOSFETs operating at different electric fields and temperatures. The sum of each reciprocal mobility component is proportional to the reciprocal of total mobility as given by Matthiessen's rule:

$$\frac{1}{\mu_T} = \frac{1}{\mu_C} + \frac{1}{\mu_{SR}} + \frac{1}{\mu_{SP}} + \frac{1}{\mu_B} \quad (4)$$

where μ_C is Coulomb mobility, μ_{SR} is surface roughness mobility, μ_{SP} is phonon mobility, and μ_B is bulk mobility. For 4H-SiC MOSFET, the bulk mobility scattering has a negligible influence on the field effect mobility because other scattering mechanisms are dominant at the oxide–semiconductor interface. Figure 6 shows the contribution of the three dominant scattering mechanisms that limit the field effect mobility. Under low electric fields, Coulomb scattering from the fixed and trapped charge at the SiC–SiO₂ interface is the most prominent. Surface phonon scattering is the deflection of electrons by acoustic phonons at the semiconductor surface. However, this is not the limiting factor for field effect mobility in 4H-SiC MOSFETs. The existence of step bunching on the surface of off angle 4H-SiC wafers makes the SiC–SiO₂ interface very complex and rough, which results in a significant degradation of the field effect's mobility under high electric fields, limited by surface roughness scattering. Electrons flowing in the channel (near or at the SiC–SiO₂ interface) experience more surface roughness scattering at high electric fields (perpendicular to the surface) because electrons are strongly attracted to the SiC surface or interface as the electric field increases. Therefore, the field effect mobility is determined by the interplay of several mechanisms that are typically affected by device processing.

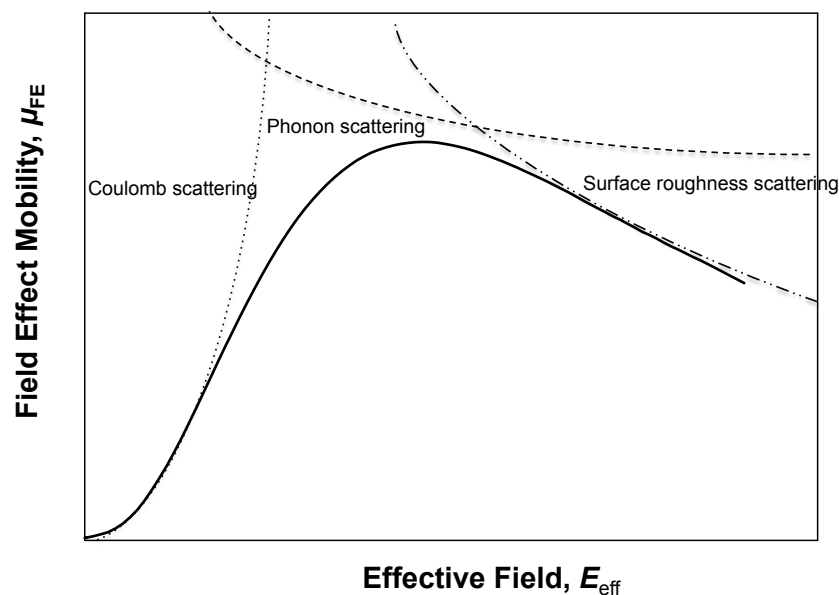


Figure 6. Scattering mechanisms that affect the field effect mobility in MOSFETs.

The I_D – V_G characteristics were repeatedly determined for gate voltages between $V_G = -2$ and $V_G = 7$ V to determine the stability of the threshold voltage. The data in Figure 7 show the shift in threshold voltage for both samples as a function of the number of measurements. The threshold voltage for both samples were extracted using the linear extrapolation method. The threshold voltage for the forming gas sample is consistent for each measurement, with a variation below 0.2 V; however, the data for the thin oxide sample show a significant shift in threshold voltage from ~ 6 V to ~ 8 V for the first and second measurements. The observed shift reduces on the third and fourth measurement because the interface traps become occupied during the first and second measurements.

This effect is not observed in the forming gas-annealed sample, consistent with a lower density of trapping states in at the SiC–dielectric interface.

The origin of hysteresis can be in the bulk oxide or at the interfacial layer. For a sample with Al_2O_3 as a dielectric, the hysteresis can be due to the trapping and de-trapping in the bulk oxide itself during forward and reverse bias. On the other hand, the hysteresis for the sample with a 3 min oxidation is huge compared to the FGA sample, possibly due to the high density of the interface trap in addition to the trapping and de-trapping in the Al_2O_3 gate dielectric. Since the interface trap density is high, it will also enhance the electron trapping and oxide degradation that results in low channel mobility.

The findings in Figure 8 demonstrate how the retrieved peak field effect mobility varies with gate length, supporting the dependency between the two MOSFETs. This trend is expected as the overlap capacitance (gate to source, C_{GS} , and gate to drain, C_{GD}) becomes less important for physically larger devices. In this work, an overlap length of 2 μm is applied on each side of the gate metal. Minimizing parasitic capacitances in the device structure is important because it leads to enhanced electrical performance for high-frequency applications.

The data presented show MOSFETs with high field effect mobility and positive threshold voltage realised by the use of high temperature annealing in hydrogen prior to Al_2O_3 dielectric deposition. Tungsten, with a high work function (~ 5 eV), is a good choice of metal to impede the reduction in threshold voltage with increasing peak mobility [29].

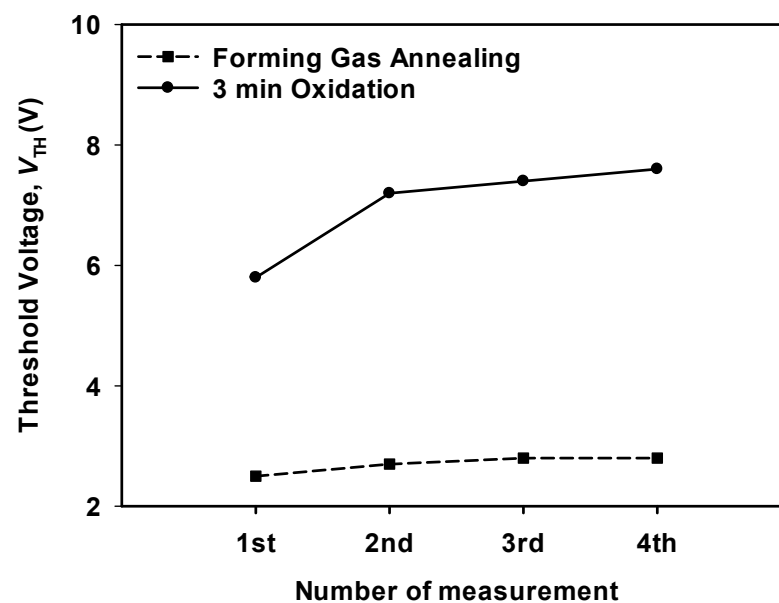


Figure 7. Shift in V_{TH} for both samples as a function of the number of measurements. (The measurement were repeated on the same samples.) The V_{TH} for both samples were extracted using the linear extrapolation method. After the fourth measurement, both samples exhibited negligible shifts or changes.

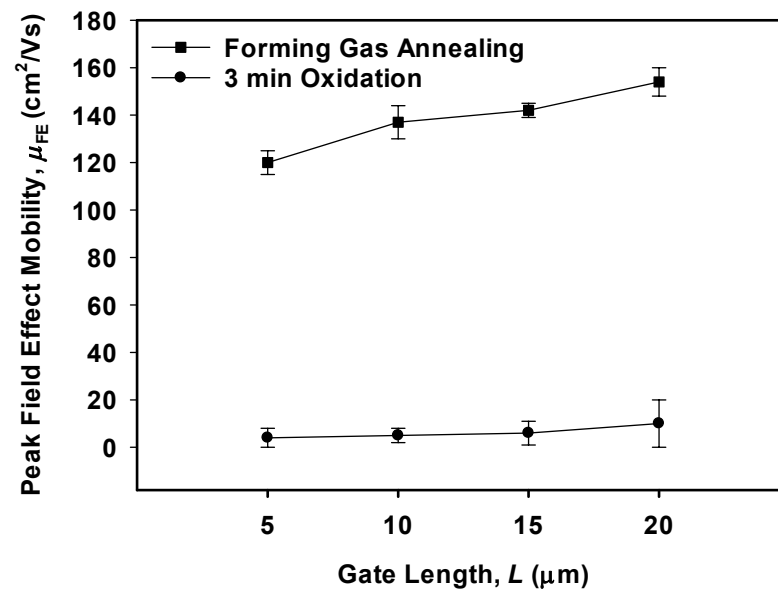


Figure 8. Peak field effect mobility of different MOSFETs as a function of gate length, L (5, 10, 15, and 20 μm), with $W = 100 \mu\text{m}$.

4. Conclusions

We report the characteristics of 4H-SiC MOSFETs with different surface treatments on an p-type 4H-SiC epitaxial layer using Al_2O_3 as a gate dielectric. The annealing of the SiC surface as a pre-treatment immediately prior to Al_2O_3 deposition was useful in decreasing the interfacial defect density. Thus, in this work, a D_{it} of $1 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ at $E_C - E = 0.2 \text{ eV}$ and field effect mobility of $150 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ were achieved.

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

MOSFET	Metal Oxide Semiconductor Field Effect Transistor
Al ₂ O ₃	Aluminium Oxide
SiC	Silicon Carbide
SiO ₂	Silicon Oxide
I _D	Drain Current
ALD	Atomic Layer Deposition
MOS	Metal Oxide Semiconductor
C–V	Capacitive Voltage
TMA	Trimethylaluminum
HF	Hydrofluoric
AFM	Atomic Force Microscopy
D _{it}	Interface traps density

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