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# **Controller-Based Energy-Aware Wireless Sensor Network Routing Using Quantum Algorithms**

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**ABSTRACT** Energy-efficient routing in wireless sensor networks has attracted attention from researchers in both academia and industry, most recently motivated by the opportunity to use software-defined networkinspired approaches. These problems are NP-hard, with algorithms needing computation time that scales faster than polynomials in the problem size. Consequently, heuristic algorithms are used in practice, which are unable to guarantee optimally. In this article, we show proof-of-principle for the use of a quantum annealing processor instead of a classical processor, to find optimal or nearly optimal solutions very quickly. Our preliminary results for small networks show that this approach using quantum computing has great promise and may open the door for other significant improvements in the efficacy of network algorithms.

**INDEX TERMS** Next generation networking, routing protocols, wireless sensor network, quantum algorithms.

## **I. INTRODUCTION**

Wireless sensor and ad-hoc networks have attracted much attention in research recently, including the Internet of Things (IoT), embedded systems, and autonomous vehicles. The network structure is usually nonhierarchical and autonomously forms a network facilitated by ad-hoc mobile network protocols. In order to achieve resource utilization efficiency in terms of energy consumption, the concept of a network controller device is seen as appropriate [1], influenced by software-defined networking (SDN) [2]. Using SDN at the network edge with devices that are resource-constrained, wireless, and perhaps mobile raises many challenges but presents a great opportunity to use algorithms for routing and other tasks that can take advantage of centralized computation. In our case, the network controller uses a hybrid of classical and quantum algorithms to minimize the energy consumption and also meet the expected average data rate metrics for the network. The controller runs the computation of the optimal path set for a given set of packet streams

at various inception nodes and assigns the path to each stream.

## *A. BACKGROUND*

Quantum computers use quantum mechanical phenomena of superposition, entanglement, and tunneling to perform computation. They operate in the tensor-product Hilbert spaces and can perform computations in exponentially large dimensions to solve complex problems. Quantum algorithms are known to outperform classical algorithms on many challenging problems such as integer factoring [3], search [4], Fourier transform [5], and training machine learning models [6], [7]. Several quantum and quantum-classical hybrid algorithms have also been proposed to address different types of optimization problems. These include, for instance, the Harrow–Hassidim–Lloyd algorithm for least square fitting [8], quantum semidefinite programming

algorithm for semidefinite programming [9], quantum approximate optimization algorithm for combinatorial optimization [10], adiabatic quantum computing for quadratic programming as well as NP-complete problems [11], and variational quantum eigensolver for nonlinear optimization [12].

In this work, we focus on the D-Wave adiabatic quantum computers, which were designed to approximately solve the quadratic unconstrained binary optimization (QUBO) problem, which is NP-hard. As such, these machines have been used to address many NP-hard problems in the literature in purely quantum as well as quantum-classical hybrid approaches. D-Wave machines have been used to address the graph partitioning [13], [14] and graph coloring problems [15]. Warren [16] addresses the traveling salesman problem using the D-Wave quantum annealing computers. Date et al. [17] propose a quantum-classical hybrid algorithm to train restricted Boltzmann machines and deep belief networks. One of the biggest challenges pertaining to adiabatic quantum computing is the embedding of a given QUBO problem onto the hardware of the quantum computer [18]. In this work, we first convert the energy-efficient network routing problem as a QUBO problem and then leverage two D-Wave processors, both 2000Q and Advantage to solve it, we find that both can provide faster (in terms of raw processing time) solutions than state-of-the-art-classical solvers for some small network problems. While these problems are too small to directly show a quantum advantage, these are still hopeful signs in terms of the ability of these devices to find a "good solution quickly."

# *B. NOVELTY AND CONTRIBUTION*

This work has made three breakthroughs in the field of quantum computing, being the first to do the following:

- 1) engage the computation power of a quantum processor unit (QPU) to network design, in this instance focused on energy management;
- 2) compare the 2000Q and Advantage\_System1.1 processors in solving a network design problem;
- 3) apply the Domain Wall Encoding scheme [19] for QPU in a practical engineering problem.

The work demonstrates the merits of applying a quantum annealing QPU in network design but also provides a simulation platform that can be used by other researchers for future QPU-facilitated design and test problems.

We start by discussing the current state of the art and related work, which we build upon. We then discuss the general formulation of the problem by conventional methods and how to translate it to the recently proposed domain-wall encoding and propose an algorithm for mapping the problem. We then describe the details of our experimental methods and report our results. Finally, we discuss the consequences of the results and the longer-term outlook.

## **II. RELATED WORK**

Energy consumption in network routing is caused by neighborhood discovery, communication, and computation. Energy-efficient routing with quality-of-service (QoS) guarantee in different applications or diverse wireless sensor networks (WSNs) can be viewed as an interesting area for future investigation [1]. Unbalanced energy consumption among the nodes causes network partition and node failures, where transmission from some nodes to the sink becomes blocked [20]. Energy efficiency can be improved at various layers of the communication protocol stack of WSN. For hardware-related energy efficiency, topics have been focusing on lower power electronics, power-off mode, and energy-efficient modulation. For network-layer-related energy, Lee et al. [21] proposed the routing schemes in consideration of both the link quality and the residual energy level. It discusses the mechanism for forwarding route requesting packets by calculation of the probability to forward or not by taking into account the link quality and residual energy level two metrics. The scheme is evaluated against the plain Adhoc On-Demand Distance Vector (AODV) algorithm. Due to the heuristic nature of the algorithm, it is not assured to be optimal. In, Liu et al. [22] presented a simple and highly efficient strategy to form the energy-aware path from source to sink node in WSN. When the event path and query path intersects, an anchor node is discovered or it can be found within the candidate region around the intersection point. It solves the spiral problem in rumor routing by keeping the event and query paths as straight as possible and proves to outperform rumor routing and achieves higher successful path discovery ratios and lower hop counts and saves more energy. The algorithm limitation is that it guarantees the shortest path routing but without assuring energy savings. In, Zhao et al.[23] solve the optimal routing path issue of WSN by formulating the problem using the optimal path set, which consists of a possible combination of nodes that falls within the optimal transmission range of the source node and have minimum cost value corresponding to the cost function with energy and loss rate as the input parameters. The author first derives the metrics to evaluate the cost function and then proposes a brute force scheme to scan all the possible combinations of nodes to determine the optimal path set. Experiments have shown that the scheme can provide robust connectivity and prolong the lifetime of the network compared with benchmarks across different scenarios. Yao et al. [24] solve the energy efficiency problem within WSN while not violating QoS metrics by formulating the problem in the framework of the open vehicle routing problem in operation research. As the open vehicle routing (OVR) problem proves to be NP-hard, the authors subsequently proposed two different heuristic algorithms to approximate the design outcome. The results demonstrated that it outperforms baseline protocols in achieving elongation of the network lifetime operating within the expected delivery latency bounds. Due to complexity, all today's network routing solutions for WSNs rely on heuristic algorithms.

#### **TABLE I List of Symbols Used in This Article**



In this work, the computation for the optimal set of paths is achieved by formulating the problem as a QUBO problem that can be easily mapped to the Ising model. QUBO has been used to solve network routing and similar optimization problems in the literature [25], [26], [27] and it is just one of the possible formulation selected to demonstrate the power of quantum. The optimization can be solved by applying the quantum annealing technique used in physics to attain the ground state of the final state of the Hamiltonian system specified by the Ising model coefficients. We are using the QPU by D-Wave Systems, Inc., in this work.

#### **III. PROBLEM FORMULATION**

For this problem, symbols used are listed in Table. 1. We assume the network controller monitors the data traffic at a regular basis  $\Delta t$ , starting from  $t_{org} = 0$ . Multiple source nodes exist in the network  $s_i$  while only one destination  $d$ , i.e., the WSN sink node is present. For each packet stream  $p_j$  with average data rate  $r_j$ , there is an associated pair of the destination node and the source node  $(s_{i,j}, d)$ . It describes the packet stream  $p_j$  routed to the sink node  $d$  from source node *si*. Let the number of available routes to choose be a constant number *K* for all the packet streams, an approach similar to that in [28]. For each route route  $i, k$ , there exists a set of edges edge*<sup>m</sup>* that connect with each other to compose the route. route  $_{i,k}$  describes the *k*th route for packet stream *j*.



**FIGURE 1. Small network example.**

*K* is the maximum number of routes available for each packet stream to be routed from its source node to the destination node.

At a given moment  $t' \in \{n\Delta t, (n+1)\Delta t\}$ , let there be *L* packet streams. Consequently, there would be a binary set *xi* of size  $K * L$  for  $x_i$  that represents the *i* (mod *K*)th optional route for path  $n = \lfloor \frac{i}{k} \rfloor$ .  $x_i \in \{0, 1\}$ . The edges associated with  $x_i$  is edge<sub>*i*, *j*</sub>. For each edge *j*, the length is  $l_j$ .

**TABLE II Parameter Value**

Name	Value
$E_{\text{elec}}$	50 nJ/b
$\epsilon_{mp}$	$0.0013 \frac{pj}{hit} / m^4$
$\epsilon_{fs}$	$10 \frac{pj}{bit} / m^2$
do	$\frac{\epsilon_{fs}}{\epsilon_{mn}} = 87.7058$

## *A. EXAMPLE ILLUSTRATION*

There are five source nodes and one sink in Fig. 1. Suppose only node 1 and node 3 are transmitting at the moment of *t*, each with an average data rate of *r*<sup>1</sup> and *r*3. For node 1 to sink 6, there are two paths  $p_{1,1}$  and  $p_{1,2}$ . For node 3 to sink 6, there are also two paths  $p_{3,1}$  and  $p_{3,2}$ . From the graph, we realize that  $p_{1,1} = [\text{edg}_1, \text{edg}_2], p_{1,2} =$  $[$ edg<sub>1</sub>, edg<sub>3</sub>, edg<sub>5</sub>, edg<sub>6</sub>],  $p_{3,1}$  =  $[$ edg<sub>3</sub>, edg<sub>2</sub>], and  $p_{3,2}$  =  $[$ edg<sub>5</sub>, edg<sub>6</sub> $]$ .edg<sub>*i*</sub> is the *i*<sup>th</sup> edge. Set  $\overline{X_1} = [xp_{1,1}, xp_{1,2}]$  and  $\bar{X}_2 = [xp_{3,1}, xp_{3,2}],$  where  $xp_{i,j} \in \{0, 1\}$  indicates whether the *j*th path for traffic stream starting from node *i* is selected or not. For each path, we assume the energy consumption per interval  $\Delta t$  is  $e_{i,j} = \sum_{\text{edge}_k} e_{i,j,k}$ , where  $e_{i,j,k}$  is the energy consumption at *k*th edge with source number *i* whose path index is *j*.

The overall energy consumption is  $E = xp_{1,1}e_{1,1} +$  $xp_{1,2}e_{1,2} + xp_{3,1}e_{3,1} + xp_{3,2}e_{3,2}$ , where  $xp_{1,1} + xp_{1,2} = 1$ and  $xp_{3,1} + xp_{3,2} = 1$ .

The conditions indicate for each traffic stream, only one path can be selected.

There exists another condition, which is the edge load should not exceed the maximum capacity. Assume for the edges within the network, the maximum capacity is uniform as *C*max. As a simple combinatorial problem, it is easy to deduce that there will be four combinations. Take one combination  $[X_{1,1}^-, X_{3,1}^-,]$ , for example, there are three edges in use. For edg<sub>1</sub> and edg<sub>3</sub>, the edge load is  $r_1 \leq C_{\text{max}}$  and  $r_3 \leq C_{\text{max}}$ , respectively. For edg<sub>2</sub>, the edge load is  $r_1 + r_3 \leq C_{\text{max}}$ .

#### *B. ENERGY MODEL*

We use the energy model from [29]. Details for the parameters are listed in Table. 2.

$$
E_{Tx}(l,d) = \begin{cases} lE_{\text{elec}} + l\epsilon_{fs}d^2, & d < d_0\\ lE_{\text{elec}} + l\epsilon_{mp}d^4, & \text{else.} \end{cases}
$$
 (1)

The second item in the formula is the transmission energy for *l* bits and the first item is the device holding energy for *l* bits. *d* is the distance of the edge connecting the transmitter and the receiver

$$
E_{Rx}(l, d) = lE_{\text{elec}}.\tag{2}
$$

#### *C. OBJECTIVE FUNCTION*

The objective function is the summation of energy consumption per path per edge per computation interval subject to bandwidth capacity and the encoding format according to domain wall encoding [19].

Suppose  $f(d_i)$  is the transmission power consumption on edge *j* with length  $d_i$ . Suppose  $\bar{X} = x_i | i \leq K$  indicates whether a path has been selected or not. *K* is the total number of available paths. We go over all the edges and within each edge *j*, we go through all the paths. And within each valid path  $i$  that is indicated by  $x_i$ , we add the edge power consumption, which includes both the transmitter and receiver power consumption

$$
\min_{x_i} \sum_{\text{alledge } j} \left\{ f(d_j) \left( \sum_{j \in x_i} x_i r_n \Delta t \right) + 2 * E_{\text{elec}} * \sum_{j \in x_i} x_i r_n \Delta t \right\}
$$
\n
$$
\text{s.t.} \sum_{j \in x_i} x_i * r_n \le C_{\text{max}} \ \forall \text{edge } j
$$
\n
$$
\sum_{x_i \in n} x_i = 1 \ \forall n. \tag{3}
$$

We apply the slack variable technique to mitigate the inequality and equality constraint. As  $x_i$  is either 0 or 1, it can be equivalently transferred to  $x_i^2$  such that the objective function becomes a quadratic function with a constant term, which will be omitted in computation

$$
f_{obj} = \sum_{\text{all edge } j} \left\{ f(d_j) \left( \sum_{j \in x_i} x_i r_n \Delta t \right) \right\}
$$
  
+  $2 * E_{\text{elec}} \sum_{j \in x_i} x_i r_n \Delta t + \lambda_1 \left( \sum_{j \in x_i} x_i r_n - C_{\text{max}} \right) \right\}$   
+ 
$$
\sum_{\text{all stream } n} \lambda_2 \left( \sum_{x_i \in n} x_i - 1 \right)^2
$$
  
= 
$$
\sum_{\text{all edge } j} \left\{ \sum_{j \in x_i} (x_i)^2 [r_n \lambda_1 + 2 * E_{\text{elec}} r_n \Delta t + f(d_j) r_n \Delta t] \right\}
$$
  
- 
$$
C_{\text{max}} * \lambda_1 * \sum_{\text{all edge } j \text{ all stream } n} \sum_{j \in n} \mathbf{I}_{j,n}
$$
  
+ 
$$
\sum_{\text{all stream } n} (\lambda_2 - 2) \sum_{x_i \in n} (x_i)^2 + 2\lambda_2 \sum_{i \neq j} x_i x_j
$$
  
+ 
$$
\lambda_2 * n.
$$
 (4)

As the second constraint sum<sub> $x_i \in n x_i = 1 \forall n$  of the optimiza-</sub> tion problem falls into the one-hot encoding format.

In order to save the computational resources (number of logical/physical qubits) so as to ease the actual computational process, we converted the encoding of the whole problem into domain wall encoding, the explanation of which is as follows.

## **IV. TRANSLATION TO DOMAIN-WALL ENCODING**

Motivated by the enhanced performance seen in [30] and [31] (although not yet shown on a real engineering problem on a quantum annealer), we employ the domain-wall encoding scheme first proposed in [19], and to translate this encoding, we first replace one-hot constraints with

$$
H_K = -\lambda \left[ \sum_{i=0}^{K-2} Z_i Z_{i+1} - Z_0 + Z_{K-1} \right]
$$
 (5)

where  $Z_i = -2\bar{x}_i + 1$  are Ising variables used to construct that encoding (note that the  $\bar{x}$  is used to distinguish these variables from the original variables  $x$ ), since we wish to work in a QUBO formulation, we substitute to obtain

$$
H_K = -\lambda \left[ \sum_{i=0}^{K-2} 4\bar{x}_i \bar{x}_{i+1} - 2\bar{x}_i - 2\bar{x}_{i+1} + 2\bar{x}_0 - 2\bar{x}_{K-1} \right] - \lambda
$$
\n(6)

which can directly be used to replace variables under a onehot constraint such that

$$
x_i \rightarrow \begin{cases} \bar{x}_i, & i = 0\\ \bar{x}_i - \bar{x}_{i-1}, & 0 < i < K - 1\\ -\bar{x}_{i-1}, & i = K - 1\\ \text{undefined}, & \text{otherwise.} \end{cases}
$$
(7)

Since this translation takes linear terms to linear terms, a quadratic formula in *x* will also be quadratic in  $\bar{x}$ . Moving to a domain wall rather than one-hot encoding will generally have complicated effects on the dynamics of the system, including properties such as the minimum spectralgap. The goal of the present work is not to gain a detailed understanding of how the encoding affects the dynamics, but all available experimental evidence suggests that it improves performance. For example, Chen et al. [30] show a dramatic improvement in performance in solving coloring problems. Meanwhile, Berwald et al. [31] explain this improvement both in terms of entropic arguments related to the size of the solution space, and a physical mechanism related to perturbative dynamics of bit flips within the encoding.

## **V. ALGORITHM**

Subprocedure *getEdgeM* in line 2 of Algorithm 2 is to form a virtual three-dimensional matrix that  $pID = M_{i,j,k}$ . *pID* is the path ID assigned consecutively when running the *PathCollector* algorithm. In  $M_{i,j,k}$ , *i*, *j* is the node ID and  $(i, j)$  indicates the edge that connects node *i* and node *j*. *k* indicates the *k*th path that goes through the edge (*i*, *j*). In the implementation, a two-dimensional matrix of size  $N*N$ by *Path*\_*Amount* is created instead for manipulation convenience. In this case,  $(i, j, k)$  in the virtual three-dimensional matrix corresponds to the  $((i - 1) * N + j)$ th position in the row and *k*th position in the column in the real twodimensional matrix.

### **VI. EXPERIMENT**

Configuration parameters for the experiments are listed in Table. 3. The goal of the experiment is to evaluate the performance of the QPU against classical solvers (Cplex and Gurobi) in a multiobjective routing problem that has been

Algorithm 1: Mapping Algorithm.

Result: The Mapped Matrix Q **Input:** Graph **Output: Q** 

foreach  $edge_j$  do

**for each** *each original route*<sub>i</sub> **do**  
\n**if** *route*<sub>i</sub> *go through edge*<sub>j</sub> **then**  
\n
$$
Q[i, i] = Q[i, i] + ['r_n^2 * (\lambda_1 - 2\lambda_2 C_{\text{max}}) + 2E_{\text{elec}} r_n \Delta t + f(d_j) r_n \Delta t]
$$
\n**foreach** *route*<sub>i</sub> *go through edge*<sub>j</sub> *and*  
\n
$$
h \neq i
$$
 **do**  
\n
$$
Q[i, h] = Q[i, h] + \lambda_1 2r_n^2
$$
\n**end**  
\n**check** 
$$
KL + (j - 1)K' < i \leq KL + jK'
$$
 **do**  
\n
$$
k = (i - KL) \mod K'
$$
  
\n
$$
Q[i][i] = Q[i][i] + (\lambda_1 k^2 - 2\lambda_1 C_{\text{max}} k)
$$
  
\n**foreach** 
$$
i < q < KL + jK'
$$
 **do**  
\n
$$
|Q[i][q] = 2\lambda_1 k^2
$$
\n**end**  
\n**end**

**foreach** each packetstream<sub>n</sub> do

**foreach** each route<sub>i</sub> belongs to stream<sub>n</sub> do  $Q[i, i] = Q[i, i] + \lambda_2 - 2$ **foreach** route<sub>j</sub> belongs to stream<sub>n</sub> and  $i > i$  do  $[Q[i,j] = Q[i,j] + 2 * \lambda_2]$ end end end

**Algorithm 2:** Hybrid Algorithm Procedure.

- 1: Call the subprocedure to collect all feasible paths PathCollector
- 2: Call the subprocedure to assign paths to respective edges - getEdgeM
- 3: Call the subprocedure to formulate QUBO problem - makeEffArray
- 4: Call the subprocedure to encode the QUBO problem - makeEncoding
- 5: Call the QPU API Solver

formulated into a QUBO. We expect that QPU given current hardware maturity can guarantee a solution quality as good as the classical solvers while at a faster speed.

## *A. CONFIGURATION AND SETUP*

Two random number generators are used. One is to generate the probability following a uniform distribution. That is *p*. If  $p > 0.5$ , a value is generated by the second random number



**Require:** adjacency matrix, destination ID, source ID array, maxflownum

- **for all** destination and source pair **do**
- 2: no node has been assigned the relay role yet
- **while** path amount is less than maxflownum **do** 4: **while** the last relay node is not the destination node **do**

Find the next relay node

- 6: Tick this node as assigned
- **end while**
- 8: **end while end for**

generator uniformly distributed over 1 to 5 and it is assigned to be the corresponding flow rate.

Since we are interested in the ability of the annealers to provide samples very quickly, we have used 10 samples for every anneal, except where stated otherwise. For the classical solvers, we deployed timers to record the time before the solver call and after the solver call and calculate the lap between them. For the QPU, we use qpu\_sampling\_time within the "timing" info as the processing time per run. We are using the default anneal time of 20  $\mu$ s for each run. We further use the fixed\_variable technique [32] to slim the effective QUBO size submitted to the QPU.

There are two target experiment types that we have done. The first is that we go over all the possible combinations of graph size up to size 12 and source number excluding the randomness of the flow rate per source and the second is that we apply the Erdős–Rényí graph generation algorithm (assigning different edge existence probabilities) and generate 20 problem samples each graph size from (4 to 12) and run the statistical analysis.

# *B. EXPERIMENTAL METHODS AND DATA REPORTING*

There are several quantities that we used as axes on our plots, for the readers convenience, we define them here (see Section III for details of problem formulation).

- 1) Source number: The number of nodes on the network graph that acts as sources within the network.
- 2) Graph size: The size of the graph used in the network problem, larger graphs will typically lead to larger QU-BOs.
- 3) Edge probability: The probability of an edge appearing within an Erdös–Rényi random graph used to construct the routing problems.
- 4) QUBO size: The number of binary variables used in the problem that is passed to the annealer or classical solver, this number is always quoted before minor embedding is performed to allow a fair comparison across solvers. The QUBO size we report is after variable fixing has been performed.
- 5) Performance degradation graph size: The point along axis one step ahead of the cross point where Correct Rate intersects with Incorrect Rate or Embedding Error Rate.
- 6) Correctness rate: The number of solutions from QPU that reach the minimum to the overall number of problem instances (the fraction of the samples that returned an optimal solution).
- 7) Processing time: The time taken to attain a feasible solution. In our experiments, we consider the QPU sampling time as the Processing time.
- 8) Embedding error rate: The number of problem instances that fail to be embedded onto the QPU to the overall number of problem instances.
- 9) Incorrect rate: The number of solutions from the QPU where none of the returned solutions reach the minimum energy found for all solvers. Note that Correctness rate +Incorrect rate+ Embedding error rate sum to one.

We often plot the correctness rate for different solvers and we use this as a key metric to compare performance between the QPUs and classical solver over different quantities such as QUBO size, source number, or the graph size.

We used macOS Sierra version 10.12.6 to run the classical algorithms. The processor is a 3.4-GHz Intel Core i7, and the memory is a 16-GB, 1333 MHz-DDR3.

For all experiments reported here, we performed 10 reads on the quantum annealer, we have chosen this relatively small number of reads to assess the ability to attain a "good solution quickly" as it is likely that solving network problems like those described here will be very time-sensitive in most real applications. It is likely that some quantities, such as the probability that a valid solution is ever found for a given problem, would be substantially improved by taking more reads.

# *C. DATA AVAILABILITY*

The data that support the findings of this study are available from the corresponding author upon reasonable request.

# **VII. RESULTS**

Before getting into the discussion of how the plots depend on the properties of the graph problem we are solving, it is worth briefly stepping back and seeing how they depend on lower-level properties, from Fig. 2, we see that for a broad sampling of the data, the correctness rate correlates strongly with QUBO size with a relatively narrow window where success probability drops off from approximately 1 to approximately 0. We also observe that the success probability is increased by taking more reads; however, in this article, we are interested in being able to get a good solution very quickly, so we base the data in the remainder of the paper on 10 reads.

#### **TABLE III List of Parameter Configurations Used in This Article**





**FIGURE 2. Advantage\_System Correctness Plot\_ Erdos\_Renyi: Plot of correctness rates for graph sizes up to size 12 and source numbers one up to 11, and edge probabilities 0.6–0.9.**



**FIGURE 3. Plot of different measures of success for Advantage\_System QPU versus source number using exhaustively generated graphs of size 5, see text for details.**

#### *A. CORRECTNESS*

### 1) CORRECTNESS RATE BASED ON BRUTE FORCE GRAPH GENERATION ALGORITHM

We ran over all the possible combinations of graph topology and traffic source for graph sizes 4 and 5. The plots in Figs. 3 and 4 show the correctness rate (defined as the fraction of feasible solutions obtained in a given experiment) against the source number. There are the following three categories that the result data from QPU can fall into:

- 1) QPU reports embedding error and hence cannot solve the problem;
- 2) QPU solves the problem but it is not the most optimal;
- 3) QPU provides the most optimal solution.



**FIGURE 4. Plot of different measures of success for 2000Q QPU versus source number using exhaustively generated graphs of size 5, see text for details.**

We note that for all cases at graph size 5, the problem can be embedded and solved to optimality by the QPU.

We also note from Fig. 19 that if more samples were taken the range in which this transition occurs increases, but the qualitative shape remains the same. In this article, we are restricting ourselves to studying how the annealer performs when restricted to running for a very short time and, therefore, a small number of samples, but it is worth remarking that many of the problems tested in this article could be solved eventually with more anneals.

From these plots, we can tell from the data that advantage\_sys1.1 has an absolute advantage in terms of speed as QUBO size increases to around 10. Up to around size 20, the QPUs are typically able to solve the problems within the 10 reads we take. By a one-by-one eye-check of the data, we can tell that in these experiments 2000Q also outperforms classical solvers in terms of speed. As the solution is not found as quickly as the advantage\_sys1.1, in this plot, the speediness correctness rate (the ratio of the fraction of cases where a solution is found faster) for 2000Q is always 0.

Figs. 3 and 4 depict results for problems generated exhaustively for graph size 5 with source numbers 1–4 and all possible connected graphs. The measures are explained in Section VI-B, the correct and incorrect rates refer to cases where the most optimal solution was or was not found, respectively. The embedding error rate refers to cases where the problem could not be embedded successfully. We can tell from these figures that the correctness rate decreases as the source number increases for both the advantage system



**FIGURE 5. Plot of different measures of success for Advantage\_System QPU versus graph size for graphs generated with the Erdős-Rényi algorithm with an edge probability of 0.6.**

and 2000Q. This is probably because the QUBO size increases when the number of sources increases. Furthermore, the advantage system keeps a more than 60% faster rate than both the classical solvers and 2000Q across all possible numbers of source nodes. Even further, at the highest number of source nodes, the faster rate for the advantage system reaches the highest value among all. We suspect it is because given highest number of source nodes, the practical QUBOs submitted for all the four solvers become more complicated. While classical solvers can tackle the smaller size of QUBO problems at a faster rate (we suspect that the QPU processing time might decrease at the same solution quality if we reduce the sample number per run to 5 or 3), they are losing ground for larger QUBO size to QPU solvers possibly because of the parallel solution searching mechanism facilitated by quantum mechanics.

From the analysis of data collected from all the problem instances for graph size 4 that are feasible for submission to the QPU, we can tell that the QPU demonstrates an absolute advantage over the classical solvers we tested in terms of solution quality across all the problem space. It does not show an advantage in the speed with a number of reads equal to 3000. It is because the overall QUBO size is small  $(= 5)$ so it is fast enough for classical solvers to attain a correct solution and when the number of runs is to be decreased to 5, the QPU speed will be overriding those by the classical solvers without degrading the solution quality.

## 2) CORRECTNESS RATE BASED ON PROBABILISTIC GRAPH GENERATION ALGORITHM

Figs. 5–11 depict relevant quantities for data collected by using the Erdős–Rényi graph generator with the edge probability set to 0.6, 0.7, and 0.9 separately. We generated 20 graph samples per edge probability and do the average in the analysis. For Figs. 5–10, the correct and incorrect rates refer to cases where the most optimal solution was or was not found, respectively. The embedding error rate refers to cases where the problem could not be embedded successfully, and



**FIGURE 6. Plot of different measures of success for 2000Q QPU versus** graph size for graphs generated with the Erdős-Rényi algorithm with an **edge probability of 0.6. See text for details.**



**FIGURE 7. Plot of different measures of success for Advantage\_System QPU versus graph size for graphs generated with the Erdős-Rényi algorithm with an edge probability of 0.7. See text for details.**



**FIGURE 8. Plot of different measures of success for 2000Q QPU versus** graph size for graphs generated with the Erdős-Rényi algorithm with an **edge probability of 0.7. See text for details.**

the measures are explained in Section VI-B. These plots differ only in the edge probability and the QPU used.

We can tell that for edge probability 0.6, advantage\_system's performance starts to degrade at graph size 10 while 2000Q system's performance starts to degrade at graph



**FIGURE 9. Plot of different measures of success for Advantage\_System QPU versus graph size for graphs generated with the Erdős-Rényi algorithm with an edge probability of 0.9. See text for details.**



**FIGURE 10. Plot of different measures of success for 2000Q QPU versus** graph size for graphs generated with the Erdős-Rényi algorithm with an **edge probability of 0.9, see text for details.**



**FIGURE 11. QUBO size versus graph size for graphs generated by the Erdős-Rényi algorithm for different edge probabilities.** 

size 9. Embedding errors are reported occasionally for the graph size equal to 12.

As we increase the edge probability to 0.7, intuitively we suspect the graph becomes more complex and 11 shows that as the edge probability increases, the trimmed QUBO size increases. A larger share of embedding error cases emerges. For advantage\_system, the performance starts to degrade at



**FIGURE 12. Scatter plot of the speediness of 2000Q QPU versus Cplex. The blue line shows equal times and is a guide to the eye. Plotted for over all graphs of size 5.**



**FIGURE 13. Scatter plot of the speediness of 2000Q QPU versus Gurobi. The blue line shows equal times and is a guide to the eye. Plotted for over all graphs of size 5.**

graph size 9 while for 2000Q system, it is at graph size 8. Furthermore, more we notice that for advantage\_system, embedding errors occur by around 20% for the graph size equal to 11 and this figure increases to 80% when the graph size reaches 12. For 2000Q, embedding errors appear at graph size 8 at around 20% and reach 100% at graph size 11 and onward.

At the edge probability of 0.9, the degradation graph size is 8 for advantage\_system while 7 for 2000Q. Furthermore, advantage\_system starts to report embedding error at a higher rate when the graph size reaches 10 and onward while for 2000Q, the graph size value is 8 with around 80% embedding error rate.

#### *B. SPEEDINESS*

# 1) SPEEDINESS BASED ON BRUTE FORCE GRAPH GENERATION ALGORITHM

For the network size of 5, we compare the processing time between the classical solvers and the QPUs, we ignore cases where embedding errors were encountered for this analysis. The percentage of problems that reports embedding error is 57%. We observe from Figs. 12–15 that QPUs have a nearly constant value of processing time across almost



**FIGURE 14. Scatter plot of the speediness of Advantage\_System QPU versus Cplex. The blue line shows equal times and is a guide to the eye. Plotted for over all graphs of size 5.**



**FIGURE 15. Scatter plot of the speediness of Advantage\_System QPU versus Gurobi. The blue line shows equal times and is a guide to the eye. Plotted for over all graphs of size 5.**



**FIGURE 16. Comparison of 2000Q QPU Speediness with Gurobi averaged for different graph sizes. This plot uses graphs generated with the Erdos–Rényi algorithm. ˝**

all the valid problem instances. For 2000Q, the processing time is as constant as 0.0025 s while for Advantage\_system the processing time is nearly half that value. There exists a larger portion of valid problem instances for 2000Q that consume longer processing time than for Advantage\_system against both Gurobi and Cplex. We further notice that Cplex



**FIGURE 17. Comparison of 2000Q QPU Speediness with Cplex averaged for different graph sizes. This plot uses graphs generated with the Erdos–Rényi algorithm. ˝**



**FIGURE 18. Comparison of Advantage\_System QPU Speediness with Cplex averaged for different graph sizes. This plot uses graphs generated with the Erdős-Rényi algorithm.** 



**FIGURE 19. Comparison of Advantage\_System QPU Speediness with Gurobi averaged for different graph sizes. This plot uses graphs generated with the Erdos–Rényi algorithm. ˝**

works noticeably longer than Gurobi for all valid problems. Figs. 16–19 show the average processing time (in seconds) per graph size for QPUs and classical solvers, respectively. We excluded problems where embedding errors occurred on either QPU. Hence, readers will notice that for Figs. 16–19 the plots of the processing time for classical solvers have similar patterns, respectively. To be more specific, from previous figures, we can tell that 2000Q is running faster to encounter embedding errors as the graph size increases, compared with the Advantage\_system.

## 2) SPEEDINESS BASED ON PROBABILISTIC GRAPH GENERATION ALGORITHM

As the same as what has been observed from 12, 2000Q shows a constant processing time on average. While for Advantage\_system, the average processing time goes up the graph size increases but stops increasing certain graph sizes and beyond. For Edge probability equal to 0.9, this occurs at size 9, for edge probability equal to 0.7, this happens at size 11 while for edge probability equal to 0.6, we cannot see this effect and hypothesize that this may happen beyond size 12—our experiment graph size upper limit. From previous figures, we have come to agree that for edge probability equal to 0.9 with a graph size larger than 9, only problem instances below graph size 9 can consistently be embedded well onto the QPUs and return valid solutions. The similar conjecture can be applied to cases where the edge probability is less with larger turning points. For the phenomenon that average processing time is lessened for even larger graph sizes, we suspect the graph size alone cannot determine the complexity of the network. Other factors take effect such as the structure of the network.

The Cplex average processing time seems to correlate less with the graph size and the edge probability while for Gurobi, Figs. 16 and 19 show that the average processing time goes up as the graph size increases in general and with larger edge probability. If this trend continues, it suggests that for larger problems there may be a crossover where Cplex becomes more effective.

## **VIII. CONCLUSION**

We have studied the performance of two D-Wave QPUs on small network routing problems with a limited number of reads from the processor. By comparing this to the well-used Gurobi and Cplex classical solvers on a standard workstation, we find that both the 2000Q and Advantage yield superior performance in terms of absolute runtime. This is an encouraging proof-of-concept result for the application of similar QPUs to this kind of problem. We find that the most relevant quantity to determine QPU performance is the overall size of the QUBO that we apply it to, although we did find that both the size of the underlying network graph, and the number of sources had a significant effect as well. While most of the problems here involved small QUBOs, larger ones were occasionally also generated. Even within a few reads the QPUs were able to solve most QUBOs below size about 20 and were not able to beyond this size. While this range is still accessible by exhaustive search methods, this study still provides useful proof-of-concept, as the problems could often be solved very quickly. This work suggests a route to practical quantum advantage where problems that can be solved classically still yield an advantage by being solved much more quickly.

## *A. DISCUSSION I*

## 1) PHASE I

Some preliminary experiments (not presented in this article) are conducted in ns3, the codes of which have been made public via [https://github.com/cjie3331/quantumrouting.](https://github.com/cjie3331/quantumrouting) They demonstrated the feasibility of applying a QPU in the network routing design softwaredly. By experiments (presented in this article) conducted in python, we have shown the advantage of QPU over classical solvers toward the same QUBO problem tailored to optimal route selection. It is our interest to run the performance comparison in ns3 between QPU and classical solvers in the near future and then compare the overall design to current state-of-the-art heuristic algorithm such as various localized learning algorithms. Due to the limited number of qubits supported by current QPU hardware, it is our plan to employ the clustering concept in sensor networks to assign controller to each micronetwork in a hierarchical manner. Last but not least, we intend to implement the overall hierarchical design into automated vehicular communication based on the justification that faster computation turn-around time can more seamlessly monitor/manage the communication process to its best effort.

## 2) PHASE II

Jie Chen at this phase has successfully executed the plan to borrow the clustering technique for energy efficiency purpose in general network routing. Jie Chen has compared the results with Advanced\_Leach algorithm (benchmark) in the literature. Here, she describes the settings briefly and provides a batch of the result. The application scenario is 100 m  $\times$  100 m circular area with 200 nodes randomly distributed with a fixed sink node in the circle center. She uses the measurement metrics of First Node Die (FND), Half Node Die (HND), and Full Node Die (FND). For FND, it is 2122 in the new design while 865 is for the benchmark. For HND, it is 2493 in the new design while 1929 is for the benchmark. For FND, it is 4998 in the new design while 3559 for the benchmark.

## *B. DISCUSSION II*

In this work, the authors proposed a generalized sensor network routing problem. And results both in terms of speediness and also correctness are optimal in comparison with those attained from the commercially available classical solvers. The authors suspect by hardware interpretation, it means this kindred of problem structure falls neatly into the D-wave machine underlying qubit network topology. There exist relatively less chain-breaks that prohibit the machine return valid solutions. From this point, the authors suggest the following strategy toward embedding a network optimization problem into a quantum processor unit properly: encode the problem effectively and efficiently. Effectiveness means the QUBO formulation should work. Efficiency means the QUBO size should be as economic as possible. The author has tried to embed some other network design problems. It is due to the overexpanding QUBO size submitted to the Solver API, the solutions returned are not optimal. The author did not use the roof\_duality strategy to slim the QUBO size though.

With the effectiveness and efficiency strategy, the authors endeavor to propose wider usage and more practice of employing a quantum machine in network computation problems, especially in optimization.

The authors dare to propose further for a novel quantum network processor design. A network processor that encapsulates the classical design components while embedding a quantum routing algorithm. By classical design components, the author suggests to stay with encapsulated layered protocol stack design in the hope that quantum advantage can be seamlessly integrated into the conventional network infrastructure and to increase the quantum network design acceptance by practitioners and market players who are working with/pertaining to various classical techniques and ideas.

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